37 AUTOMATIC SEND-RECEIVE (ASR) TELETYPEWRITER SET

FOR SWITCHED NETWORK SERVICE

WIRING DIAGRAM AND CIRCUIT DESCRIPTIONS

CONTENTS PAGE

1. GENERAL

1.01 This section is issued to provide actual and schematic wiring diagrams and detailed circuit description information for the 37 Automatic Send-Receive (ASR) Teletypewriter Set (Figure 1).

1.02 Notes are included on the diagrams and explain the symbols used or point out special conditions that should be observed.

1.03 Most wiring diagrams (WDs) and circuit descriptions (CDs) in this section are a part of one or more wiring diagram packages (WDPs). A complete listing of these WDs and CDs is found on the attached WDP control sheets, and a numerical summary is included in the wiring diagram index. Other WDs and CDs which are not a part of a basic set or logic card WDPs are listed separately in the index in numerical order.

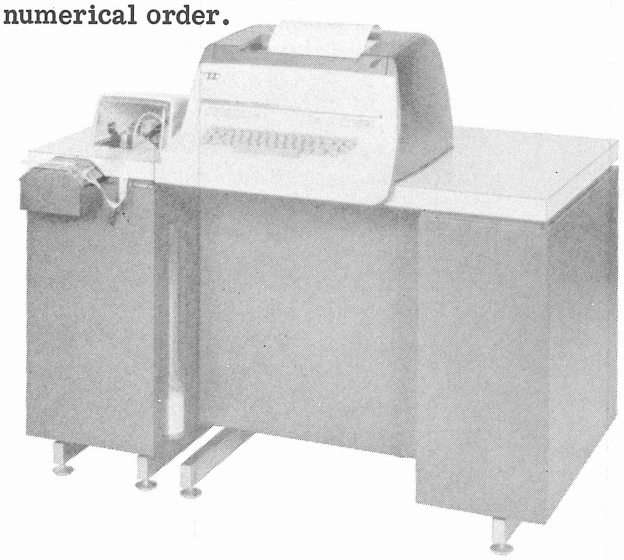

Figure 1 - 37 ASR Teletypewriter Set

WIRING DIAGRAM INDEX (ATTACHMENTS)

DRAWING NUMBER	ISSUE NUMBER	TITLE
Wiring Diagram Packages		
WDP0118	10	Basic Wiring Diagram Package for 37 RO, KSR, and ASR Sets. It includes the following WDs and CDs: 8352WD 8360WD 8353WD 8361WD 8358WD 8365WD 8358CD 303150 8359WD

Prepared for American Telephone and Telegraph Company by Teletype Corporation

WIRING DIAGRAM INDEX (continued)

DRAWING NUMBER	ISSUE NUMBER	TITLE
Wiring Diagram Packages		
WDP0127	10	Wiring Diagram Package for Circuit Card Set TP332652 (ASR). It includes the following WDs and CDs: 7856WD 8369WD 8370WD 8370CD 8371WD 8371CD 8374WD 8374CD 8375WD 8375CD 8376WD 8376CD 8380WD 8380CD 8383WD 8383CD 8386WD 8386CD 8388WD 8388CD 8389WD 8389CD 8395WD 8395CD 8399WD 8772WD 8772CD 303149 322044 322045 322047 322055 322059 322062 322066 322068 322070 322079 322303
WDP0128	2	Wiring Diagram Package for Circuit Card Set TP332563 (Tape Module). It includes the following WDs and CDs: 7856WD 8370WD 8370CD 8379WD 8379CD 8399WD 303149 322054

WIRING DIAGRAM INDEX (continued)

DRAWING NUMBER	ISSUE NUMBER	TITLE
Wiring Diagram Packages		
WDP0129	9	Basic Wiring Diagram Package for 37 Tape Module. It includes the following WDs: 8354WD 8355WD 8365WD
Other Wiring Diagram and Circuit Descriptions		
5072WD	3	Reader — Actual
7828WD	7	Motor Unit — Actual
7874WD	7	Base — Actual
8362WD	3	Typing Unit (37P001/001/AA and 37P001/001/AB) — Actual
8363WD	2	Function Box (TP319655, TP319776, TP319875) — Actual
8364WD	3	Typing Unit (37P001/001/AD) — Actual
8494WD	3	Non-Typing Reperforator — Actual
8497WD	3	Tape Cabinet — Actual
8500WD	1	Keyboard — Actual and Schematic
8558WD	2	Tape Cabinet Doors — Actual

WIRING DIAGRAM PACKAGE FOR CIRCUIT CARD SET 332652 (ASR)

WDP 0127

DRAWING NO.	SHEET NO.	DESCRIPTION	ISSUE NUMBER 1	2	3	4	5	6	7	8	9	10
7856WD	1	OPTION ANALYSIS CHART	1	1	1	1	2	2	2	2	2	2
8399WD	1	TRUTH TABLES AND LOGIC SYMBOLS	1	1	1	1	1	1	1	1	1	1
8371WD	1	SCHEMATIC DISTRIBUTOR LOGIC	1	1	1	1	1	1	1	1	1	1
8371WD	2	SCHEMATIC DISTRIBUTOR LOGIC	1	1	1	1	1	1	1	1	1	1
8772WD	1	SCHEMATIC ASR SEND CONTROL	1	1	1	1	1	1	1	1	1	1
8772WD	2	SCHEMATIC ASR SEND CONTROL	1	1	1	1	1	1	1	1	1	1
8386WD	1	SCHEMATIC ASR MODE CONTROL	1	1	1	1	1	1	1	1	1	1
8383WD	1	SCHEMATIC RECEIVE CONTROL (W/REGENERATOR)	1	1	1	2	2	2	2	2	2	2
8383WD	2	SCHEMATIC RECEIVE CONTROL (W/REGENERATOR)	1	1	1	1	1	1	1	1	1	1
8388WD	1	SCHEMATIC CHANNEL CONTROL	1	1	1	1	1	1	1	1	1	1
8388WD	2	SCHEMATIC CHANNEL CONTROL	1	1	1	2	2	2	2	2	2	2
8388WD	3	SCHEMATIC CHANNEL CONTROL	1	1	1	1	1	1	1	1	1	1
8374WD	1	SCHEMATIC KEYBOARD CONTROL	1	1	1	1	1	1	1	1	1	1
8375WD	1	SCHEMATIC CHARACTER COUNTER	1	1	1	1	1	1	1	1	1	1
8380WD	1	SCHEMATIC COUNTER CONTROL (BI-DIRECTIONAL)	1	1	1	1	1	1	1	1	1	1
8380WD	2	SCHEMATIC COUNTER CONTROL (BI-DIRECTIONAL)	1	1	1	1	1	1	1	1	1	1
8395WD	1	SCHEMATIC ALARMS AND AUTOMATIC CONTROL	1	1	1	1	1	1	1	1	1	2
8395WD	2	SCHEMATIC ALARMS AND AUTOMATIC CONTROL	1	1	1	1	1	1	1	1	1	1
8370WD	1	SCHEMATIC RECEIVING DEVICE	1	1	1	1	1	1	1	1	1	1
8369WD	1	ACTUAL AND SCHEMATIC FOR 327801 ANSWER BACK	—	—	—	—	—	—	4	4	4	4
8376WD	1	SCHEMATIC ANSWER BACK DRIVER	—	—	—	—	—	—	3	3	3	3
8389WD	1	SCHEMATIC TWO COLOR RIBBON CONTROL	—	—	—	—	—	—	1	1	1	1

TELETYPE CORPORATION

NOTE : THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF WDP.

R&D FORM 361 (6-66)

WIRING DIAGRAM PACKAGE FOR CIRCUIT CARD SET 332652 (ASR)

WDP 0127

DRAWING NO.	SHEET NO.	DESCRIPTION	ISSUE NUMBER 1	2	3	4	5	6	7	8	9	10
303149	1	CIRCUIT CARD RECEIVING DEVICE	4	4	4A	4A	4A	4A	6	6	6	6
322059	1	CIRCUIT CARD DISTRIBUTOR LOGIC	~~2~~	~~2~~	~~2A~~	~~2A~~	~~2A~~	~~2A~~	~~4~~	~~4~~	~~4~~	1
322044	1	CIRCUIT CARD KEYBOARD CONTROL	5	5	5	5	5	5	6	6	6	6
322045	1	CIRCUIT CARD CHARACTER COUNTER	1	1	2	2	2	2	2	3	3	3
322055	1	CIRCUIT CARD COUNTER CONTROL	2	2	2	2	2	2	3	4	4	4
322303	1	CIRCUIT CARD ASR SEND CONTROL	—	—	1	1	1	1	1	1	1	1
322062	1	CIRCUIT CARD RECEIVE CONTROL (W/REGENERATOR)	3	3	3	3A	3A	3A	4	4	5	5
322066	1	CIRCUIT CARD ASR MODE CONTROL	5	5	6	6	6	6	6	6	6	6
322068	1	CIRCUIT CARD-CHANNEL CONTROL	5	5	5B	5B	5B	5B	7	7	7	7
322079	1	CIRCUIT CARD-AUTOMATIC ALARMS AND CONTROL	4	4	4	4	4	4	5	5	5	5
322047	1	CIRCUIT-ANSWER BACK DRIVER							5	6	6	6
322070	1	CIRCUIT CARD-TWO COLOR RIBBON CONTROL							4	4	4	4

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NOTE : THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF WDP.

SHEET 2 OF 3

R & D FORM 361 (6-66)

WIRING DIAGRAM PACKAGE FOR CIRCUIT CARD SET 332652 (ASR)

WDP 0127

DRAWING NO.	SHEET NO.	DESCRIPTION	ISSUE NUMBER 1	2	3	4	5	6	7	8	9	10
8371WD	CD-ALL	CIRCUIT DESCRIPTION-DISTRIBUTOR LOGIC	1	1	1	1	1	1	1	1	1	1
8772WD	CD-ALL	CIRCUIT DESCRIPTION-ASR SEND CONTROL	1	1	1	1	1	1	1	1	1	1
8386WD	CD-ALL	CIRCUIT DESCRIPTION-ASR MODE CONTROL	1	1	2	2	3	3	3	3	3	3
8383WD	CD-ALL	CIRCUIT DESCRIPTION-RECEIVE CONTROL	1	1	1	1	1	1	2	2	2	2
8388WD	CD-ALL	CIRCUIT DESCRIPTION-CHANNEL CONTROL	1	1	1	1	1	1	1	2	2	2
8374WD	CD-ALL	CIRCUIT DESCRIPTION-KEYBOARD CONTROL	1	1	1	1	1	1	1	1	1	1
8375WD	CD-ALL	CIRCUIT DESCRIPTION-CHARACTER COUNTER	1	1	1	1	1	1	1	1	1	1
8380WD	CD-ALL	CIRCUIT DESCRIPTION-COUNTER CONTROL	1	1	1	1	1	1	1	1	1	1
8395WD	CD-ALL	CIRCUIT DESCRIPTION-AUTOMATIC ALARMS&CONTROL	1	1	1	1	1	1	1	1	1	1
8370WD	CD-ALL	CIRCUIT DESCRIPTION-RECEIVING DEVICE	1	1	1	1	1	1	1	1	1	1
8376WD	CD-ALL	CIRCUIT DESCRIPTION-ANSWER BACK DRIVER							2	2	2	2
8389WD	CD-ALL	CIRCUIT DESCRIPTION-TWO COLOR RIBBON CONTROL							1	1	1	1

TELETYPE CORPORATION

NOTE : THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF WDP.

SHEET 3 OF 3

R & D FORM 361 (6-66)

NO.	NOTES
1	THE FOLLOWING PROCEDURE SHOULD BE FOLLOWED WHEN INSTALLING CIRCUIT CARD OPTIONS: A. TURN POWER OFF B. LOCATE CARD POSITION GIVEN IN INSTALLATION PROCEDURE. C. CHECK POLARITY OF CARDS (NOTCHES) AGAINST POLARITY OF CARD CONNECTOR. (SMALL TAB IN CONNECTOR) D. INSTALL CARD.
2.	THE FOLLOWING PROCEDURE SHOULD BE FOLLOWED WHEN INSTALLING CABLE OPTIONS: A. TURN POWER OFF. B. IDENTIFY WIRES AND TERMINALS TO BE CONNECTED PER INSTALLATION PROCEDURE. C. INSTALL PUSH-ON TERMINAL CONTACTS DIRECTLY OVER ALLOTTED TERMINALS ON WIRING FIELD TERMINAL BOARD. D. DO NOT SHORT OR BEND TERMINALS ON WIRING FIELD TERMINAL BOARD.
3.	IN REMOVING CIRCUIT CARD STRAP OPTIONS CARE SHOULD BE TAKEN TO AVOID: A. DAMAGE TO ADJACENT COMPONENTS AND CIRCUIT BOARD. B. SHORTING REMAINING PORTION OF STRAP TO ADJACENT CIRCUITS. C. LITTERING CARD WITH CUT STRAPS.
4	IN ADDING CIRCUIT CARD STRAP OPTIONS TO PREVIOUSLY PROGRAMMED CARDS, A SOLDERING IRON NOT LARGER THAN 25 WATTS SHOULD BE USED. CARE SHOULD BE TAKEN TO AVOID DAMAGING ADJACENT COMPONENTS OR CIRCUIT BOARD.
5.	REFERENCES TO 8365WD, PRINTER, AND STUNT BOXES INDICATE THAT OPTION IS PART ELECTRICAL AND MECHANICAL.

SERVICE UNIT OPTION ARRANGEMENTS	DESCRIPTION	APPLICATION	ASSEMBLY AFFECTED	INSTALLATION PROCEDURE
X	CHARACTER COUNTER & CONTROL	ASR	322045	INSTALL PIGGY-BACK ON CARD ASSEMBLY 322045 POSITION XZ 301. 1. REMOVE STRAP "A" WHEN "NU-LINE" IS NOT IMPLEMENTED IN PRINTER.
			322055	INSTALL IN POSITION XZ303. 1. PROGRAM P1-P24 FOR A COUNT OF 66 AS FOLLOWS, STRAP P3-P18, P6-P19, P8-P20, P10-P21, P12-P22, P13-P23, P2-P17 2. FOR OTHER COUNTS REFER TO 8380WD-CD.
X	10/11 UNIT CODE 150 WPM.	RO/KSR ASR	322067 322066	PROGRAM CIRCUIT CARD ASSEMBLY AFFECTED. POSITION XZ 105 AS FOLLOWS: 1. 10 UNIT DO NOT REMOVE STRAP "A".
X	HALF & FULL DUPLEX	KSR/ASR	322062	PROGRAM CIRCUIT CARD ASSEMBLY AFFECTED POSITION XZ 107 AS FOLLOWS: (FIELD MODIFICATION ONLY, CARD TO BE SHIPPED WITH ALL STRAPS. 1. DEDICATED HALF DUPLEX - REMOVE STRAPS "B" 2. DEDICATED FULL DUPLEX - REMOVE STRAPS "A" 3. LINE CONTROL OPERATION - REMOVE STRAPS "A B & C". 4. CHECK MECHANICAL PORTIONS OF STUNT BOX FOR APPROPRIATE CODES.
X	RECEIVER STATUS ALARM	KSR/ASR	322062	1. REMOVE STRAP "C"
X	MOTOR CONTROL (DATAPHONE) EOT AND ALARM DISCONNECT.	RO/KSR/ASR	322068	PROGRAM CIRCUIT CARD ASSEMBLY AFFECTED POSITION XZ 109 AS FOLLOWS: 1. REMOVE STRAPS "D, E, G, H, K, M, Y." DO NOT REMOVE STRAPS "A, B, C, F, L".
X	AUTOMATIC READER AND PUNCH CONTROL.	ASR	322079	1. INSTALL CIRCUIT CARD ASSEMBLY IN POSITION XZ 304. 2. PROGRAM CONTROL PANEL PER 8365 WD. 3. CHECK MECHANICAL PORTIONS OF STUNT BOX FOR APPROPRIATE CODES.
			322054	REMOVE STRAP "A" OF CIRCUIT CARD ASSEMBLY POSITION XZ 108 OF R-T ELECTRICAL SERVICE UNIT.
X	TWO COLOR RIBBON.	RO/KSR/ASR	322070	1. INSTALL CIRCUIT CARD ASSEMBLY AFFECTED IN POSITION XZ 405. 2. CHECK PRINTER AND STUNT BOX FOR APPROPRIATE MECHANISM & CODES.
X	ANSWER BACK	RO/KSR/ASR	327801	1. INSTALL THIS SELF CONTAINED ASSEMBLY IN POSITIONS XZ 310-XZ 315. 2. INSTALL CABLE ASSEMBLY 326575 AS FOLLOWS: WIRE COLOR — TBIII CONNECTION. WHITE-BROWN — A 1 WHITE-RED — A 2 WHITE-ORANGE — A 3 WHITE-YELLOW — A 4 WHITE-GREEN — A 5 WHITE-BLUE — A 6 WHITE-PURPLE — A 7 WHITE-SLATE — A 8 WHITE-BLACK — A 11 GREEN-SLATE — J 3 BLUE-GREEN — H 3 ORANGE-GREEN — F 3 RED-BLUE — C 3 YELLOW — A 13 GREEN — A 14 BLACK — G 3 BLUE — A 10 BROWN — D 3 BROWN — E 3

7856 WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	11-21-68	19778 R
2	3-17-69	96904

WDP

MODEL 37
OPTION
ANALYSIS CHART

APPROVALS

D AND R	E OF M
fDm	

E-NUMBER

PROD. NO. 7856 WD.

DATE 9-4-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. CHKD.

ENGD. M.J.R. APPD.

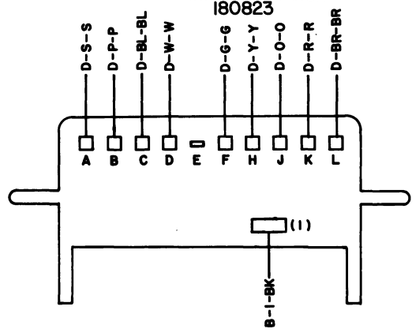
TELETYPE CORPORATION

7856 WD

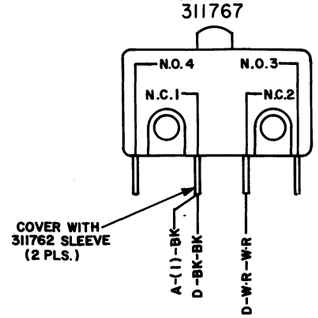
NO.	NOTES
1.	WIRING LEGEND: DISTANT TERMINATING AREA. DISTANT TERMINATING DESIGNATION. A-W-R-W-R WIRE COLOR CODE.
2.	COLOR CODE: Y-YELLOW, W-WHITE, S-SLATE, P-PURPLE, BL-BLUE, G-GREEN, R-RED, O-ORANGE, BR-BROWN, BK-BLACK
3.	INDICATES MALE TERMINAL AND INDICATES FEMALE TERMINAL ON CONNECTOR.
4.	CONNECTORS VIEWED FROM WIRED ENDS.
5.	ASSOCIATED CABLE 326568.
6.	REFERENCE SPEC FOR TELETYPE CORPORATION EMPLOYEES ONLY.
7.	REFER TO 8376 WD-CD FOR SCHEMATIC WIRING DIAGRAM AND CIRCUIT DESCRIPTION.

ACTUAL WIRING DIAGRAM

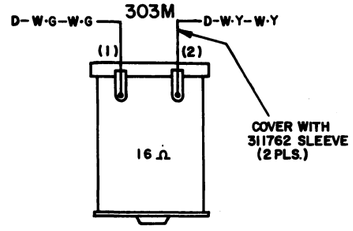
A
CONTACT BLOCK
180823



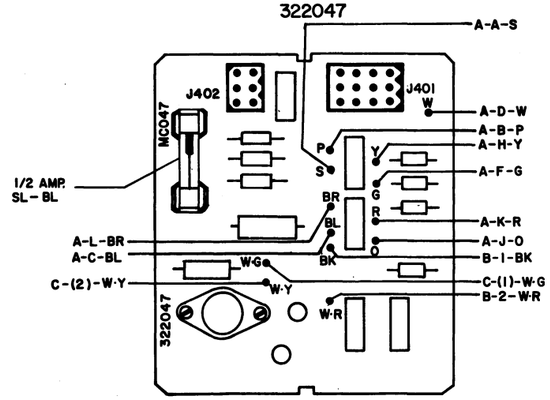
B
SWITCH
311767



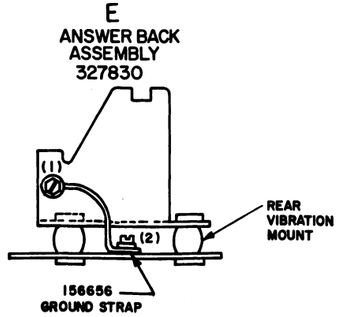
C
RESET
MAGNET
303M



D
ANSWER BACK
DRIVER
322047

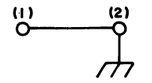


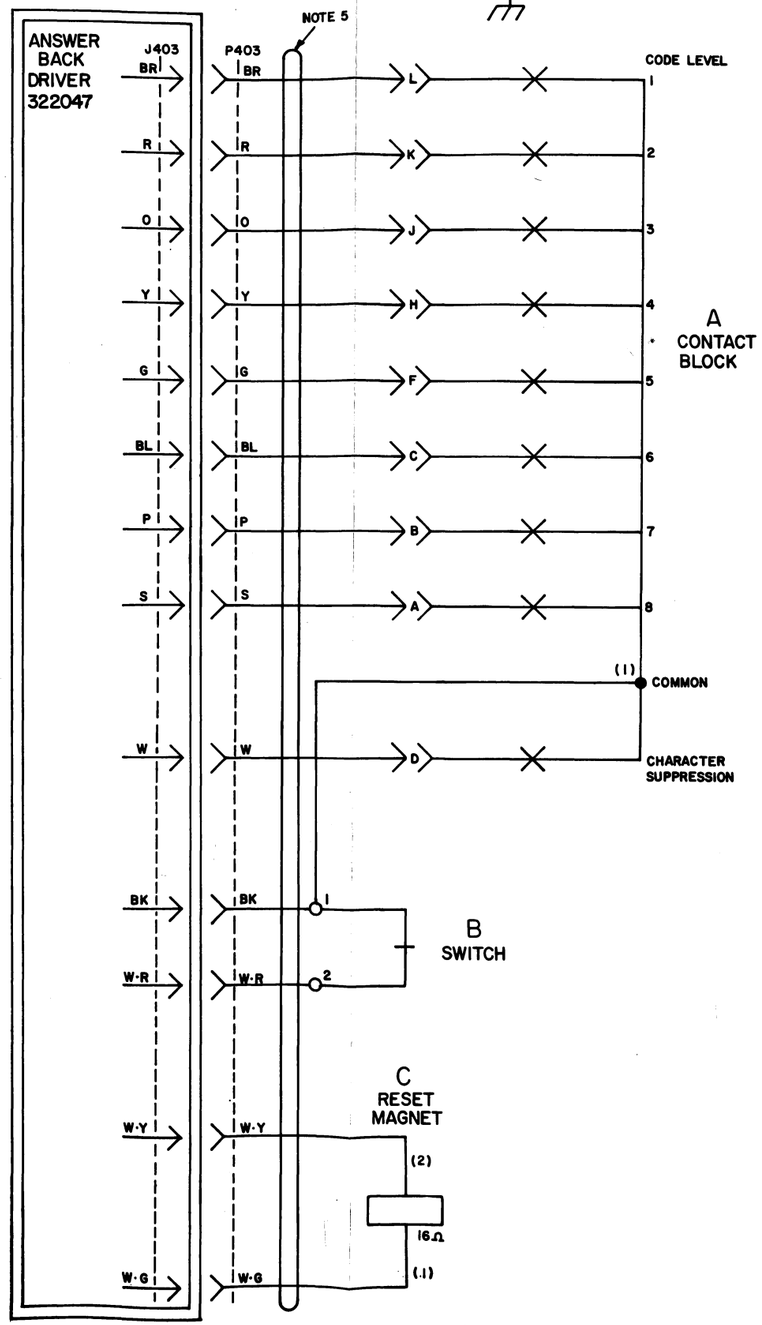
E
ANSWER BACK
ASSEMBLY
327830



SCHEMATIC WIRING DIAGRAM

E
ANSWER BACK
ASSEMBLY





8369WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	5-2-68	19260 R
2	7-2-68	95927
3	8-23-68	96117
4	1-3-69	96485

ACTUAL & SCHEMATIC WIRING DIAGRAM FOR 327801 ANSWERBACK

APPROVALS

D AND R	E OF M
HAK	C

E-NUMBER

PROD. NO. 8369WD

DATE 1-22-68

P.D. FILE NO. G-A354AA

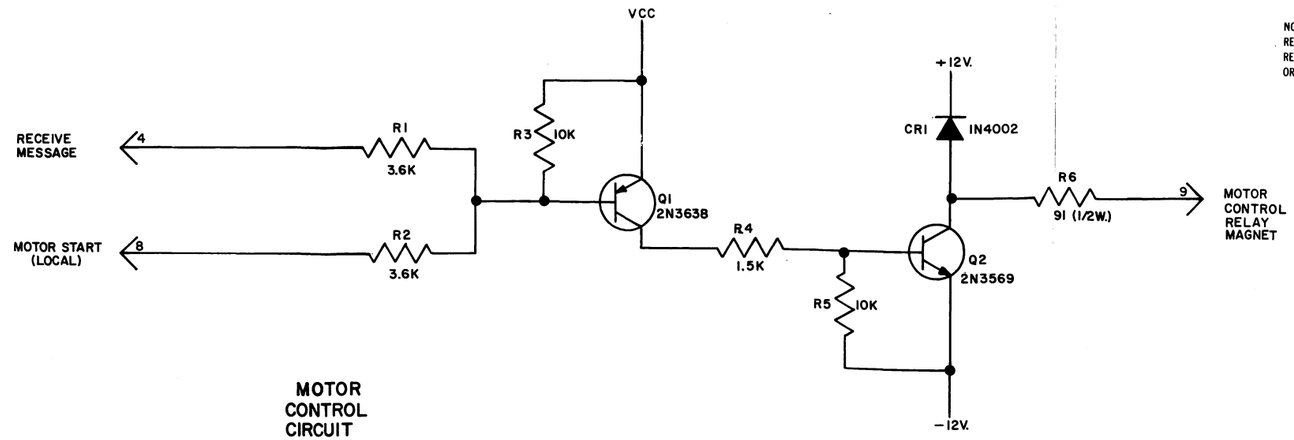
DRAWN RJP	CHKD.
ENGD. AB	APPD.

TELETYPE CORPORATION

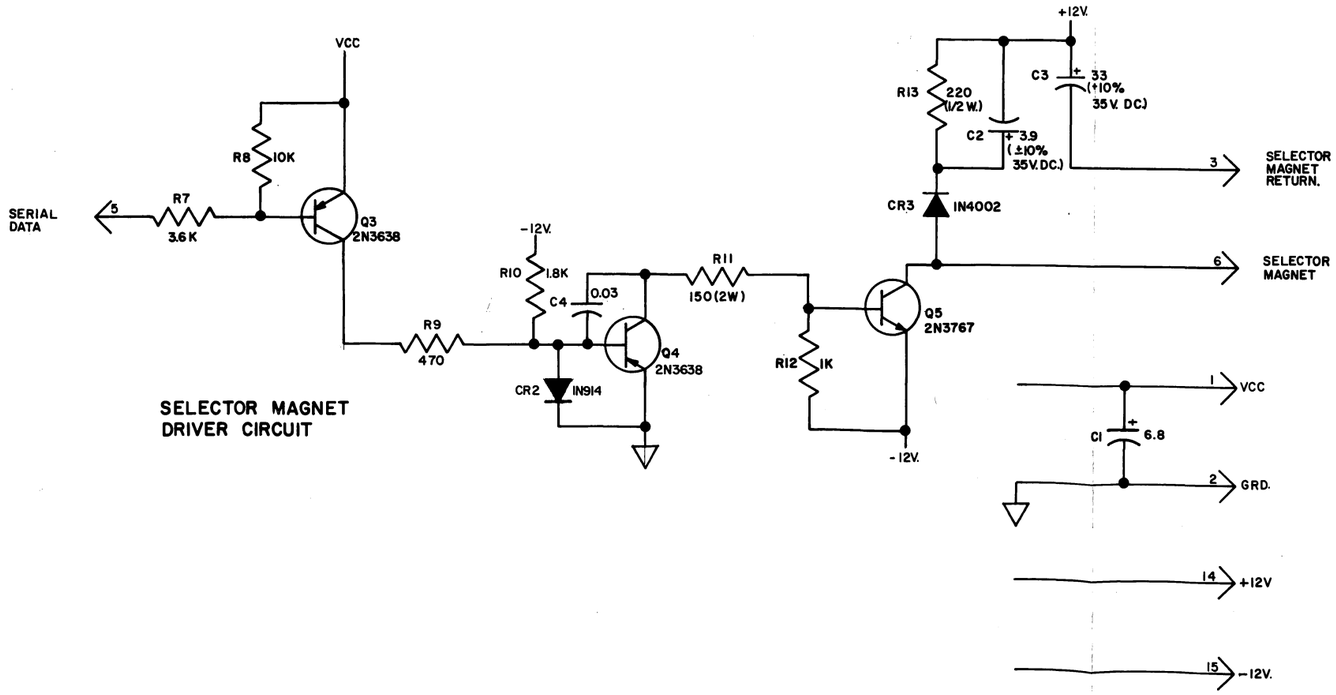
8369WD

TC 404 (5-68)

NO.	NOTES
1.	ALL VOLTAGES DC. UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
5.	INDICATES FEMALE AND INDICATES MALE TERMINAL
6.	REFER TO 303149 FOR ASSEMBLY INFORMATION.
7.	S NUMBER: 61,428 S.
8	REFERENCE CIRCUIT DESCRIPTION: 8370WD-CD.
9.	INDICATES CIRCUIT GROUND.



MOTOR CONTROL CIRCUIT



SELECTOR MAGNET DRIVER CIRCUIT

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8370WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET - 1

SCHEMATIC WIRING DIAGRAM FOR RECEIVING DEVICE

APPROVALS	
D AND R	E OF M
H.P.K	

E-NUMBER	
PROD. NO.	8370 WD.
DATE	2-29-68
P.D. FILE NO.	G-A354AA
DRAWN W.P.B.	CHKD.
ENGD. C.A.Y.	APPD.

TELETYPE CORPORATION

8370WD

TC 456 (2-68)

CIRCUIT DESCRIPTION OF THE RECEIVING DEVICE LOGIC CARD (ASSEMBLY NUMBER 303149)

TABLE OF CONTENTS

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NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF THE RECEIVING DEVICE LOGIC CARD (ASSEMBLY NUMBER 303149)

SECTION I

GENERAL TECHNICAL DATA

1. BASIC FUNCTION

1.1 The 303149 Receiving Device Logic card combines the function of a selector magnet driver and a motor control relay driver.

1.2 Selector Magnet Driver

The selector magnet driver sinks a steady state current of up to 600 ma DC on a MARK input and sinks zero current on a SPACE input. The MARK input is a logic one, and a SPACE input is a logical zero.

1.3 Motor Control

The motor control relay driver is capable of supplying a current of 40 to 60 ma to operate the motor control relay. The relay will be operated on a logic zero input and released on a logic one input.

2. GENERAL TECHNICAL DATA

2.1 Input-Output Data

2.1.1 The Receiving Device Logic card converts the integrated circuit logic levels to current levels appropriate for magnet operation.

A logic one is defined as a voltage level between 5.0 Volts and 6.6 Volts (usually a logic one approximates the integrated circuit supply voltage). A logic one draws no current from the input of the logic element. 202

Signal voltages between circuit ground potential and +0.5 Volts are considered logic zero.

2.2 Input-Output Characteristics

Motor Control

2.2.1 Receive Message/Motor Start Local (Pins 4 and 8)

These two inputs are connected together in a logical or configuration. A logic zero input will energize the associated motor control relay. Input impedance is 3.6K.

2.2.2 Motor Control Relay Magnet (Pin 9)

The associated motor control relay is connected to this output (typical coil resistance 430 ohms). The output impedance is 91 ohms in series with a -12 Volts. The relay driver output is capable of supplying up to 60 ma of current. Relay magnet drop-out is diode suppressed.

Selector Magnet Driver

2.2.3 Send Data (Pin 5)

Under the control of set logic this input is supplied with MARK and SPACE signals corresponding to received data. A logic one signal (MARK) will cause the selector magnet to be energized. A logic zero signal (SPACE) will de-energize the selector magnet. Input and impedance is 3.6K.

2.2.4 Selector Magnet (Pin 6)

The negative end of the selector magnet is connected to this output which will establish a discharge path through a Diode coupled resistor capacitor network. Typical dropout time is approximately 2.50 milliseconds.

2.2.5 Selector Magnet Return (Pin 3)

The positive end of the selector magnet is connected to this output. In series with the selector-coil is a parallel resistor capacitor network which permits maximum current through the coil during SPACE to MARK transitions. Typical MARK hold current is approximately 600 milliamperes. Nominal rise time is 2.25 milliseconds. Typical load supplied is 3.5 ohms 20 millihenries inductance.

2.3 Mechanical Requirements

The motor control amplifier and the selector magnet driver are mounted on a 15-pin circuit board.

2.4 Power Requirements

203

D.C. Supply	Current Required
+5.0V to +5.50V (+5.25V Nom.)	0 to 20 ma
+11.65 to +13.75V (+12.5V Nom.)	0 to 660 ma
-11.13V to -13.88V (-12.5V Nom.)	0 to 660 ma

2.5 Operating Temperature Range

0°C to 70°C (in free air)

2.6 Storage Temperature Range

-40°C to 70°C

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Schematic Drawing - 8370 WD.

1.2 Assembly Drawing - 303149.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 Selector Magnet Driver

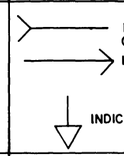
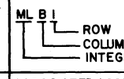
2.1.1 The selector magnet driver circuit is a three stage amplifier, designed to operate full on or off without intermediate levels. The input characteristics are matched to the output of currents sinking DTL integrated circuit elements. The output circuit is matched to the characteristics of the 312936 Selector Magnet Assembly.

2.1.2 A logic one signal input, (See Section I-2.1), will turn the output on, picking up the selector magnet armature. The logic one signal turns off Q3, allowing Q4 and Q5 to be turned on. With Q5 turned on, C3 will be charged through the load impedance to give a high initial current. As C3 becomes charged, load current will be limited by the external 50 ohm, 50 watt resistor connected across C3.

2.1.3 With a logic zero signal on the input, (see Section I-2.1), Q3 will be turned on, driving the base of Q4 positive, turning off Q4 and Q5. The positive voltage on the base of Q4 is limited by ground clamp Diode CR2. With Q5 turned off, the load inductance and C3 will discharge through steering Diode CR3, and the discharge network C2, R13. The impedance values of the output circuit are chosen to provide equal selector magnet armature pickup and drop-out times. The characteristics of the(loaded) output circuit will determine the maximum signalling rate. The values chosen will give proper operation with a nominal pulse length of 6 ms or more. 204

2.2 Motor Control Relay Driver

2.2.1 The motor control relay driver is a two-stage amplifier which is designed to operate full ON or OFF without intermediate levels. This circuit is designed to drive an external motor start relay. Inputs to the motor control relay drive circuit are on Pins 4 and 8. The inputs are connected in a logical OR configuration each having an input resistance of 3.6K. With logic zero, (see Section I-2.1), applied to either input, Q1 is switched ON. This switches Q2 ON, energizing the relay. With logic one applied at both inputs Q1 and Q2 are switched OFF. When Q2 is switched OFF, any positive voltage transient developed by the inductive load will be clamped to the positive supply voltage by CR1.

NO.	NOTES
1.	ALL VOLTAGES DC, UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
4.	
5.	
6.	ASSOCIATED ASSEMBLY: 322059.
7.	S-NUMBER: 61658S
8.	REFERENCE CIRCUIT DESCRIPTION 8371WD-CD.
9.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER THE GATE IS USE AS AN INVERTER.
10.	LOGIC NEGATION: A SMALL CIRCLE JOIN TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
11.	THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE +6V AND 0V, RESPECTIVELY.
12.	VCC. IS PROVIDED TO THE INTEGRATED CIRCUIT PACKAGE ON PIN 14, AND GROUND ON PIN 7. THIS APPLIES TO ALL PACKAGES EXCEPT MLBI.
13.	REFER TO 8399WD FOR TRUTH TABLES.
14.	ABBREVIATIONS: ST - START. SP - STOP. TCL - TIMER CONTROL LATCH. CSL - CHARACTER SAMPLE LATCH. CCL - CONTROL CHARACTER LATCH. OBL - OUTPUT BLIND LATCH. ECL - ESCAPE CHARACTER LATCH. TCS - TIMER CONTROL SET. TC - TAKE CHARACTER. PNC - PRESENT NEXT CHARACTER. FX32 - FREQUENCY X 32 RS(NOT- REGISTER SAMPLE NOT. CP - CLOCK PULSE. SCS - SHIFT CONTROL SAMPLE. CC(NOT) - CONTROL CHARACTER NOT.

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8371WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	3-10-69	19887 R

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 1

SCHEMATIC
WIRING DIAGRAM
FOR
DISTRIBUTOR

APPROVALS

D AND R	E OF M
LDM	

E-NUMBER

PROD. NO. 8371 WD.

DATE 4-24-68

P.D. FILE NO. G-A354AA.

DRAWN W.P.B.	CHKD.
ENGD. A.B.	APPD.

TELETYPE
CORPORATION

8371WD

1

TC 484 (2-68)

SEE SHEET 1 FOR NOTES.

8371 WD

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	3-10-69	19867 R

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

TIMER

F X 32

MLA2 FF

MLA2 FF

MLA1 FF

MLA1 FF

MLE1 FF

MLF1

MLF1

MLD1

MLF1

SCS

R S.(NOT)

CC.(NOT)

MLH2

MLH2

CSL

MLH2

MLH2

MLG3

MLH3

CCL

MLH3

MLG3

MLF2

OBL

R2 100

MLF2

MLF2

MLG3

MLG2

MLG2

TCL

MLG1

MLG2

C13 0.003

MLG1

MLH1

ECL

MLH1

MLH1

TC

TCS

PNC

MLG2

C1 0.003

100 R1

C2 0.003

GRD.

C11 6.8

+6V.

MLB1

MLB1

MLC1

MLC1

MLD1

MLF2

MLF3

MLF3

10-11 BIT CODE (GRD FOR IO)

CP

MLA3 FF SP

MLA3 FF 8

MLB2 FF 7

MLB2 FF 6

MLC2 FF 5

MLC2 FF 4

MLD2 FF 3

MLD2 FF 2

MLE2 FF 1

MLE2 FF ST

MLE1 FF LINE

BLIND

MLB3

MLB3

MLB3

MLB3

MLE3

MLE3

MLE3

MLE3

MLF3

C10 0.1 R10 100

C9 0.1 R9 100

C8 0.1 R8 100

C7 0.1 R7 100

C6 0.1 R6 100

C5 0.1 R5 100

C4 0.1 R4 100

C3 0.1 R3 100

C12 0.003

DATA INPUT 8

DATA INPUT 7

DATA INPUT 6

DATA INPUT 5

DATA INPUT 4

DATA INPUT 3

DATA INPUT 2

DATA INPUT 1

SIGNAL OUTPUT

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D. SHEET 2

SCHEMATIC WIRING DIAGRAM FOR DISTRIBUTOR.

APPROVALS	
D AND R	E OF M
LDM	

E-NUMBER

PROD. NO. 8371 WD

DATE 4-24-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. CHKD.

ENGD. A.B. APPD.

TELETYPE CORPORATION

8371 WD

1

TC 484 (8-68)

CIRCUIT DESCRIPTION OF THE ELECTRONIC TRANSMITTING DISTRIBUTOR (ASSEMBLY NUMBER 322059)

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NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF THE ELECTRONIC TRANSMITTING DISTRIBUTOR (ASSEMBLY NUMBER 322059)

SECTION I

GENERAL TECHNICAL DATA

1. BASIC FUNCTION

1.1 The 322059 Circuit Card Assembly is an Electronic Transmitting Distributor with Control Character Detection. The device converts parallel input signals to serial output signals of either 10 or 11 unit code. The parallel input consists of eight information levels (bits). The serial output consists of a start bit, eight information bits, and one or two stop bits. The telegraphic speed is determined by an external oscillator.

1.2 In addition to the basic data transmitting function of the assembly, several other functions are provided. These functions are:

1.2.1 Responds to a character delete signal (blind), and inhibits transmission of a character.

1.2.2 Recognizes ASCII control characters (6th and 7th level spacing), except ESC and electronically delays the transmission of the next character. The delay interval is a fraction more than a character length, depending upon the character unit code.

1.2.3 Recognizes ASCII control character ESC (11011000) and electronically adds a one character delay after the character following the ESC character.

1.2.4 Provides an output signal which indicates that a character is stored in the register and can be decoded.

1.2.5 Provides an output signal which is used to sample conditions prior to the parallel data input sample.

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1.2.6 Provides an output signal which indicates that another character may be distributed.

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

The inputs to the assembly are all nand type integrated Diode Transistor Logic (DTL) inputs. Each DTL input is approximately a 1.4 ma load to the device sinking current from it. At no time should any of these inputs be more positive than 8 volts or more negative than -.7 volts.

2.1.1 Take Character (TC) (Pin 10)

The TC input controls the start of the distribution cycle. When the input is in the O-state, less than 0.5V, it indicates that a character is available for distribution. Once distribution has commenced, this input will have no further effect until the end of the cycle. This input must be low for at least .25 of a bit before it will be recognized as a legitimate start signal. The device driving the input must be capable of sinking one DTL load.

1

2.1.2 Data Input (Pins 18, 19, 20, 21, 25, 26, 27, 28)

The device driving these inputs must be capable of sinking one DTL load. These inputs will only have effect on the distributor from .5 to .75 of a bit after the TC input first reverts to the low state. At all other times these inputs will not affect the distributor.

2.1.3 Blind Input (Pin 4)

A momentary low on this lead blinds the line to the distribution of the following character. The device driving this input must be capable of sinking four DTL loads. This input should never be allowed to revert to the 0-state except when the PNC output is low. Otherwise, the line would be blinded somewhere in the middle of a character, resulting in an errored character being transmitted. The low on the blind input must be removed before the end of the blinded character to allow the distributor to reset the Output Blind Latch.

2.1.4 Control Character Latch (CC(NOT)Inhibit)(Pin 7)

This input is grounded to disable the control character blind feature (See Paragraph 1.2.2). The device driving this input should be capable of sinking three DTL loads.

2.1.5 Register Condition (TCS)

This input may be grounded in order to clear the register. This may be a requirement in some applications where at times certain characters will not be transmitted. The device driving this input should be capable of sinking three DTL loads.

90 2.1.6 F X 32 (Pin 35)

This input is from an external oscillator. The frequency of the oscillator must be 32 times the desired bit-rate. The device driving this input must be capable of sinking two DTL loads.

2.1.7 10-11 Unit Option (Pin 11)

This input is grounded when the distributor is operating with a 10 unit character code. It is opened or high for 11 unit operation. The device driving this input must be capable of sinking one load.

2.2 Output Characteristics

The outputs from this assembly are all nand type Diode Transistor Logic (DTL) outputs. The outputs will be rated by the number of DTL loads it can sink. Each DTL load is approximately 1.4 ma.

2.2.1 Present Next Character (PNC) (Pin 9)

This circuit is capable of driving eight DTL loads. When the distributor is idle, this output will be 0-state (approximately .3V).

2.2.1 (Continued)

When this output is low, a character may be presented for distribution. It will revert to the 1-state (approximately Vcc) at the beginning of a distributor cycle. It will remain in the 1-state until the character has been distributed, at which time it will revert again to the 0-state.

2.2.2 Serial Data Output (Pin 12)

A mark signal is represented by a 1-state at this output and a space signal by the 0-state. This output sinks up to eight DTL loads.

2.2.3 Control Character Recognition [CC (NOT)] (Pin 2)

This output is the same as the Control Character Latch Inhibit input. This output will change from the 0-state to the 1-state when a control character is recognized, and will remain in the 1-state for a time duration of 1.1 characters. It is capable of sinking six DTL loads.

2.2.4 Clock Pulse (CP) (Pin 3)

The clock pulse output is a timing output. This output reverts to the one state for approximately .12 of a bit, occuring at the trailing edge of each transmitted bit.

2.2.5 Register Sample [RS (NOT)] (Pin 6)

The Register Sample output is approximately .12 bits in duration occuring between .75 to .87 of a bit following the start of the distributor. When this output reverts from its normally low state to the 1-state, it indicates that a character is in storage, and the parallel data outputs of the register may now be sampled. This output is capable of sinking current from seven additional DTL loads.

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2.2.6 Parallel Data Outputs (Pins 14, 17, 29, 31)

When these parallel outputs are in the 1-state it indicates that a mark is stored in the particular position that the given lead is monitoring. These outputs are capable of sinking seven DTL loads.

2.2.7 Parallel Data Outputs (Pins 13, 15, 16, 22, 23, 24, 30, 32)

When these parallel outputs are in the 1-state it indicates that a space is stored in the particular position that the lead is monitoring. Pins 13, 15, 16, 22, 23, and 32 are capable of sinking six DTL loads. Pins 24 and 30 are capable of sinking five DTL loads.

2.2.8 Shift Control Sample (SCS) (Pin 5)

The output of SCS reverts to the 0-state from .25 to .5 of a bit after the start of the distributor. It is a timing signal occuring prior to

2.2.8 (Continued)

the character sample, and may be used to set up characters in external logic prior to the character sample by the distributor.

2.2.9 Stop Output (SP) (Pins 33, 34)

Pin 33 is in the 1-state when a stop bit is set in the SP Flip-Flop. This is a timing signal which may be used by external logic to identify that a character is being distributed. Pin 33 is capable of sinking four DTL loads Pin 34 is capable of sinking five external DTL loads.

2.3 Size

The distributor is a 5-3/4 inch by 4-1/4 inch circuit card which mates with a standard 36 pin circuit card connector.

2.4 Options Available

2.4.1 The distributor may be changed from eleven unit code to ten unit code by grounding Pin 10.

2.4.2 Another option is the electronic insertion of an idle time, one character in duration, following each ASCII control character except control character ESC. This feature may be removed by grounding Pin 7. Grounding Pin 7 also removes the electronic insertion of a character interval for the character following the control character ESC.

2.5 Miscellaneous Requirements

2.5.1 Power Supply Requirement

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VDC	I (ma)
+5V to +6.6V	520 ma (max)

2.5.2 Operating Temperature Range

0°C to 70°C (free air)

2.5.3 Storage Temperature Range

-40°C to +70°C

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly drawing 322059 (MC059) and schematic drawing 8371 WD.

1.2 Logic symbols and truth table 8399 WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 General

2.1 Refer to the timing diagram, flow chart and the schematic 8371 WD to aid in understanding the following discussion.

The flow chart should be used as an outline. When two lines enter a symbol, it is implied that either input causes the function in the symbol to be performed. It is not intended that any of the symbols be construed to represent logic functions. The flow chart is intended to relate circuit operation with respect to time.

2.2 Starting Function

Assume that the distributor is idle, i.e., no character is being distributed. In this state the distributor issues a present next character command (PNC in 0-state) which indicates to external logic that a character may be presented for distribution. The command to begin the distribution cycle is presented on the take character lead. This command (TC in 0-state) releases and controls the timer through MLG3-12.

The TC must remain ON for at least .25 of a bit, after which time the timer is locked on by the timer control latch, TCL, for one distribution cycle. Should TC turn off anytime prior to .25 bit, the timer will be recycled to the 0-count. This time period provides integration to reject noise pulses at the TC input. 93

When the time out reaches .25 of a bit, two gates MLF1-6 and MLF1-12 change to the 0-state. MLF1-6 provides the shift-control sample (SCS) signal at Pin 5, while MLF1-12 sets the timer control latch (TCL). An output from TCL locks the timer on, committing the distributor to a complete character cycle. (As a condition, the take character input must remain on for .75 of a bit to assure that a character is correctly entered into the shift register.)

2.3 Preliminary Events

The shift-control signal (SCS) started at .25 of a bit remains on until .5 bit. This signal is used by keyboard logic to perform a controlling function.

At .5 of a bit gate MLD1-6 changes to the 0-state. This condition causes the character sample latch to set and opens the character input gates MLB3 and MLE3 to accept data signals. A 1-state on any data input level sets a MARK into the corresponding register flip-flop. The sample period lasts for one quarter bit (until .75 of a bit after TC) at which time MLD1 reverts back to the one-state. If TC is removed prematurely i.e., before .75 bit the

2.3 (Continued)

character sample period will be terminated early or may not occur at all. TC may be removed after .75 bit.

Immediately following the character sample period the register sample(RS)pulse is developed. This is a positive going output which appears on Pin 6. This output, lasting .12 bits, indicates to external logic that a character has been stored in the register and may now be sampled. Internally this signal enables the control character detected gate MLG3-6, whose functions will be further discussed in the control character section.

At approximately .87 of a bit, the clock pulse changes to the 1-state, priming the data flip-flops. At exactly 1-bit time (.13 bits later) the clock pulse reverts to the 0-state. At this time each data bit stored in the distributor is shifted one position. Additional clock pulses shift the data to the LINE flip-flop, which becomes the output signal. This continues for nine additional clock pulses, (10 for an 11-unit code), at which time the register will have been cleared (all flip-flops in the space condition). The distribution cycle is now completed.

2.4 Serializing Function

The serializing function is performed by the shift register. It consists of eleven clocked flip-flops, labeled on the schematic as Stop (SP), Start (ST), Line (LINE) and Data Levels 1 through 8. Information is transferred into the shift register on a parallel basis. When the Sp input of any flip-flop reverts to the 0-state, a mark is set in that position of the distributor. Positions SP, ST and LINE are set internally. The elements are cascaded in such a manner that a positive pulse applied to the CP input of the flip-flop will result in each flip-flop assuming the state of the preceding flip-flop when the pulse is removed. Therefore, the shift register performs the function of serializing parallel input signals.

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When the distributor is idle, TCL is used to hold the register in the no character stored state, that is, data positions 1 through 8 and ST are held spacing while SB and LINE are held marking. The result is that a character cannot be set in the register until TCL is set, which occurs .25 of a bit after TC. Data bits are read into the register during the character sample period, .5 to .75 of a bit after TC. A 1-state on any data input during the sample period sets a mark into the corresponding data flip-flop. Likewise a 0-state on any data input for the duration of the sample period holds the corresponding data flip-flop in its cleared state (corresponding data flip-flop remains spacing). When the character sample period has passed, the data input leads have no further effect on the distributor.

One bit time after TC, the first clock pulse occurs. Each data bit in the register is shifted one position. After nine additional clock pulses, (10 for 11 unit code) the entire register will have been cleared to the spacing condition, that is, a space stored in each flip-flop. Register condition gate, MLD1-8, then reverts to the 0-state. MLD1-8 resets the timer control latch, TCL, and the output blind latch, OBL, if it had been previously set. TCL clamps the register and sets a MARK in the SB flip-flop which in turn causes the present next character, PNC, command to be issued. A new cycle may now begin.

2.5 Control Character Operation

Another function of the distributor is to insert a marking interval of approximately one character length after the transmission of each control character. This time period is needed by the typing unit to detect, respond, or perform logic associated with certain control characters prior to the transmission of the next character. This feature may be inhibited by grounding the CC (NOT) lead, Pin 7.

When a control character has been entered in the distributor, its presence is recognized by the control character recognition gate, MLG3-6. This gate has inputs to monitor the registers sixth and seventh level for a spacing condition and a lead to monitor the register sample time. After the data has been loaded into the register (.5 to .75 bit after TC), the register sample lead, RS, reverts to the one-state (from .75 to .87 bit after TC). Therefore, for all control characters the control character recognition gate sets the control character latch, CCL.

The control character is then transmitted as any other character. After the control character has cleared the register, the register condition gate MLD1-8 resets the timer control latch, TCL. At this time the output blind latch, OBL, is set via gate MLG3-8, for all control characters except ESCAPE (ESC), which will be discussed later. The output blind latch keeps the signal output at Pin 12 in a MARK state. The control character latch, set previously, inhibits the present next character (PNC), output and provides the input required to cycle the distributor for another character interval. After the register is empty (the stop bit has moved through the register), the TCL and OBL are reset by the register condition gate MLD1-8.

When operating in 10 unit code the detection of a control character causes the distributor to shift into the 11 unit code for the control and delay character. This adds two bit intervals to the control character-delay character length. When in 10 or 11 unit code, an additional interval, approximately .87 bit, is provided by gate MLF2-3. These added time intervals are necessary to insure that all typing unit responses are completed before another character is transmitted.

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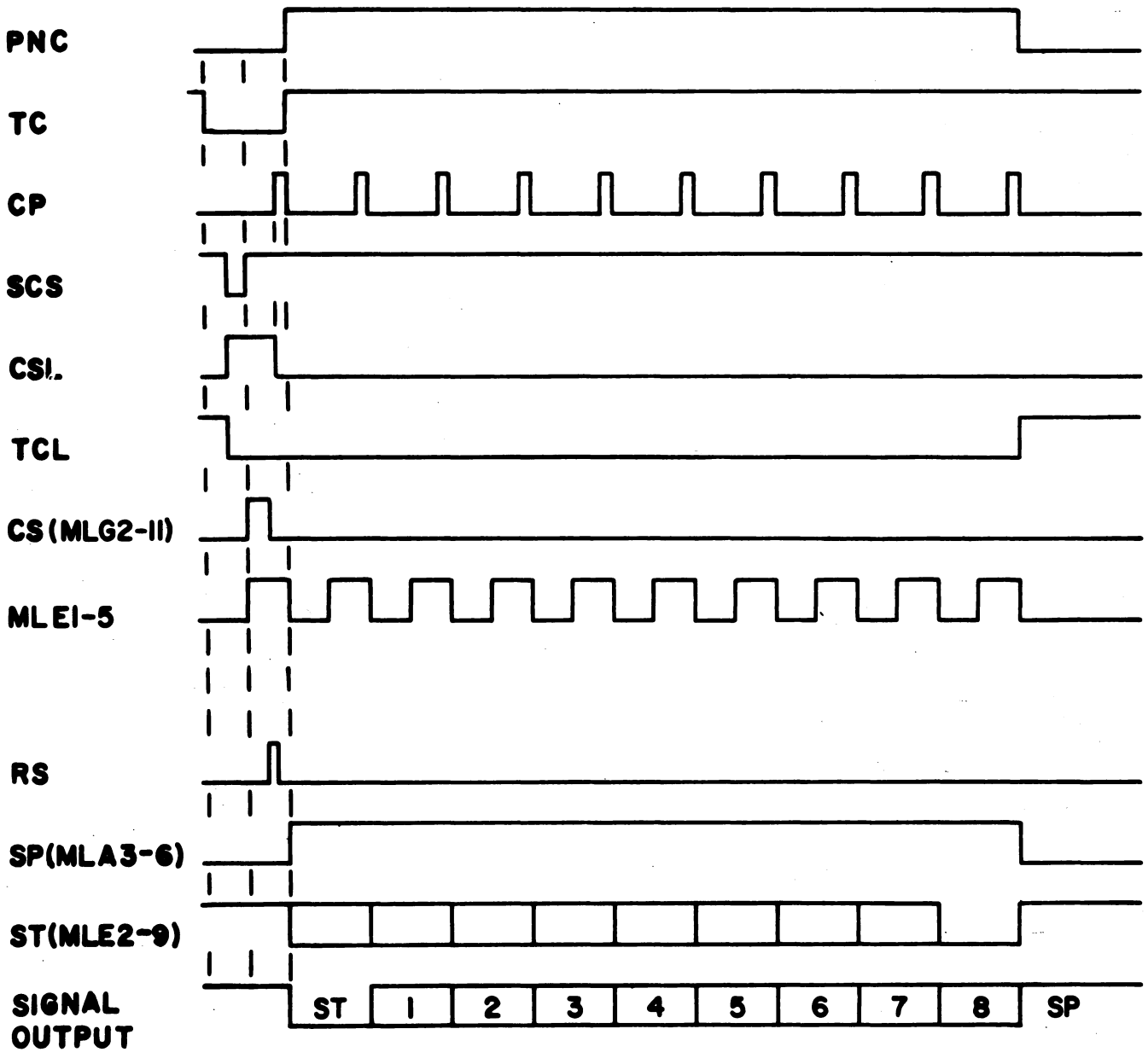
2.6 ESCAPE Character Operation

Another function of the distributor is to insert a marking interval of approximately one character length after the transmission of the character following the control character ESC. No delay is provided after the ESC character. The control character ESCAPE in itself performs no function in the typing unit. The character following ESCAPE is used by the typing unit to perform a function. The delay, therefore, is added after this two character ESCAPE sequence to allow the typing unit to complete its control function before transmission of the next character. This feature may also be inhibited by grounding the CC (NOT) lead, Pin 7.

2.6 (Continued)

An escape character is detected in the escape recognition gate MLC1-6 and MLC1-8 which in turn sets the escape character latch, ECL. ECL inhibits the operation of the output blind latch, OBL, and allows the present next character, PNC, to be issued immediately after the control character ESCAPE has been transmitted. The control character latch CCL, however, remains set. A character other than ESCAPE resets ECL which in turn removes the inhibit from gate MLG3-8. The distributor now operates as if a control character had been detected.

DISTRIBUTOR TIMING DIAGRAM



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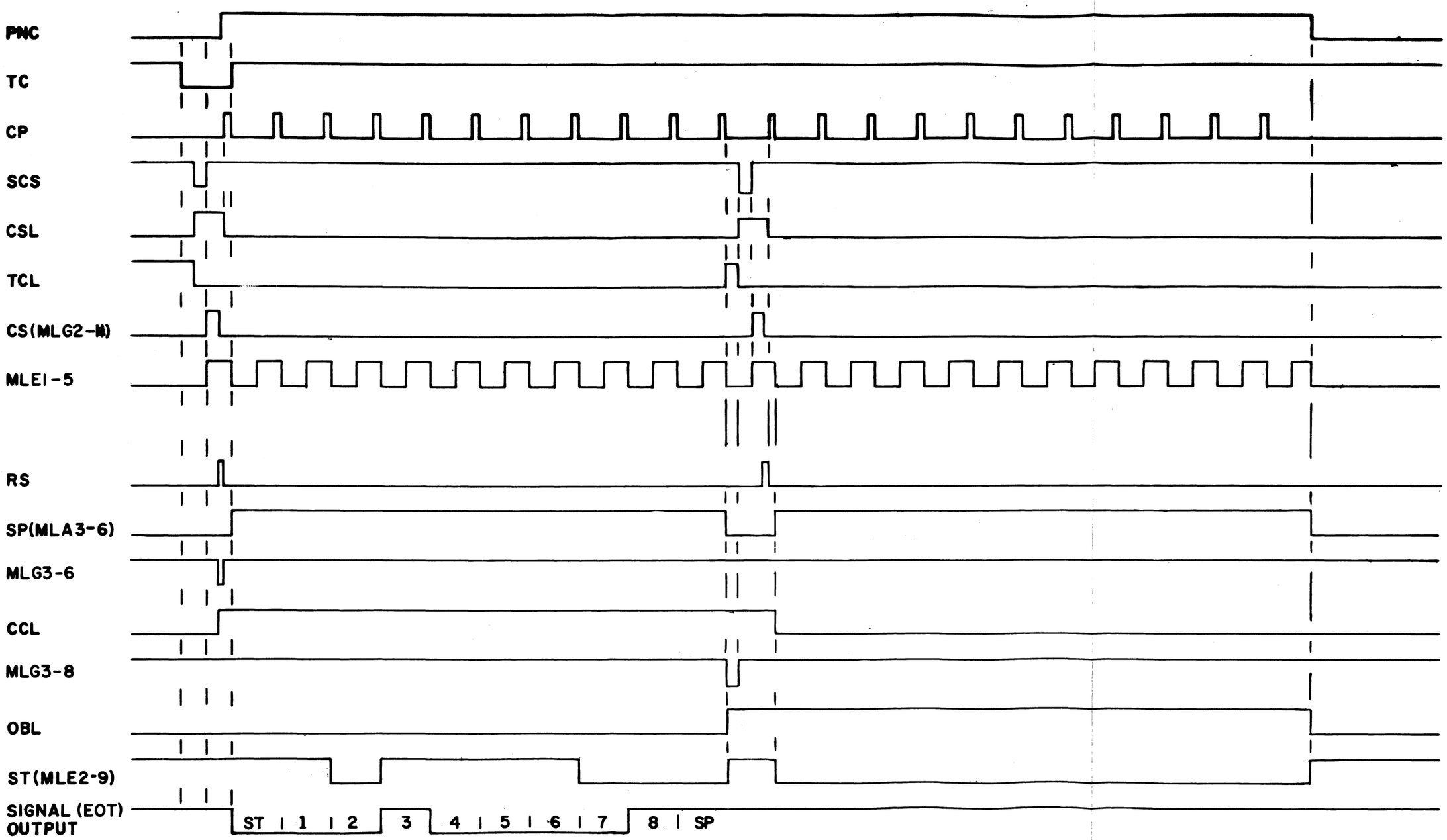
NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

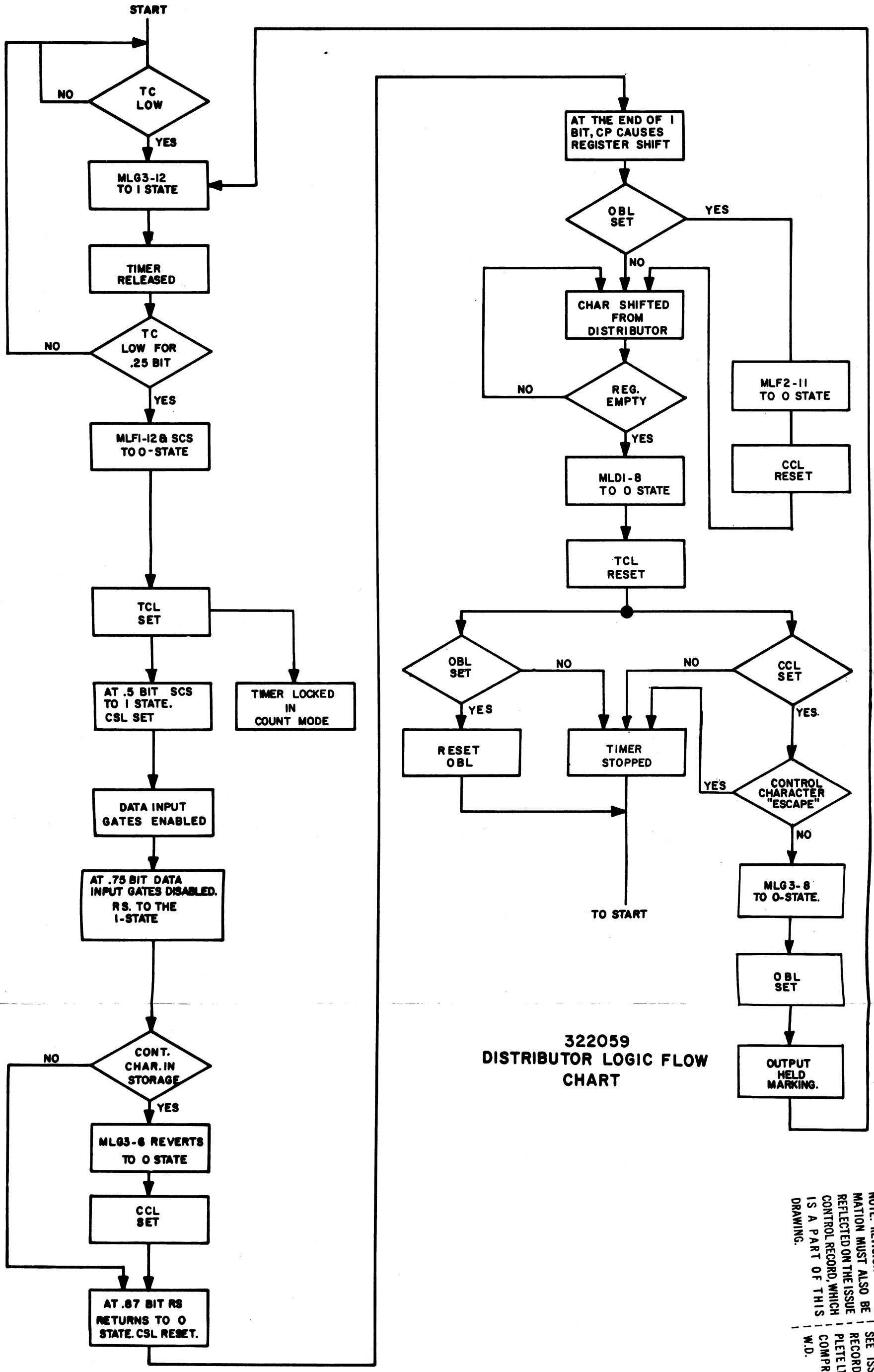
SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

DISTRIBUTOR TIMING DIAGRAM FOR CONTROL CHARACTERS (ESCAPE EXCLUDED)



NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.



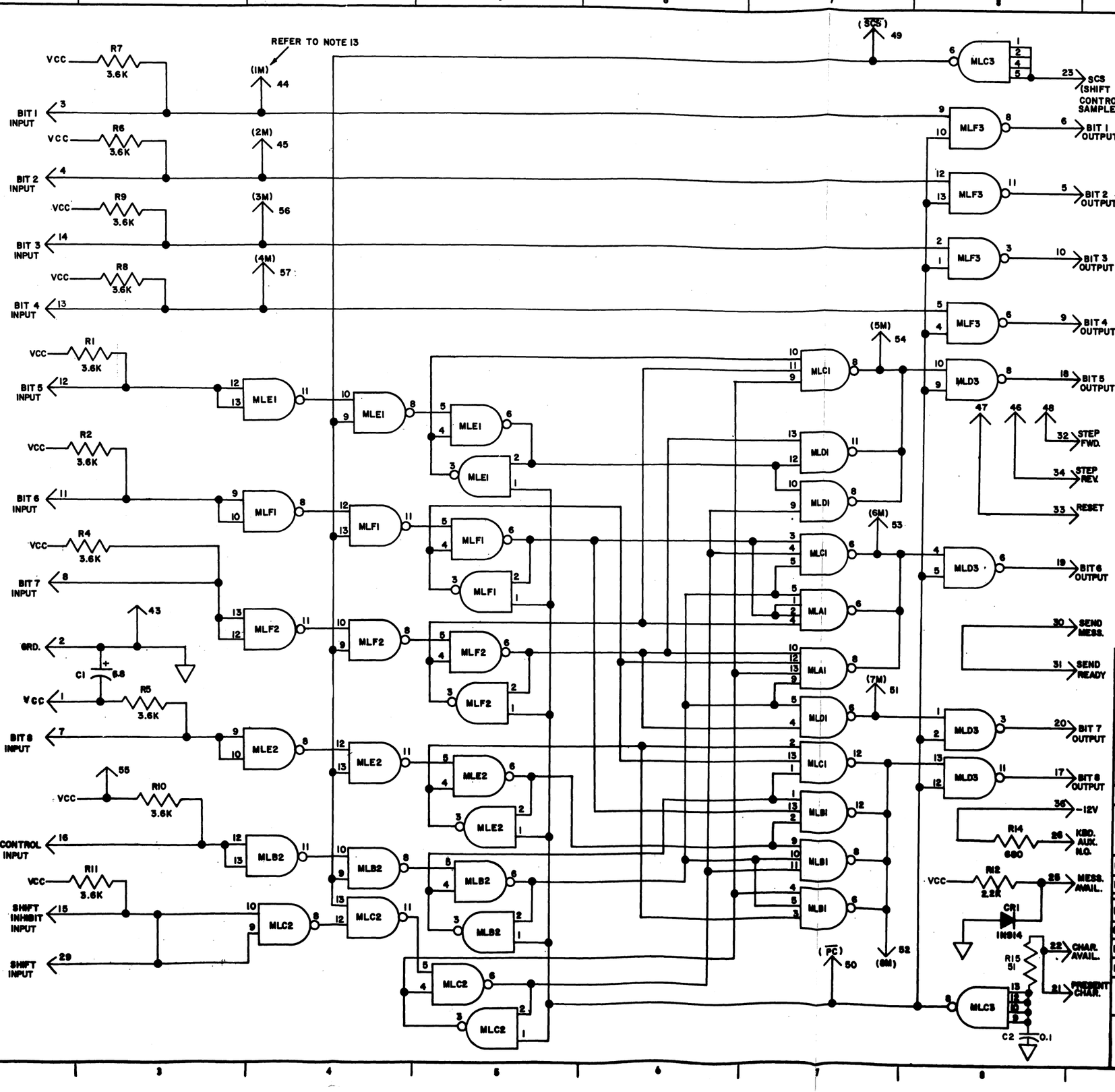
322059
DISTRIBUTOR LOGIC FLOW CHART

CIRCUIT DESCRIPTION
8371 WD-CD-11

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

NO.	NOTES
1.	ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTORS 1/4W AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
4.	INDICATES FEMALE TERMINAL AND INDICATES MALE TERMINAL
5.	REFER TO 322044 FOR ASSEMBLY INFORMATION.
6.	S NUMBER 61,430S.
7.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD: ML A 2 — ROW, COLUMN, INTEGRATED CIRCUIT
8.	THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC AND 0V, RESPECTIVELY.
9.	LOGIC NEGATION-A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
10.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER, THE GATE IS USED AS AN INVERTER.
11.	VCC IS PROVIDED TO THE INTEGRATED CIRCUIT PACKAGE ON PIN 14 AND GROUND ON PIN 7.
12.	REFER TO 8399WD FOR TRUTH TABLES.
13.	PIN CONNECTIONS 37 TO 57 REFER TO PIGGYBACK TERMINALS ON CIRCUIT CARD.
14.	REFERENCE CIRCUIT DESCRIPTION 8374 WD-CD.
15.	INDICATES CIRCUIT GROUND.



8374WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET-1

SCHEMATIC WIRING DIAGRAM FOR KEYBOARD CONTROL

APPROVALS

D AND R	E OF M

E-NUMBER

PROD. NO. 8374WD

DATE 4-10-68

R.D. FILE NO. 6-A364AA

DRAWN RJP | CHKD.

ENGR. CAY | APPD.

TELETYPE CORPORATION

8374WD

CIRCUIT DESCRIPTION OF KEYBOARD CONTROL LOGIC
(ASSEMBLY NUMBER 322044)

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NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF KEYBOARD CONTROL LOGIC (ASSEMBLY NUMBER 322044)

SECTION I

1. BASIC FUNCTION

1.1 The 322044 Circuit Card Assembly used in the Model 37 Service Unit converts the keyboard parallel input information levels (bits) to eight parallel output information levels (bits) representing USASCII characters. The card is capable of generating 128 distinct characters. These include 95 graphic characters, 32 control characters, and the delete character.

1.1.1 Provisions are made for "piggy back" mounting of the "Character Counter" Logic Card (322045) for specific ASR applications.

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

The inputs to the assembly are obtained from the keyboard contacts referenced to circuit ground. Each DTL input is a nominal 3.2 ma load on the signal source or contact.

2.1.1 Data Input (Pins 3,4,14,13,12,11,8,7)

The data inputs, bits 1 through 8, consist of MARKS or SPACES. The input logic levels are defined by using negative logic. That is, a MARK is a logic voltage level between circuit ground and +0.5 volts (low). A SPACE is a logic voltage level between +5.0 volts and +6.6 volts (high).

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The KEYBOARD CONTROL, SHIFT INHIBIT, and SHIFT inputs are defined by using negative logic. A closed contact is referenced to circuit ground and is considered a logic one. An open contact is referred to the nominal 5.25 volt supply through a 3.6K ohm pull-up resistor and is considered a logic zero.

2.1.2 Keyboard Control (Pin 16)

The device driving this input must be capable of sinking 2 DTL loads (1 DTL load = 1.4 ma). This input is normally "low" except when generating control characters on keys which can perform other functions (EOT, ENQ).

2.1.3 Shift Inhibit (Pin 15)

The device driving this input must be capable of sinking 2 DTL loads. This input is normally high except when generating control characters on keys which can perform no other function and characters which are not affected by shift to upper case.

2.1.4 Shift (Pin 29)

The device driving this input must be capable of sinking 2 DTL loads. This input is low when generating the lower case keyboard characters, high when generating upper case characters, and high or low when generating control characters.

2.1.5 Present Character (Pin 21)

The device driving this input must be capable of sinking 1 DTL load. This input is normally "high" when the machine is idle and goes "low" for 1 bit time when a character is generated.

2.1.6 Shift Control Sample (Pin 23)

The device driving this input must be capable of sinking 1 DTL load. This input is normally high when the machine is idle and goes "low" .25 bit after PC and remains low for .25 bit.

2.1.7 Message Available (Pin 25)

A KEYBOARD AUX. closure connects Pins 25 and 26. This action generates a "MESSAGE AVAILABLE" signal which is sensed by the SEND CONTROL.

2.1.8 Keyboard Aux. N.O. (Pin 26)

The KEYBOARD AUX. normally open contact closes when a character is generated and is high at all other times. This contact closure initiates the movement of data from the card input to card output.

2.2 Output Characteristics

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The outputs from this assembly are all Diode-Transistor Logic (DTL) type outputs. Output current sinking and fan out capability can be determined from the Manufacturers Specifications.

2.2.1 Data Output (Pins 6,5,10,9,18,19,20,17)

These outputs are capable of sinking approximately 16 ma each. The data output pins will be"high" (MARK) when Pin 21 is "high" and will be "high" (MARK) or "low" (SPACE) when Pin 21 and 23 are low, depending upon the character generated.

2.3 Character Counter Inputs

The 322045 Character Counter, when used, obtains its data inputs (bits 1 through 8) from those pins suffixed with an "M" (see schematic 8874 WD).

The Character Counter outputs STEP FORWARD, STEP REVERSE and RESET, enter the Keyboard Control Logic card on Pins 48, 46 and 47 respectively,

and leave via Pins 32, 34 and 33 respectively. For further information refer to schematics 8374 WD, 8375 WD and 8380 WD.

2.4 Mechanical Requirements

The 322044 Card Assembly is a standard 5-3/4 inch by 4-1/4 inch 36-pin circuit card which is inserted into a 36-pin edge card connector.

2.5 Power Supply Requirement

Vcc (DC)	Current (ma) Max.
+5.0 Volts to +6.6 Volts	175 ma
* -11.13 Volts to -13.88 Volts (12.5V Nom.)	20 ma

* Not required for card tests, but required for operation in Model 37.

2.6 Temperature Range

The operating temperature range is from 0°C to 70°C in free air. The storage temperature range is from -40°C to +70°C.

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly and Schematic drawing 322044(MC044)and 8374 WD, respectively.

1.2 Logic symbols and truth tables 8399 WD.

1.3 8375 WD and 8380 WD (Character Counter).

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 General

Refer to the 8374 WD schematic, attached timing diagrams, and USASCII Code Chart as an aid in the following discussion.

Timing Diagram 1 is representative of the timing MARK-SPACE sequence involved in getting a data bit to the Model 37 electronic distributor for a lower case "a". Timing Diagram 2 shows the general timing sequence for any USASCII character generated. Timing Diagram 3 shows the general timing sequence for proper card operation.

2.2 Operating Sequence

When the keyboard is idle, bits one through eight are marking. Assume that the lower case "a" bit sequence has just been keyboard generated. The chart below shows the logic input states. (Refer to USASCII code chart).

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INPUT DATA BIT	PIN NUMBER	*BIT LEVEL
b1	3	MARK
b2	4	SPACE
b3	14	SPACE
b4	13	SPACE
b5	12	SPACE
b6	11	MARK
b7	8	MARK
b8	7	MARK

FUNCTION	PIN NUMBER	*LOGIC LEVEL
CONTROL	16	1
SHIFT	29	1

* Logic Level 1 = Bit Level Mark = Circuit Ground

Logic Level 0 = Bit Level Space = Supply Voltage (Vcc)

Output data bits one through four (Pins 6, 5, 10, 9) are still "MARKING" because the associated output gates have not been enabled by the "PRESENT CHARACTER" (PC) gate signal. Effectively, input data bits 1 through 4 are waiting at the input of their respective output gate (MLF3-9, MLF3-12, MLF3-2, MLF3-5) for the gate signal which allows them to appear at the output.

Output data bits 5 through 8 are still "MARKING" because the associated output gates have not been enabled by the PC signal. Input data bits five through eight are at their respective latch driver inputs (MLE1-10, MLF1-12, MLF2-10, MLE2-12) waiting for the "SHIFT CONTROL SAMPLE" (SCS) gate signal.

The CONTROL, SHIFT INHIBIT, and SHIFT signals are waiting at their respective latch driver inputs for the SCS gate signal.

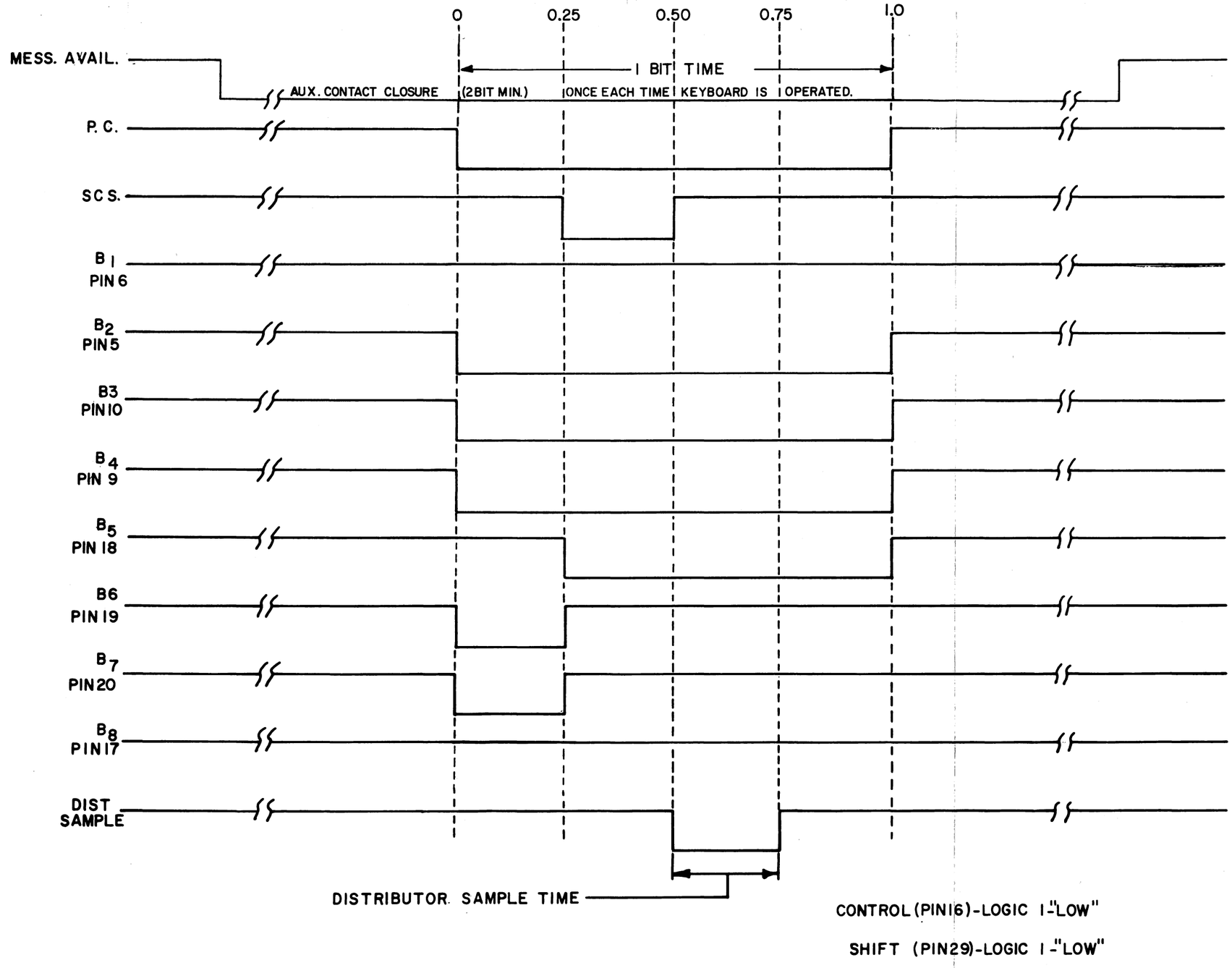
KEYBOARD AUX. N.O. contact closes when a bit sequence is generated. This action connects Pin 26 to Pin 25. With Pin 25 "low", a PRESENT CHARACTER gate signal is generated by the send control card. This signal causes MLC3-8 to go "high" and gate bits 1 through 4 to the output pins. Bit 1 is "MARKING". Bits 2, 3 and 4 are "SPACING". The PC input (Pin 21) remains "low" for one bit time. This action primes the bit latches for SCS input. The SCS input goes "low" .25 bit after PC and remains "low" for .25 bit. The latch drivers are enabled and bits 4 through 8 appear at the output. Bit 5 is "SPACING". Bits 6, 7 and 8 are marking. Bits 1 through 8 have been transmitted to the card outputs and can be entered into the electronic distributor shift register. At .5 bit time the distributor samples the output data bits and enters the data bits into the shift register. 164

The chart below shows the state of the output data bits just prior to distributor sampling.

OUTPUT DATA BIT	PIN NUMBER	*BIT LEVEL
b1	6	MARK
b2	5	SPACE
b3	10	SPACE
b4	9	SPACE
b5	18	SPACE
b6	19	MARK
b7	20	MARK
b8	17	MARK

* MARK = Logic 1 = Supply Voltage (Vcc)
* SPACE = Logic 0 = 0 - +0.5 Volts

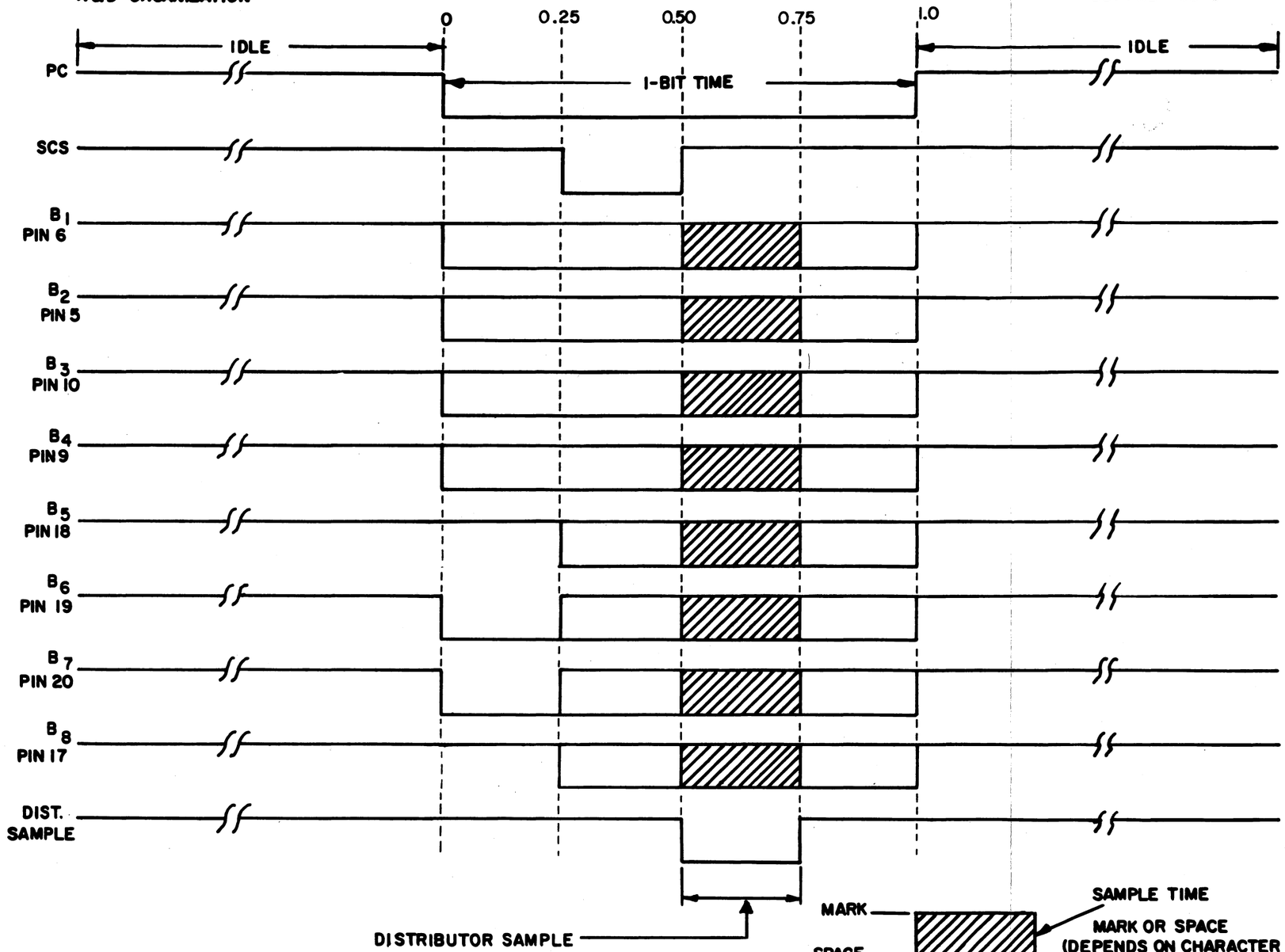
At 1 bit time, the PC and MESSAGE AVAILABLE inputs go "high". This action resets the outputs of bit latches 5 through 8 (MLE1-6, MLF1-6, MLF2-6, MLE2-6) "low". MLB2-6 and MLC2-6 are also reset to the "low" state. MLF3-10, MLF3-13, MLF3-1, MLF3-4, MLD3-9, MLD3-5, MLD3-2, MLD3-12 are brought "low" by a "high" PC input. Bits 1 through 8 are all marking and the logic is idle.



MODEL 37 TIMING DIAGRAM-1
(LOWER CASE "a" CHARACTER GENERATION)

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.



* CONTROL (PIN 16)-LOGIC 1 OR 0-"LOW" OR "HIGH"

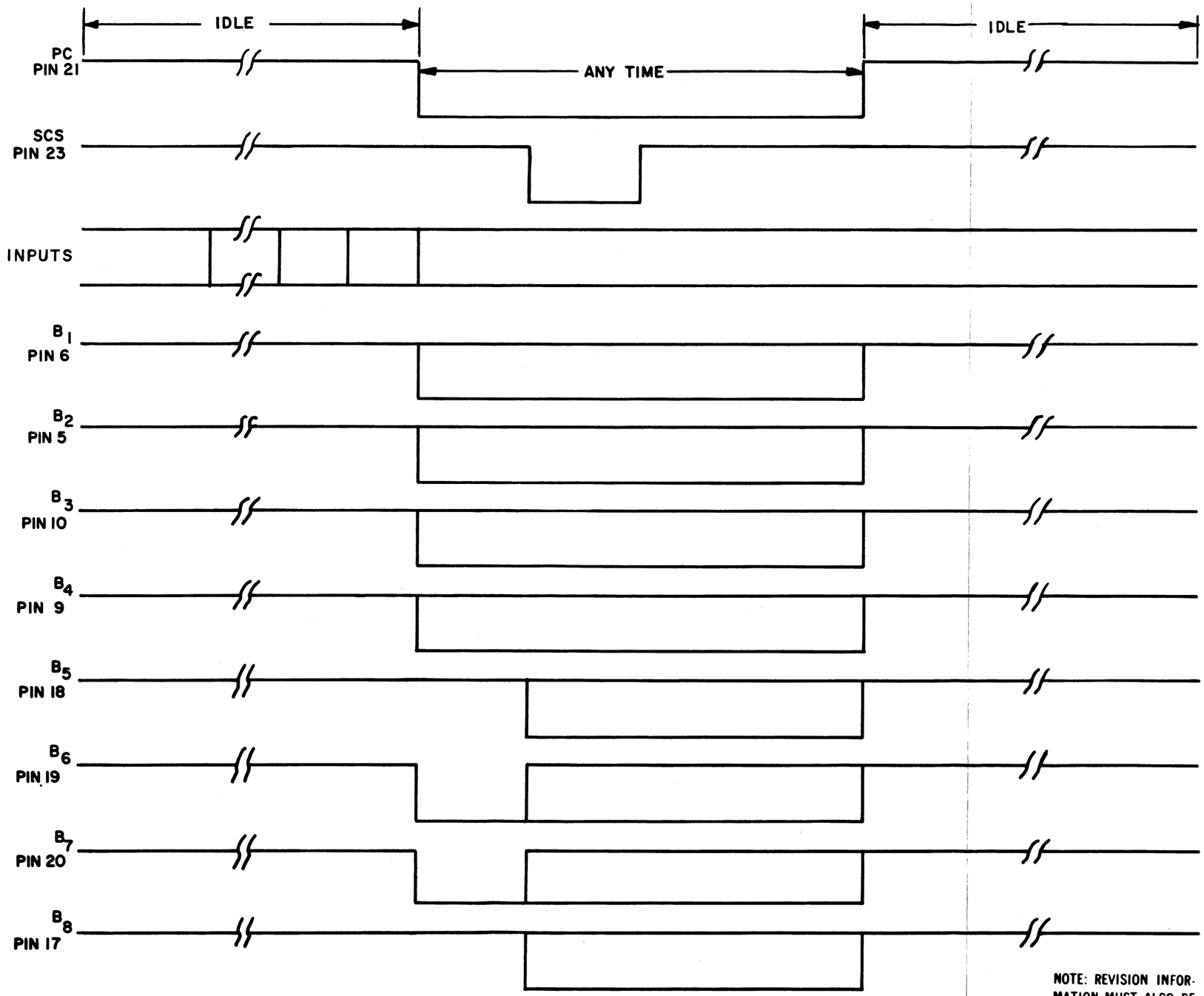
* SHIFT (PIN 29)-LOGIC 1 OR 0-"LOW" OR "HIGH"
* (DEPENDS UPON CHARACTER GENERATED)

MODEL 37
GENERAL TIMING DIAGRAM-2

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

1

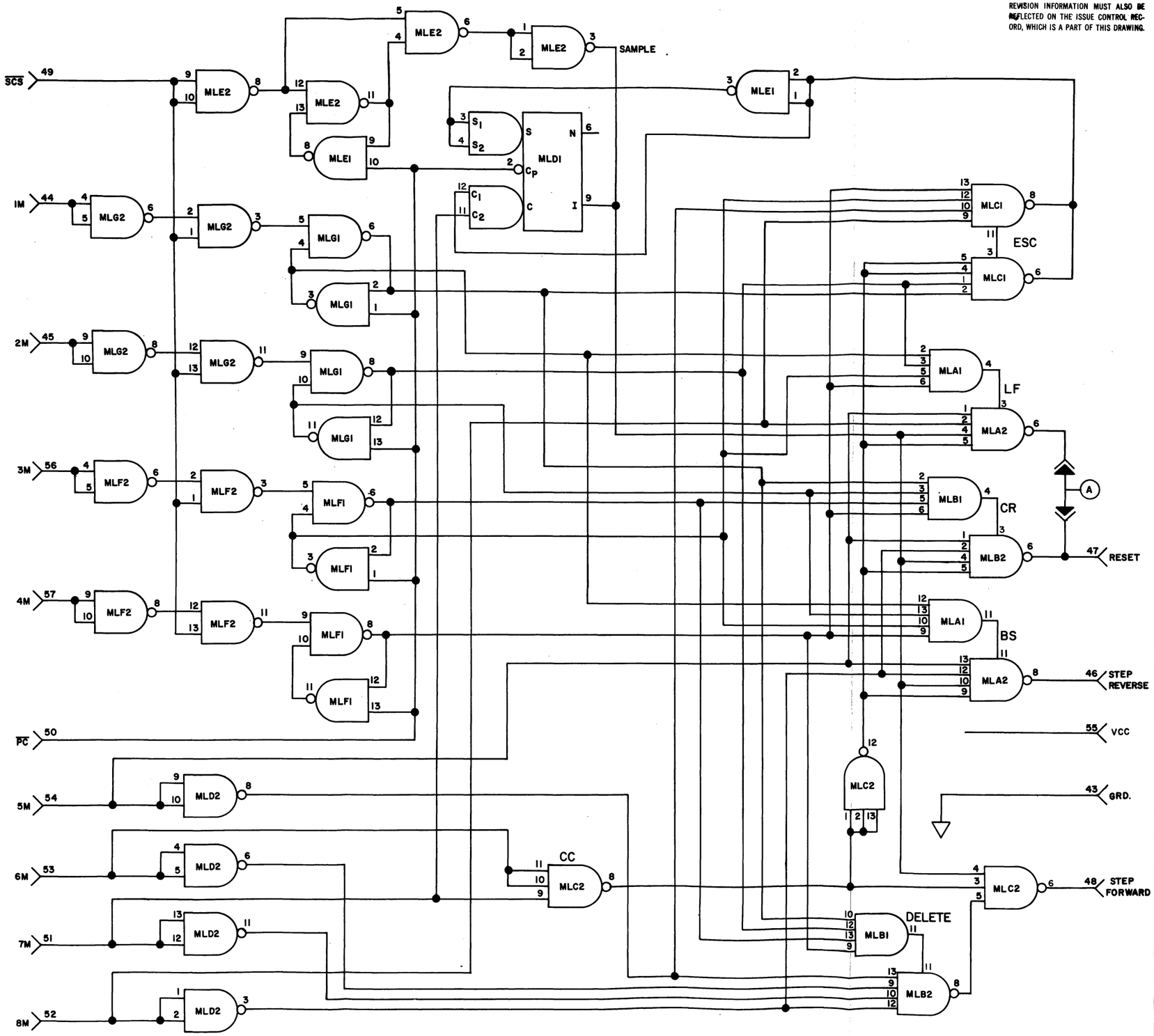


GENERAL TIMING DIAGRAM - 3

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

NO.	NOTES
1.	ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTORS 1/4 WATT AND RESISTANCE IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
4.	INDICATES FEMALE TERMINAL AND INDICATES MALE TERMINAL
5.	REFER TO 322045 FOR ASSEMBLY INFORMATION.
6.	S NUMBER: 61,508 S.
7.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD: ML A 2 — ROW, COLUMN, INTEGRATED CIRCUIT
8.	THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC AND 0V RESPECTIVELY.
9.	LOGIC NEGATION-A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
10.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER, THE GATE IS USED AS AN INVERTER.
11.	VCC IS PROVIDED TO THE INTEGRATED CIRCUIT PACKAGE ON PIN 14 AND GROUND ON PIN 7, THIS APPLIES TO ALL PACKAGES.
12.	REFER TO 8399WD FOR TRUTH TABLES.
13.	OPTIONS A - RESET ON LINE FEED OR CARRIAGE RETURN. STRAP MUST BE ADDED.
14.	REFERENCE CIRCUIT DESCRIPTION 8375 WD-CD
15.	ABBREVIATIONS USED. BS - BACKSPACE. CC - CONTROL CHARACTERS. CR - CARRIAGE RETURN. DELETE - DELETE. ECS - ESCAPE. LF - LINE FEED.
16.	INDICATES CIRCUIT GROUND.



NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8375WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET-1

SCHEMATIC WIRING DIAGRAM FOR CHARACTER COUNTER

APPROVALS

D AND R	E OF M
HK	

E-NUMBER

PROD. NO. 8375WD

DATE 4-26-68

P.D. FILE NO. G-A354AA

DRAWN RJP	CHKD.
ENGD. CAY	APPD.

TELETYPE CORPORATION

8375WD

TC 484 (5-69)

CIRCUIT DESCRIPTION OF THE CHARACTER COUNTER CARD (ASSEMBLY NUMBER 322045)

TABLE OF CONTENTS

CIRCUIT DESCRIPTION OF THE CHARACTER COUNTER CARD (ASSEMBLY NUMBER 322045)

SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

The 322045 Character Counter Card controls the binary counting circuitry of the 322055 Counter Control Card. The parallel inputs consist of eight information levels (bits) obtained from the Keyboard Control Card (322044). The outputs provide up-count, down-count, and reset counter control signals for the Counter Control Card.

1.1 The 322045 Character Counter Card may be used in conjunction with the 322044 Keyboard Control Card. The Character Counter Card is an option and is required if keyboard generated printed characters and spaces are to be counted.

1.2 With Strap A installed, the counting circuits on the Counter Control Card are reset when the NEW LINE (Line Feed character) key is depressed. Strap A is installed if the keyboard is equipped with the NEW LINE feature and the receiving on-line printer is equipped with the NEW LINE feature.

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

The 322045 Character Counter, when used, obtains its data inputs (bits 1 through 8) from those pins suffixed with an "M" (see Schematic 8874 WD). The inputs to this assembly are all integrated Diode Transistor (DTL) type inputs. Each DTL input is approximately a 1.4 ma load to the device sinking current from it. At no time should any of these inputs be more positive than +8 volts or more negative than -0.7 volts.

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A MARK input is considered a logical zero (low), a voltage level between 0 volts and +0.5 volts, and is represented by a closed keyboard contact. A SPACE input is considered a logical one (high), a voltage level between +5.0 volts and +6.6 volts, and is represented by an open keyboard contact.

2.1.1 Shift Control Sample Not ($\overline{SCS}$) (Pin 49)

The SHIFT CONTROL SAMPLE NOT input switches to a high state from .25 to .5 of a bit after the start of a character distribution cycle. At .5 bit, this input reverts to its normal low state until .25 bit of the next character distribution cycle. The source driving this input must be capable of sinking 5 DTL loads.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

2.1.2 Data Inputs (Pins 44, 45, 56, 57)

The data bits consist of MARKS or SPACES obtained from the Keyboard Control Card (See 8874 WD). Input logic levels are defined in Section I-2.1. Each data input represents one DTL load.

2.1.3 Data Input (Pin 54)

Refer to Section I-2.1.2.

This data input represents 4 DTL loads.

2.1.4 Data Input (Pin 53)

Refer to Section I-2.1.2.

This data input represents two DTL loads.

2.1.5 Data Inputs (Pin 51, 52)

Refer to Section I-2.1.2.

A. This data input represents a DTL loads.
B. This data represents three DTL loads.

2.1.6 Present Character Not ($\overline{PC}$) (Pin 50)

When the keyboard is idle, this input is low. It reverts to a high state at the start of a character distribution cycle and remains high for one bit, at which time it reverts to its normal low state. The device driving this input must be capable of sinking 5 DTL loads.

3. Output Characteristics

The Character Counter outputs STEP FORWARD, STEP REVERSE, and RESET, enter the Keyboard Control Card on Pins 48, 46 and 47 respectively, and leave via Pins 32, 34, and 33 respectively. For further information refer to Schematics 8374 WD, 8375 WD, and 8380 WD.

The outputs from this assembly are all Diode Transistor Logic (DTL) type outputs. Output current capability can be determined from the manufacturers specification.

3.1 Reset (Pin 47)

If Strap A is installed, and a CARRIAGE RETURN or NEW LINE character is generated, the RESET output will go low for approximately .5 bit after the SHIFT CONTROL SAMPLE NOT input goes low. Pin 47 is routed off the card to the Character Counter Control which recognizes a low state as a counter RESET signal. This output is high at all times except when a NEW LINE (Line Feed character) or CARRIAGE RETURN character is detected. If Strap A is removed, the RESET output will go low when a CARRIAGE RETURN is detected and remain high at all other times. Current sinking capability is limited to approximately 36 ma.

3.2 Step Reverse (Pin 46)

The STEP REVERSE output is high at all times except when a BACKSPACE is detected at which time it goes low for .5 bit after the SHIFT CONTROL SAMPLE NOT input goes low. Pin 46 is routed off the card to the Character Counter Control which recognizes a low state as a down count signal. The counting circuitry down counts by one each time STEP REVERSE goes low. The current sinking capability of this output is approximately 36 ma.

3.3 Step Forward (Pin 48)

The STEP FORWARD output is normally high and goes low for .5 bit each time a SPACE or printed character is detected. Pin 48 is routed off the card to the Character Counter Control which recognizes a low state as an up-count signal. Each up-count adds one to the contents of the counting circuitry. A STEP FORWARD output (low) is inhibited by DELETE and CONTROL CHARACTERS. When using the Control Character Code Extension, ESC, in a two or three character sequence, Pin 48 will remain high until SHIFT CONTROL SAMPLE NOT goes low during the next printed character distribution cycle. Current sinking capability is limited to approximately 12 ma.

4. MECHANICAL REQUIREMENTS

The 322045 Card Assembly is $3\frac{1}{2}$ inch by 5 inch printed circuit card which is mounted in a "piggy back" fashion on the Keyboard Control Card.

5. POWER SUPPLY REQUIREMENTS

Vcc (DC)	Current (ma) Max.
+5.0 Volts to +6.6 Volts	100 ma

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6. TEMPERATURE RANGE

The operating temperature range is from $0^{\circ}C$ to $+70^{\circ}C$ in free air. The storage temperature range is from $-40^{\circ}C$ to $+70^{\circ}C$.

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly and Schematic drawing 322045 (MC045) and 8375 WD, respectively.

1.2 8374 WD and 8380 WD (Keyboard Control and Character Counter Control Schematics, respectively).

1.3 Logic symbols and truth tables 8399 WD.

2. GENERAL

Refer to 8375 WD and 8374 WD, schematics, enclosed timing diagrams and USASCII Code Chart as an aid in the following discussion.

2.1 Definitions

A. ESC - First character of a Control Character Code Extension sequence. The on-line terminal recognizes ESC as the beginning of a terminal control function (horizontal tab set, full duplex, etc.).

B. FINAL - Last character of a Control Character Code Extension sequence. The on-line terminal performs the control function upon receiving the FINAL character. The FINAL Character also indicates the end of the code extension sequence.

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3. DETAILED DESCRIPTION AND THEORY OF OPERATION

The data inputs (bits 1 through 8), PRESENT CHARACTER NOT, and SHIFT CONTROL SAMPLE NOT signals are obtained from the 322044 Keyboard Control Card. A low input voltage level is associated with a MARK data output and a high input voltage level is associated with a SPACE data output (see USASCII code chart). At the end of each character distribution cycle PC goes low providing a clock pulse for MLD1 (a clocked flip-flop) and a reset pulse for the data bit and SCS latches. MLE2-11, MLG1-6, MLG1-8, MLF1-6 and MLF1-8 revert to the low state when PC goes low. SCS goes high .25 bit into the character distribution cycle, sets the data bit latches and SCS latch to the proper state. At .5 bits SCS reverts to its low state. SAMPLE pulse time occurs between .5 bit and the end of the character distribution cycle. Between .5 bit and 1.0 bit, the logic level of the SAMPLE signal is determined by MLD1-9.

The 322045 assembly inhibits a count for two characters. An up-count resumes on the third keyboard generated character provided it is a printed character or space.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

A new Character Counter assembly capable of inhibiting a count on INTERMEDIATE (Column 2) characters and FINAL (Columns 3,4,5,6 and 7) characters will be produced in the future.

This new card will comply with the latest USASCII doctrine concerning Control Character Code Extension.

Refer to Timing Diagram 2 during the following discussion. A printed character has just been distributed and $\overline{PC}$ reverts to its low state. This negative transition attempts to set MLD1-9 to a high state, but the SAMPLE signal is held low by MLE2-3. Assume the next character generated is any printed character or space. At the start of the distribution cycle $\overline{PC}$ goes high, thus priming the data bit latches and $\overline{SCS}$ latch for the SCS signal. At .25 bit, SCS goes high and gates bits 1 through 8 to the inputs of the counter output control gates (ESC, LF, CR, BS, CC, DELETE). MLC1 inputs monitor all eight data bits. The character generated was not ESC, therefore MLC1-8 and MLD1-C1 remain high and MLD1-S1 remains low. Between .25 bit and .5 bit, MLE2-3 will always be low regardless of the character generated. At .5 bit SCS reverts to its low state and remains low until .25 bit of the next distribution cycle. A low to high transition occurs at .5 bit producing a sample pulse for the duration of the distribution cycle. Counter control gates LF and CR monitor the eight data bits. A LINE FEED (New Line) or CARRIAGE RETURN Character was not generated, therefore MLA2-6 and MLB2-6 remain high. No RESET signal is sent to the counting circuitry. A BACKSPACE character was not generated, therefore MLA2-8 remains high and no STEP REVERSE signal is generated. The character generated was neither a Control character nor a DELETE Character, therefore MLC2-8 and MLB2-8 are high. The high on MLD1-9 causes MLC2-6 to go low at .5 bit. A STEP FORWARD (up-count) signal is sent to the counting circuitry, MLC2-6 remains low until the end of the distribution cycle at which time $\overline{PC}$ reverts to its low state thus removing the SAMPLE signal (returns to low state).

In a similar fashion, a LINE FEED or CARRIAGE RETURN character is detected and the RESET output goes low between .5 bit and 1.0 bit.

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The STEP REVERSE output goes low between .5 bit and 1.0 bit when a BACKSPACE Character is detected.

Refer to Timing Diagram 1 during the following discussion concerning Control Character Code Extension.

Assume an ESC has just been generated. $\overline{PC}$ goes high at the start of the character distribution cycle. At .25 bit SCS goes high, MLC1 gates (ESC) detect an ESCAPE (PREFIX) character, and MLC1-8 goes low. At .5 bit $\overline{SCS}$ reverts to its low state. MLD1-9 had been held low by MLE2-3 but at .5 bit MLE2-3 goes high and a SAMPLE pulse generated. MLD1-9 remains high until $\overline{PC}$ reverts to its low state. MLC2-10 and MLC2-9 inputs have detected bits 6 and 7 SPACING, therefore MLC2-8 is low. MLB2-8 (DELETE) is high. Thus between .5 bit and 1.0 bit, the CONTROL CHARACTER gate inhibits a STEP FORWARD signal (low). At the end of the distribution cycle, $\overline{PC}$ reverts to its low state, generates a clock pulse for MLD1-2, and resets the $\overline{SCS}$ and data bit latches. The MLD1 clock pulse causes MLD1-9 to go low.

The next character generated is any character in Columns 2,3,4, 5,6 or 7 except DELETE. The timing sequence is the same as described above. At .5 bit, SCS reverts to its low state, MLD1-9 is low, and the SAMPLE signal is inhibited. MLC2-8 is high and MLB2-8 is high, and Pin 48 (STEP FORWARD) remains high. An up-count (STEP FORWARD) signal is inhibited on the FINAL character of a Control Character Code Extension sequence. PC reverts to its low state at 1.0 bit and resets MLD1-6 low. MLD1-9 is held low by MLE2-3. If a DELETE character is generated, MLB2-5 is low. All other outputs specified remain unchanged. If a Control Character is generated, MLC2-8 is low, all other outputs remain unchaged.

Subsequent printed characters or spaces will allow MLD1-9 to go high at .5 bit and revert to a low state at 1.0 bit.

Additional information converning clocked flip-flop operation can be obtained from 8399 WD.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

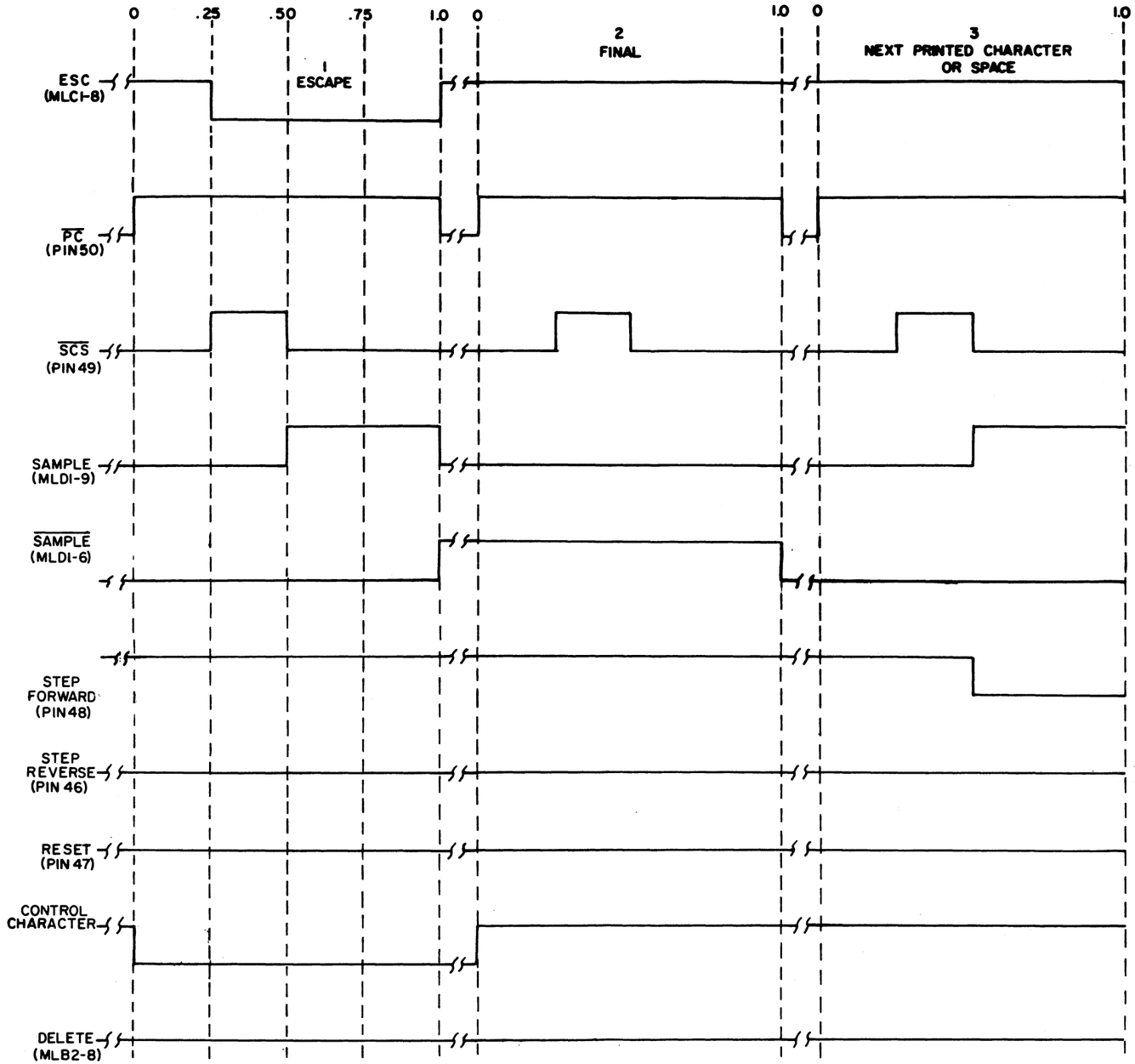
SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

b_7 → / b_6 → / b_5 →					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
Bits	b_4	b_3	b_2	b_1	COLUMN → / ROW ↓	0	1	2	3	4	5	6	7
	0	0	0	0	0	NUL	DLE	SP	0	@	P	`	p
	0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
	0	0	1	0	2	STX	DC2	"	2	B	R	b	r
	0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
	0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
	0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
	0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
	0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
	1	0	0	0	8	BS	CAN	(	8	H	X	h	x
	1	0	0	1	9	HT	EM	)	9	I	Y	i	y
	1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
	1	0	1	1	11	VT	ESC	+	;	K	[	k	{
	1	1	0	0	12	FF	FS	,	<	L	\	l	¦
	1	1	0	1	13	CR	GS	-	=	M	]	m	}
	1	1	1	0	14	SO	RS	.	>	N	^	n	~
	1	1	1	1	15	SI	US	/	?	O	_	o	DEL

ARRANGEMENT AAY

1-25-67

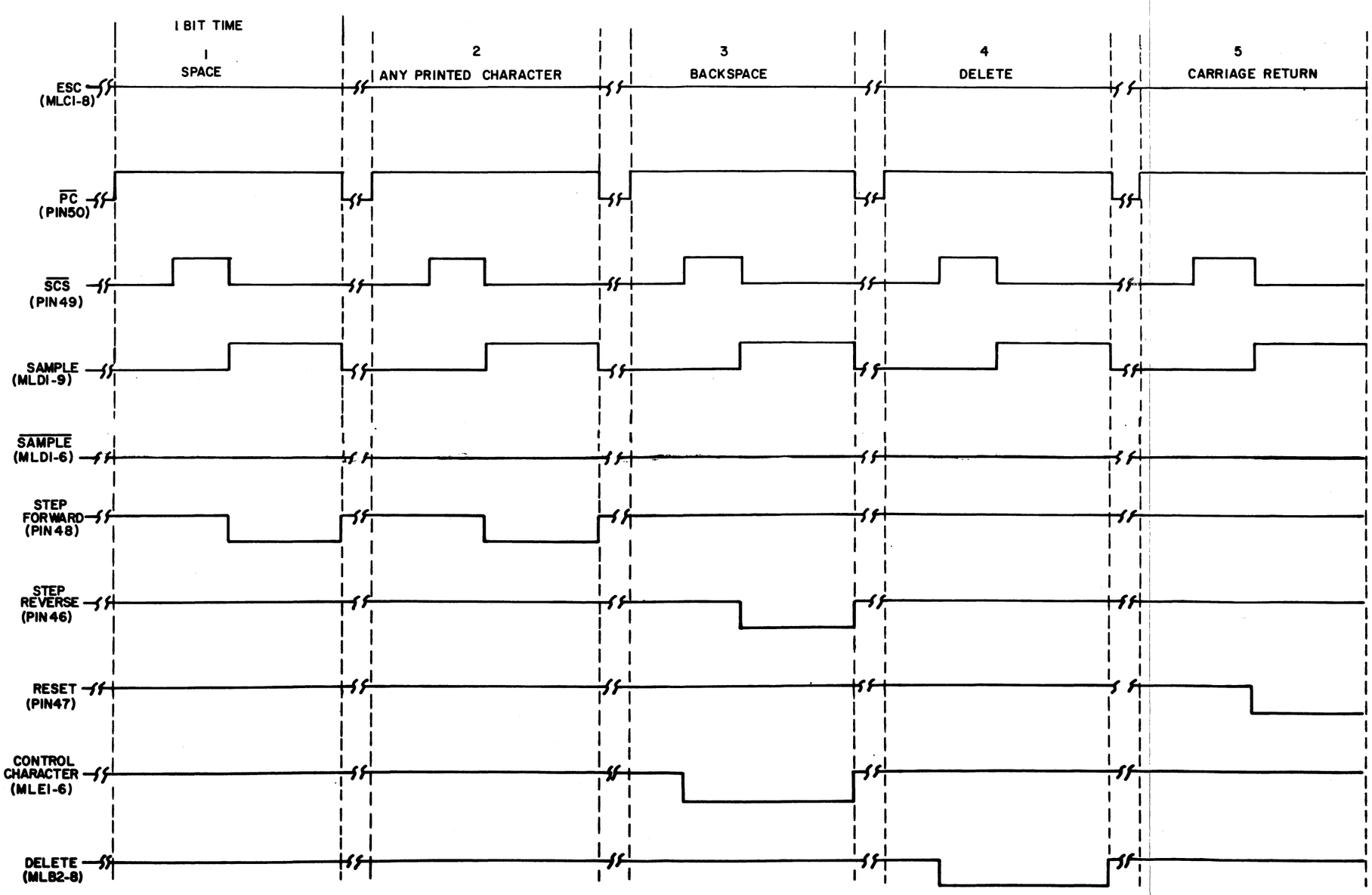
TIMING DIAGRAM I



NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

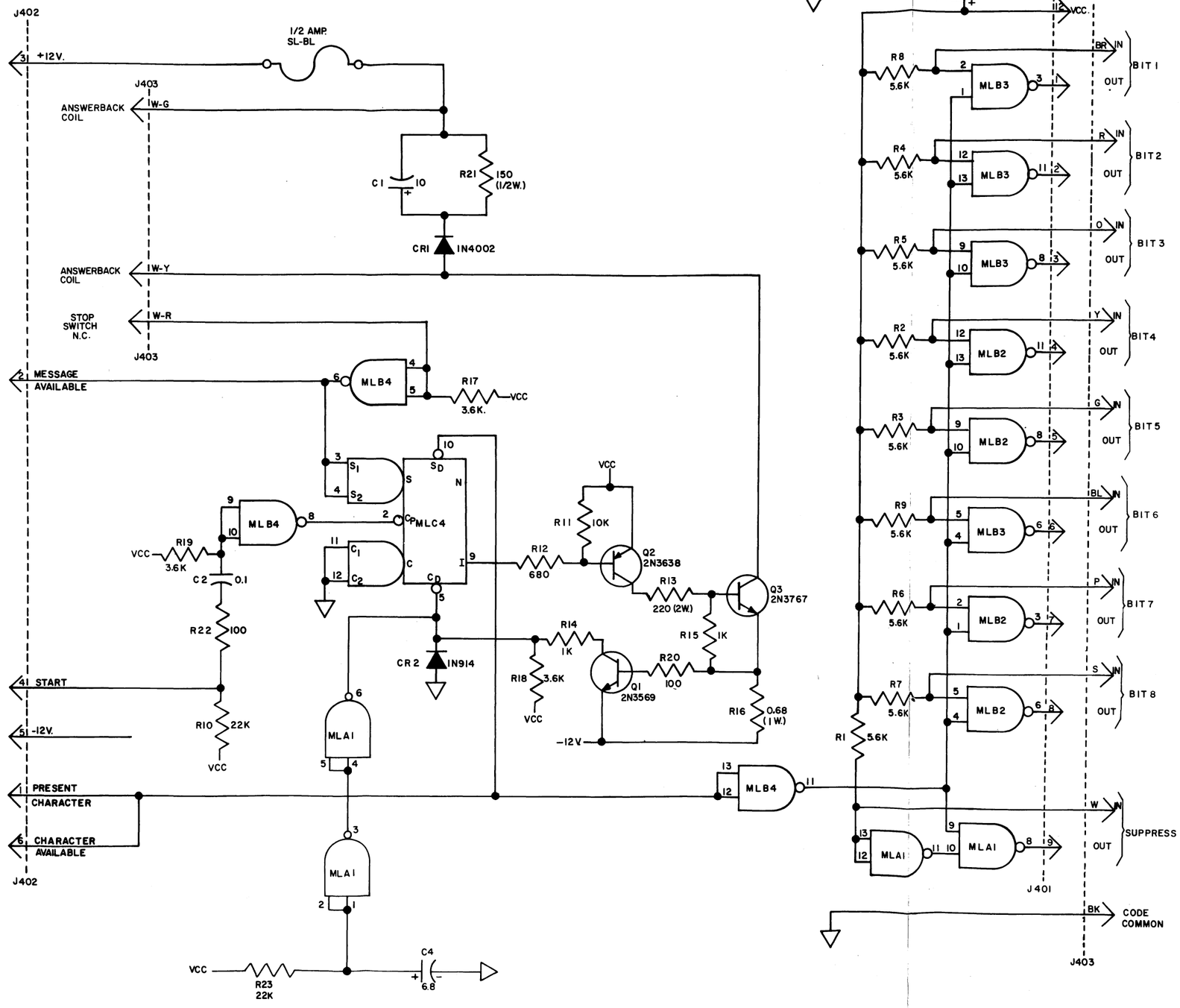
TIMING DIAGRAM II



NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

NO.	NOTES
1.	ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
4.	INDICATES FEMALE AND INDICATES MALE TERMINALS
5.	REFER TO 322047 FOR ASSEMBLY INFORMATION.
6.	S NUMBER
7.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD. ML D 3 — ROW, COLUMN, INTEGRATED CIRCUIT
8.	LOGIC NEGATION - A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
9.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER, THE GATE IS USE AS AN INVERTER.
10.	VCC IS PROVIDED TO THE INTEGRATED CIRCUIT PACKAGE ON PIN 14, AND GROUND ON PIN 7, THIS APPLIES TO ALL PACKAGES.
11.	THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC AND 0V, RESPECTIVELY.
12.	REFER TO 8399WD. FOR TRUTH TABLES.
13.	COLOR CODE LEGEND: BK-BLACK, O-ORANGE, R-RED, G-GREEN, P-PURPLE, S-SLATE, Y-YELLOW, W-WHITE, BR-BROWN, BL-BLUE
14.	REFERENCE CIRCUIT DESCRIPTION 8376WD-CD
15.	INDICATES CIRCUIT GROUND.



8376WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R
2	1-3-69	96485
3	2-27-69	96898

NOTE:
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SHEET-1

ANSWER BACK DRIVER

APPROVALS

D AND R	E OF M

E-NUMBER

PROD. NO. 8376 WD.

DATE 4-8-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. CHKD.

ENGD. A.B. APPD.

TELETYPE CORPORATION

8376WD

3

CIRCUIT DESCRIPTION OF THE ANSWER BACK DRIVER CARD (ASSEMBLY NUMBER 322047)

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NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION FOR THE ANSWER BACK DRIVER CARD (ASSEMBLY NUMBER 322047)

SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The 322047 Circuit Card Assembly is the electronic circuit portion for the 327801 Answer Back Assembly. The card contains logic necessary for the data outputs, and the logic required to drive the answer back coil. It is mounted to a plate with two circuit card clamps.

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

The inputs to the circuit assembly are of two types: Nand type integrated Diode Transistor Logic (DTL) and contact inputs. Each DTL input is approximately a 1.4 ma load to the device sinking current from it. At no time should any of the DTL inputs be more positive than 8 volts or more negative than -.7volt.

2.1.1 Present Character (Pin 1, J402)

The Present Character input controls the read-out of the data bits and initiates the timing to step the answer back drum to the next position. When this lead reverts to the O-state, the answer back begins to step and the data leads are sampled. The device driving this input must be capable of sinking three DTL loads.

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2.1.2 Data Inputs (Color BR, R, O, Y, G, BL, P, S, W)

These inputs are connected to the data contacts 1 through 8 and the suppress contact which ride the answer back drum. A contact closure is defined as a MARK while a contact open is defined as a SPACE. A closure on the Suppress input produces a suppression command. These contacts must be capable of sinking two DTL loads.

2.1.3 Start (Pin 4, J402)

An O-state on this lead produces the pulse necessary to start the answer back cycle. The device driving this input must be capable of sinking two DTL loads.

2.1.4 Code Common (Pin BK)

This input is the common contact for the answer back code contacts. The lead connects to the circuit board ground lead.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

2.1.5 Stop Switch (Pin W-R)

This contact input from a switch is closed when the answer back drum is in its home position. This switch must be capable of sinking two DTL loads.

2.2 Output Characteristics

The outputs from this assembly are Nand type integrated Diode Transistor Logic (DTL) outputs unless otherwise specified. The outputs will be rated by the number of DTL loads which may be driven. (Each DTL load is approximately 1.4 ma.)

2.2.1 Message Available (Pin 2, J402)

This output, when in the O-state, indicates that the sending device is selectable and has a message. It is capable of driving seven DTL loads.

2.2.2 Character Available (Pin 6, J402)

This output is a turn-around of the present character input. It indicates that a character is present and should now be taken. This lead is capable of sinking three loads less than the capability of the present character input.

2.2.3 Data Outputs (Pins 1,2,3,4,5,6,7,8,9 of J401)

These outputs present the MARK or SPACE bit information of a character to external logic. A 1-state indicates a MARK while a O-state indicates a SPACE. A SUPPRESS command is indicated by a O-state. Each output is capable of driving eight external DTL loads.

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2.3 Miscellaneous Requirements

2.3.1 Power Supply Inputs

Integrated Circuit Voltage and Current.

Pin	V_{DC}	I Max. (MA)
J401-12	+5V to +6.6V	110
J401-11	GND	

Coil Voltage and Current.

Pin	V_{DC}	I Max. (MA)
J402-3	+12	1.2
J402-5	-12	1.2

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

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1

2.3.2 Operating Temperature Range

0°C to 70°C (free air).

2.3.3 Storage Temperature Range

-40°C to +70°C.

2.4 Size

The card size is 4 inches by 4½ inches.

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly Drawing 322047 (MC047) and Schematic Drawing 8376 WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

The answer back assembly consists of a mechanical mechanism and an electronic circuit. The mechanism contains a stepping motor which moves a codable drum. Contact fingers ride the tines of the drum. The electronic circuit drives the stepping motor and provides the read-out for the contacts. Operation of the answer back circuitry is as follows:

Symbols and nomenclature referred to in this discussion are found on 8376 WD. Assume that the answer back drum is in its idle state; a START command is absent and no MESSAGE AVAILABLE is presented.

A START command initiates answer back operation. A low input in Pin 4 couples through a filter network consisting of R10, R22, R19 and C2 and into gate MLB4-8. This circuit combination provides a momentary clock pulse to the drive flip-flop, MLC4, for each START command. At clock time flip-flop MLC4 sets, causing the answer back drum to move to the first position. This is accomplished through the drive circuitry consisting of transistors Q1, Q2 and Q3.

209 Transistor Q3 acts as a switch which allows current to flow through the answer back coil. Q3 is driven by buffer amplifier Q2. When flip-flop MLC4 is set, Q2 is turned on which subsequently turns on Q3. Q3 permits current to build in the answer back coil at an exponential rate.

$$I=V/R\ e^{-R/L\ t}$$

This current flows through resistor R16. As the current through the coil increases, the voltage developed across R16 increases. This voltage build-up causes a slight current flow through transistor Q1. When the current through the coil is approximately 600 ma, Q1 conducts sufficiently to clear the MLC4 drive flip-flop on its C_D input. With the drive flip-flop cleared, Q2, Q3 and Q1 turn off. The answer back coil releases the armature which subsequently pulls the answer back drum to the 1st position.

At this time the normally closed STOP switch contact has opened, providing a MESSAGE AVAILABLE indication and disabling the synchronous inputs of the MLC4 flip-flop (the START input now has no effect on the circuit). Control of the answer back is now under the direction of the PRESENT CHARACTER input, Pin 1.

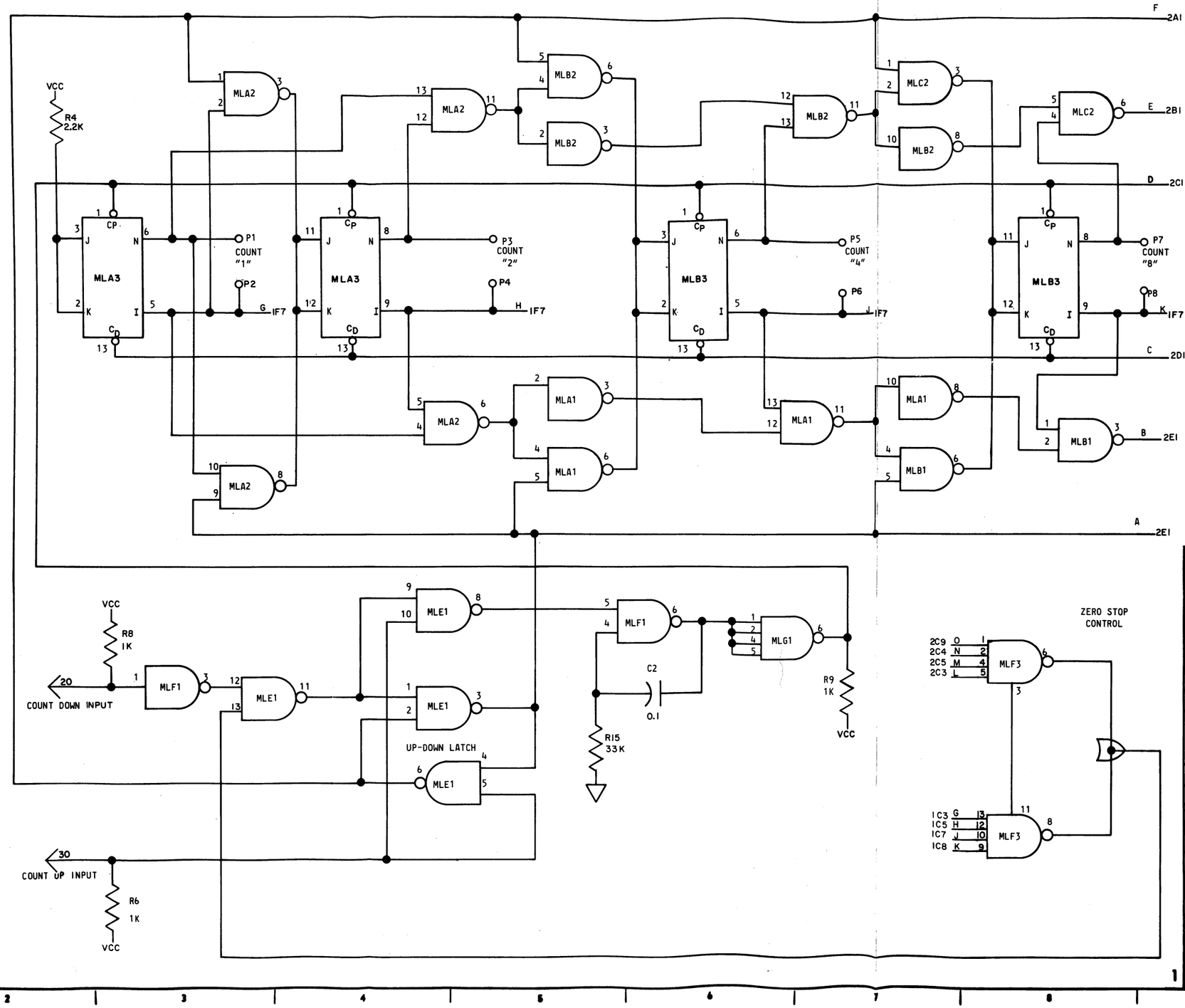
The terminal logic takes the MESSAGE AVAILABLE indication from the answer back logic and decides when to issue a PRESENT CHARACTER command. When the terminal issues the PRESENT CHARACTER (PC) command, three functions occur: data bits are presented at the data output gates for the duration of PC, the drive flip-flop is set through the S_D input, and a CHARACTER AVAILABLE is issued on Pin J402-6. Setting the drive flip-flop initiates the process of advancing the answer back drum to the next position in the same manner discussed previously. Flip-flop MLC4 turns transistor Q2 on which turns transistor Q3 on. The answer back armature begins to pick-up. Transistor Q1 monitors the coil current in order to clear the drive flip-flop at the proper time.

The PRESENT CHARACTER input has simultaneously initiated both the cycle to advance the answer back drum and the read-out of the character. The PRESENT CHARACTER command, normally one bit in length, must be removed before the answer back armature is fully attracted and before the drum is moved. Movement to the next position requires a time of approximately two bits at a 150 wpm character rate. Therefore, sufficient time is allowed to read the character before the drum is advanced.

Reading and advancing the answer back drum occurs with each PC command. When the drum advances to the home position, the STOP switch closes, causing removal of the MESSAGE AVAILABLE indication and priming the synchronous input of the drive flip-flop. The terminal logic does not issue further PRESENT CHARACTER commands when MESSAGE AVAILABLE has been removed. The answer back circuit is now in an idle state. The answer back may be started again by a START command on Pin J402-4.

The network consisting of element C1, R21 and CR1 provides noise suppression from the answer back coil.

NO.	NOTES
1.	ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTOR 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
4.	INDICATES FEMALE AND INDICATES MALE TERMINAL
5.	REFER TO 322055 FOR ASSEMBLY INFORMATION
6.	S NUMBER: 61,509S.
7.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD. ML D 2 ROW COLUMN INTEGRATED CIRCUIT
8.	CROSS REFERENCE NOTATION ON SCHEMATIC: 3B4 ROW COLUMN SHEET
9.	THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC AND 0V., RESPECTIVELY.
10.	VCC IS PROVIDED TO THE INTEGRATED PACKAGE ON PIN 14 AND GROUND ON PIN 7, THIS APPLIES TO ALL PACKAGES.
11.	REFER TO 8399WD. FOR LOGIC LEGEND AND TRUTH TABLES.
12.	REFERENCE CIRCUIT DESCRIPTION 8380WD-CD.
13.	P1-P24 MUST BE PROGRAMMED TO THE DESIRED COUNT BY CONNECTING THE TERMINALS PER 8380WD-CD.
14.	INDICATES CIRCUIT GROUND.



NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8380WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 1

SCHEMATIC
WIRING DIAGRAM
FOR
COUNTER CONTROL
(BI-DIRECTIONAL)

APPROVALS

D AND R	E OF M

E-NUMBER

PROD. NO. 8380WD.

DATE 3/29/68

P.D. FILE NO. G-A354AA

DRAWN	R.W.D.	CHKD.
ENGD.	A.F.T.	APPD.

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8380WD

SEE SHEET 1 FOR NOTES

8380WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

IB9 F
IB9 E
IC9 D
ID9 C
ID9 B
IE9 A

MLC2 MLC2 MLD2 MLD2 MLE2 MLE2 MLE2 MLE2

MLC3 CP J K CD N I

P9 COUNT "16"
P10 L IE7

MLC3 CP J K CD N I

P11 COUNT "32"
P12 M IE7

MLD3 CP J K CD N I

P13 COUNT "64"
P14 N IE7

MLD3 CP J K CD N I

P15 COUNT "128"
P16 O IE7

MLB1 MLB1 MLC1 MLC1 MLC1 MLD1 MLD1 MLD1

P17
P18
P19
P20
MLG3

P24
P23
P21
P22
MLG3

COUNT INPUTS P17 - P24

BELL OUTPUT 3

RESET INPUT 15

COUNT EOL LATCH

MLG2 MLG2 MLG2 MLG1

R7 1K VCC
R5 2.2K VCC

VCC
R11 10K
R13 3.6K
Q1 2N3638
R12 1.5K
R10 10K -12V
Q2 2N3569
R14 91 (1/2W)

33 COUNTER EOL LAMP
1 VCC
C1 6.8
2 GRD.
36 -12V.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 2

SCHEMATIC
WIRING DIAGRAM
FOR
COUNTER CONTROL
(BIDIRECTIONAL)

APPROVALS	
D AND R	E OF M

E-NUMBER

PROD. NO. 8380WD.

DATE 4/2/68

P.D. FILE NO. G-A354AA

DRAWN R.W.D.	CHKD.
ENGD. A.F.T.	APPD.

TELETYPE CORPORATION

8380WD

1

TC 484 (3-68)

CIRCUIT DESCRIPTION OF THE COUNTER CONTROL CARD (ASSEMBLY NUMBER 322055)

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NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

1

CIRCUIT DESCRIPTION OF THE COUNTER CONTROL CARD (ASSEMBLY NUMBER 322055)

SECTION I

1. BASIC FUNCTION

The 322055 Counter Control Card performs a binary up-down counting function and indicates the programmed End of Line (EOL). The visible indication of an EOL is an EOL lamp lighted on the control panel. The counting circuitry is capable of counting up to 255 keyboard generated characters, down counting by one each time a BACKSPACE character is detected, and resetting to zero each time a CARRIAGE RETURN character is detected.

1.1 The 322055 Circuit Card Assembly is considered an option and is intended to be used in conjunction with the 322045 Character Counter. Both cards are required if counting keyboard generated characters is a terminal requirement.

1.2 The 322055 Circuit Card is factory assembled and normally requires no adjustments in the field. The programmable EOL Count Input straps are factory installed per customer requirements. Any change in the printed line length requires strap re-programming to the new line length.

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

When used, the 322055 Counter Control obtains its inputs from the 322045 Character Counter (see Schematic 8375 WD). The inputs to this assembly are all integrated Diode-Transistor (DTL) type inputs. One DTL input is approximately a 1.4 ma load (Vcc = 5.25V) to the device sinking current. DTL inputs with pull-up resistors represent an additional sink current to the driving source. At no time should any of these inputs be more positive than +8.0 volts or more negative than -0.7 volts. Each card input is named by the function performed when the input goes low.

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A LOW is defined as a logical zero and a voltage level between 0 volts and +0.5 volts. A high is defined as a logical one and a voltage level between +5.0 volts and +6.6 volts.

2.1.1 Count Up Input (Pin 30)

The Count-Up input is normally high while the keyboard is idle and goes low at .5 bit into the printed character or SPACE character distribution cycle. Pin 30 reverts to a high state at the end of the distribution cycle (approximately 1.0 bit). Each high-low-high transition generates a clock pulse which adds a binary one to the contents of the binary counter. The source driving this input must be capable of sinking 6 DTL loads (Vcc = 5.25 Volts).

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

1

2.2.2 Count-Down Input (Pin 20)

The Count-Down input is normally high while the keyboard is idle and goes low for .5 bit into the BACKSPACE character distribution cycle. Pin 20 reverts to a high state at the end of the distribution cycle (approximately 1.0 bit). Each high-low-high transition generates a clock pulse which subtracts a binary one from the contents of the binary counter. The source driving this input must be capable of sinking 5 DTL loads (Vcc = 5.25 Volts).

2.2.3 Reset Input (Pin 15)

The Reset input is high at all times except when a CARRIAGE RETURN character is keyboard generated. A strapping option on the 322045 Character Counter allows the RESET input to go low when the NEW LINE key is depressed. A LINE FEED character is generated when the NEW LINE key is depressed. Pin 15 goes low for .5 bit into the CARRIAGE RETURN or NEW LINE character distribution cycle and reverts to a high state at 1.0 bit. Any high-low transition on this input resets all the NORMAL (N) counter outputs to a low state and all the INVERTED (I) counter outputs to a high state. The source driving this input must be capable of sinking 5 DTL loads (Vcc = 5.25 Volts).

3. OUTPUT CHARACTERISTICS

3.1 Bell Output (Pin 3)

The Bell Output is high at all times except when the programmed EOL is detected. This output can be used to control a bell driver which will provide an audible indication of EOL.

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3.2 Counter EOL (Pin 33)

This output is associated with a two stage complementary lamp driver consisting of Q1 and Q2. Pin 33 is approximately +12.5 volts above ground when the associated lamp is off and approximately -12.5 volts below ground when the associated lamp is on. The EOL lamp is off at all times except when the programmed EOL is detected.

4. MECHANICAL REQUIREMENTS

The 322055 card assembly is a standard 36-pin card which is inserted into a 36-pin edge card connector.

5. POWER SUPPLY REQUIREMENTS

Vcc (DC)	Current (ma) Max.
+11.65 to +13.75 Volts	35 ma
+5.0 Volts to +6.6 Volts	235 ma
-11.88 to -13.13 Volts	35 ma

6. TEMPERATURE RANGE

The operating temperature range is from 0°C to +70°C in free air. The storage temperature range is from -40°C to +70°C.

NOTE: REVISION INFORMATION MUST SO BE REFLECTED ON ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL JRD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SECTION ..

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly and Schematic drawings 322055 (MC055) and 8380 WD respectively.

1.2 8374 WD and 8375 WD (Keyboard Control and Character Counter schematics, respectively).

1.3 Logic Symbols and Truth Tables 8399 WD.

2. GENERAL

Refer to 8380 WD schematic and attached timing diagrams. The binary counter consists of eight dual J-K flip-flops which have a common clock pulse input and clear direct pulse input. J-K inputs (MLA3-2,3) are referred to Vcc through R4, thus enabling the trailing edge of each clock pulse to change the output state of MLA3-6,5. Each J-K flip-flop divides the clock pulse frequency by two. The J-K inputs of the other seven J-K flip-flops are connected in a two gate wired "OR" configuration. If MLE1-3 is low (Count-Up mode), the output of each gate connected to MLE1-3 enable the J-K inputs. The logic state of the J-K inputs at clock pulse time is determined by the other wired "OR" gate which samples the NORMAL (N) outputs of the preceeding flip-flop(s).

If MLE1-6 is low, (Down Count mode), the output of each gate connected to MLE1-6 enables the J-K inputs. The input logic state at clock pulse time is determined by the other wired "OR" gate which samples the INVERTED (I) outputs of the preceeding flip-flop(s). Each NORMAL output inverts its logic state if the J-K inputs are high at clock pulse time (high to low transition). The chart below shows the logic states of the NORMAL (N) flip-flop outputs, the binary representation of the decimal number, and the decimal number; during a COUNT UP sequence starting after a RESET pulse.

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CHART 1

Decimal Equivalent	P15	P13	P11	P9	P7	P5	P3	P1	Clock Pulse
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	1
2	0	0	0	0	0	0	1	0	2
3	0	0	0	0	0	0	1	1	3
4	0	0	0	0	0	1	0	0	4
5	0	0	0	0	0	1	0	1	5
6	0	0	0	0	0	1	1	0	6
7	0	0	0	0	0	1	1	1	7
8	0	0	0	0	1	0	0	0	8
9	0	0	0	0	1	0	0	1	9

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

Chart 2 shows the logic states of NORMAL (N) outputs, the binary representation of the decimal number and the decimal number; during a COUNT DOWN sequence starting on the tenth clock pulse.

CHART 2

Decimal Equivalent	P15	P13	P11	P9	P7	P5	P3	P1	Clock Pulse
8	0	0	0	0	1	0	0	0	10
7	0	0	0	0	0	1	1	1	12
6	0	0	0	0	0	1	1	0	13
5	0	0	0	0	0	1	0	1	13
4	0	0	0	0	0	1	0	0	14
3	0	0	0	0	0	0	1	1	15
2	0	0	0	0	0	0	1	0	16
1	0	0	0	0	0	0	0	1	17
0	0	0	0	0	0	0	0	0	18

3. DETAILED DESCRIPTION AND THEORY OF OPERATION

A common clear direct input has reset the NORMAL flip-flop outputs to a low (logic zero) state. The character preceeding CARRIAGE RETURN or NEW LINE was a printed character or space, therefore MLE1-3 is low, MLE1-6 is high, and the UP-DOWN LATCH is set in the COUNT UP counting mode. Inputs MLA2-9, MLA1-5, MLB1-5, MLB1-9, MLC1-13, MLD1-5 and MLD1-9 are low. The associated gates are disabled. These gates will be referred to as the COUNT DOWN gates. Inputs MLA2-1, MLB2-5, MLC2-1, MLC2-13, MLD2-1, MLE2-5, and MLE2-9 are high. The associated gates are enabled. These gates will be referred to as the COUNT UP gates. MLA2-2 monitors the INVERTED output (MLA3-5). This inhibits a change of state on MLA3-8 for all odd numbered clock pulses. The other input associated with each of the COUNT UP gates monitors the NORMAL outputs of the preceeding flip-flops and logically determines the J-K input (high or low) during the clock pulse. P1 (MLA3-6) changes state each clock pulse. P2(MLA3-8) changes states every second clock pulse. P15 (MLD3-8) changes state every 128th clock pulse.

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The Zero Stop Control inputs monitor the eight INVERTED flip-flop outputs. With the counter cleared, the Zero Stop Control inputs are high. Therefore, MLE1-13 is low and further down counting is inhibited. The trailing edge of the first clock pulse sets MLA3-6 and MLE1-13 high. The trailing edge of each successive clock pulse occurs at the end of the character distribution cycles and the character is counted at that time. The second clock pulse sets MLA3-6 low and MLA3-8 high. All other NORMAL outputs remain low (logic zero). The third clock pulse sets MLA3-6 high and MLA3-8 remains high. Other outputs remain low.

Each successive clock pulse adds one to the contents of the counter according to the binary sequence indicated in Chart 1. The 256th clock pulse resets the counter to zero.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

MLG-3 gates comprise a composite eight input gate. The eight COUNT inputs can be programmed to detect any count from 0 to 255 by means of wire straps. MLG3-6 low sets MLG2-6 low (COUNTER EOL LATCH) when all COUNT inputs are high, turns on the END LINE lamp on the keyboard control panel and indicates the programmed END LINE.

The lamp remains on until a CARRIAGE RETURN or NEW LINE character causes Pin 15 (RESET input) to go low, reset the COUNTER EOL LATCH, and clear the counter.

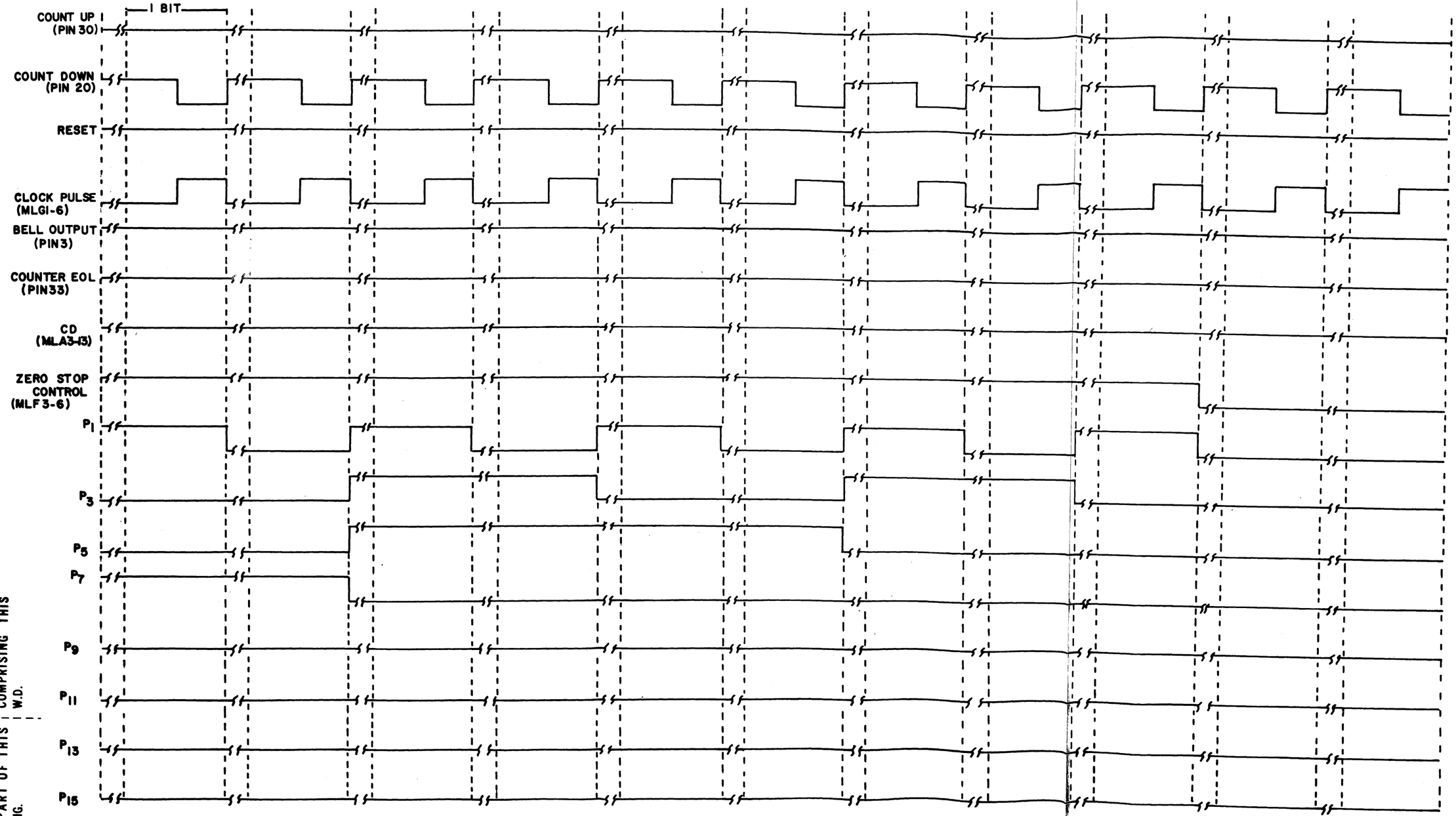
The lamp driver circuit is designed to operate full on or full off without intermediate states.

The input characteristics are compatible with DTL integrated circuit logic. When MLG2-6 goes low Q1 is turned on. Q1 collector current develops a positive signal across R10 and turns Q2 on. Q2 collector current is approximately 30 ma. The END LINE lamp is connected to Pin 33 and referred to the nominal +12.5 volt supply.

A COUNT DOWN signal (low on Pin 20) sets the UP-DOWN LATCH in the COUNT DOWN operating mode (MLE1-3 high, MLE1-6 low), generates a clock pulse, and disables the COUNT UP gates. The COUNT DOWN gates are enabled, monitor the INVERTED outputs of each preceeding flip-flop(s), and determine the J-K input logic level at clock pulse time. Each keyboard generated BACKSPACE character causes the counter to COUNT DOWN by one.

An RC integrating network (R15, C2) prevents noise pulses from creating unwanted clock pulses.

TIMING DIAGRAM (COUNT DOWN)



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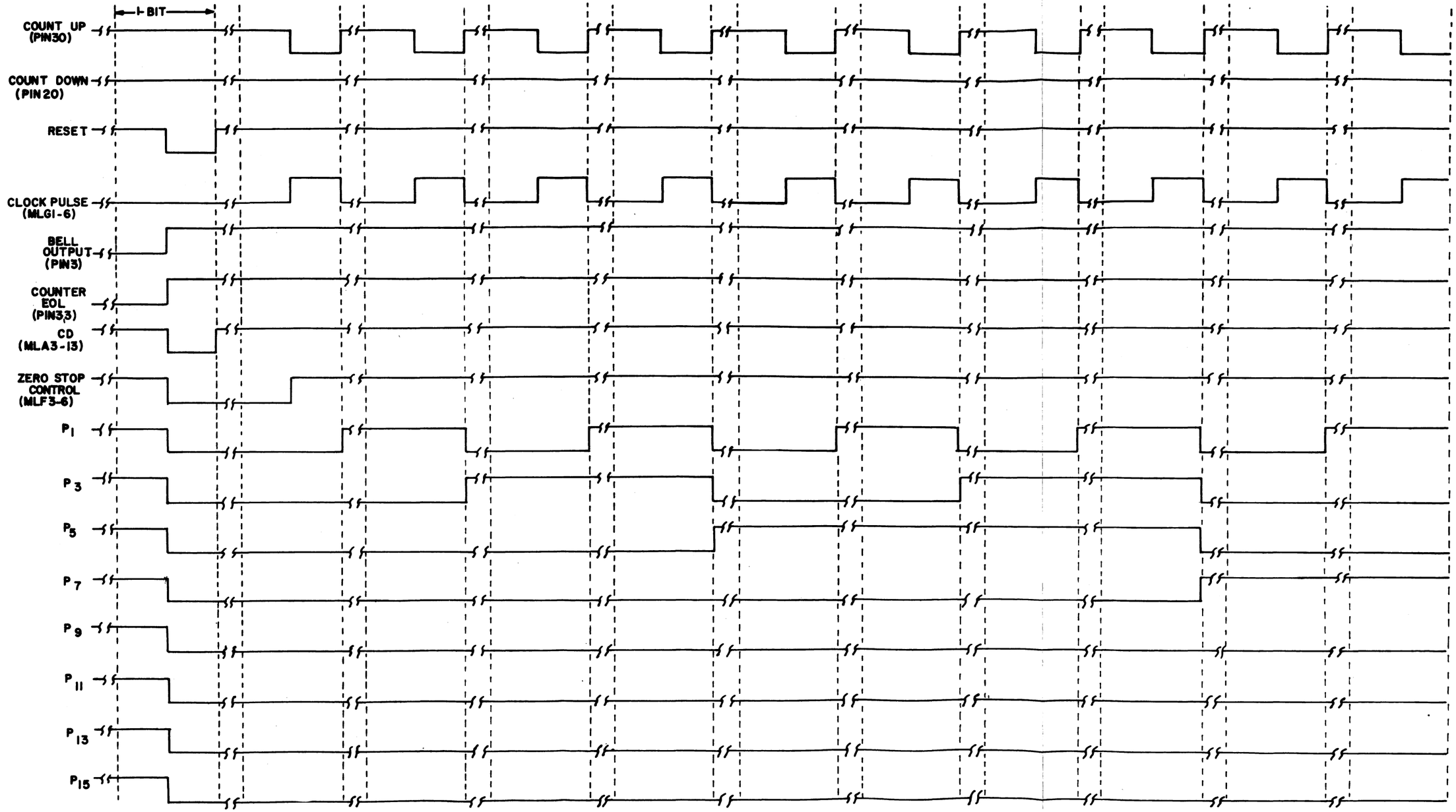
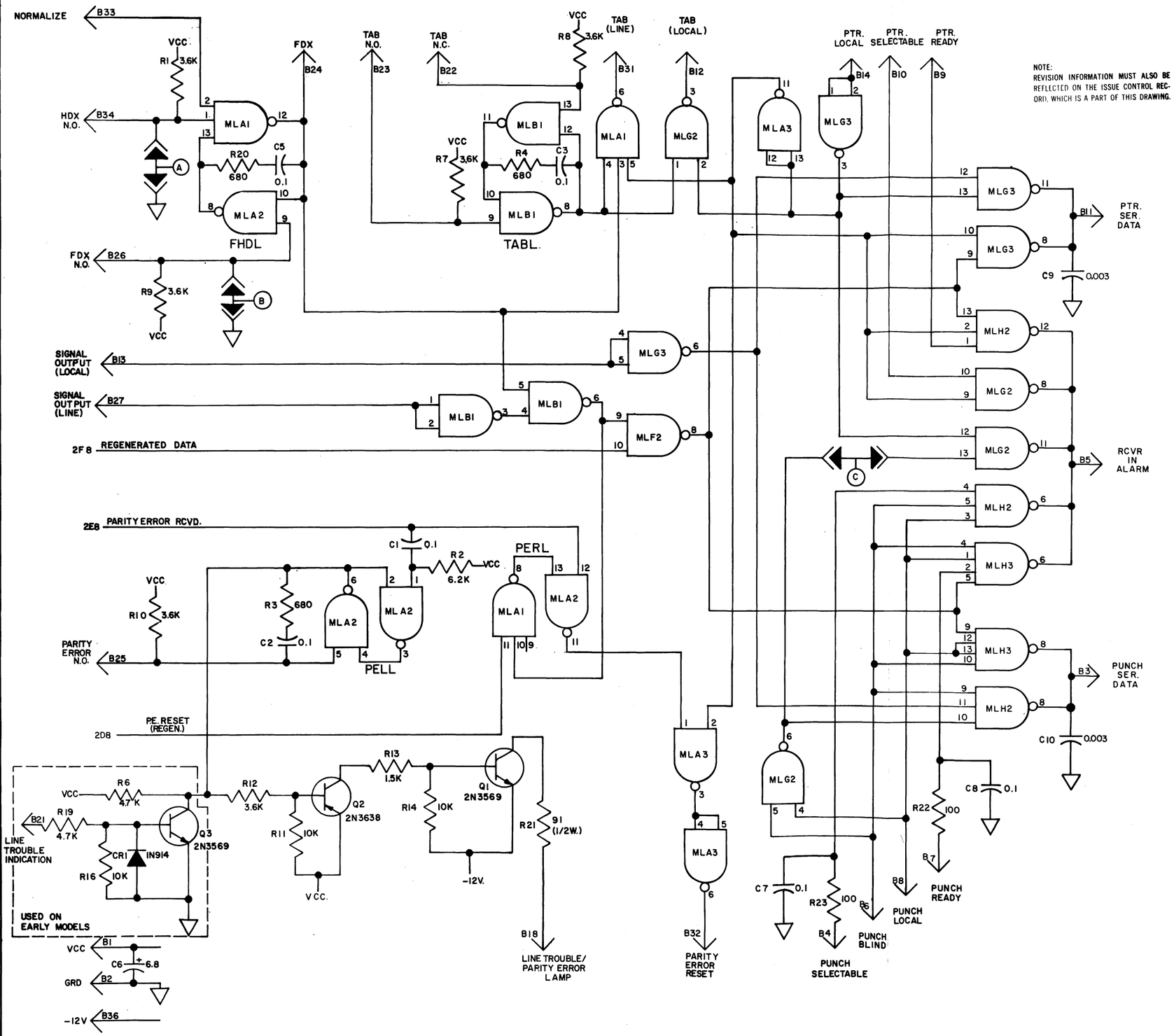
SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

TIMING DIAGRAM (COUNT UP)



NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

NO.	NOTES.
1.	ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTOR 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
4.	INDICATES OPTION. INDICATES FEMALE AND INDICATES MALE TERMINAL,
5.	REFER TO 322062 FOR ASSEMBLY INFORMATION.
6.	$ NUMBER: 61,434$.
7.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD. ML D 2 — ROW, COLUMN, INTEGRATED CIRCUIT
8.	CROSS REFERENCE NOTATION ON SCHEMATIC: 3 B 4 — ROW, COLUMN, SHEET
9.	THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC AND OV., RESPECTIVELY.
10.	VCC IS PROVIDED TO THE INTEGRATED PACKAGE ON PIN 14 AND GROUND ON PIN 7, THIS APPLIES TO ALL PACKAGES.
11.	REFER TO 8399WD. FOR LOGIC LEGEND AND TRUTH TABLES.
12.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER, THE GATE IS USED AS AN INVERTER.
13.	ABBREVIATIONS: USED: FHDL - FULL & HALF DUPLEX LATCH. TABL - TABULATION LATCH. PELL - PARITY ERROR LAMP LATCH. PERL - PARITY ERROR RECEIVED LATCH. TCL - TIME CONTROL LATCH.
14.	OPTIONS: A - DEDICATED HALF DUPLEX OPERATION STRAP MUST BE ADDED. B - DEDICATED FULL DUPLEX OPERATION STRAP MUST BE ADDED. C - ALTERNATE LINE RECEIVER. STRAP MUST BE ADDED.
15.	REFERENCE CIRCUIT DESCRIPTION - 8383 WD-CD.
16.	INDICATES CIRCUIT GROUND.



NOTE:
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8383WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R
2	2-24-69	96867-1

WDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D

SHEET 1

SCHEMATIC WIRING DIAGRAM FOR RECEIVE CONTROL (WITH REGENERATOR)

APPROVALS

D AND R	E OF M

E-NUMBER

PROD. NO. 8383 WD.

DATE 3-11-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B.	CHKD.
ENGD. A.B.	APPD.

TELETYPE CORPORATION

8383WD

2

SEE SHEET 1
FOR NOTES.

8383WD

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

BIT COUNTER

TIMER

F X 32

B16

B17

MLF3 FF

MLF3 FF

MLC3 FF

MLC3 FF

MLD2 FF

MLD3

MLHI FF

MLHI FF

MLGI FF

MLGI FF

MLF1

MLF1

MLF1

MLE2

MLE3

MLE2

MLE3

MLD3

MLE3

MLE2

MLE1

CR3

CR4

MLE1

MLF1

MLF1

B28

CHARACTER IN PROCESS

P.E. RESET

MLE3

1E2

MLF2

MLF2

B30

PARITY ERROR RCVD.

1D2

MLF2

REGENERATED DATA

B15

1C2

TCL

MLC1

MLC1

MLE1

MLE2

CR6

CR5

R15 100

C4 0.003

10 BIT CODE

B29

MLA3

LINE RCV DATA

B19

MLC1

MLC1

4.7K R5 VCC

RCV DATA (BB)

B20 4.7K R18

10K R17

CR2

Q4 2N3569

DATA

MLD1 FF

MLD2 FF

PARITY.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 2

SCHEMATIC
WIRING DIAGRAM
FOR
RECEIVE CONTROL
(WITH REGENERATOR)

APPROVALS	
D AND R	E OF M

E-NUMBER	
PROD. NO. 8383 W.D.	
DATE 3-6-68	
P.D. FILE NO. G-A354AA	
DRAWN W.P.B.	CHKD.
ENGD. A.B.	APPD.

TELETYPE CORPORATION

8383WD

CIRCUIT DESCRIPTION OF THE RECEIVE CONTROL CARD (W/REGENERATOR) (ASSEMBLY NUMBER 322062)

TABLE OF CONTENTS

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NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF THE RECEIVE CONTROL CARD (ASSEMBLY NUMBER 322062)

SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The 322062 Circuit Card Assembly controls and directs telegraph signals to the appropriate receiving device. The circuit receives serial input signals and provides serial output signals. An EIA input amplifier receives incoming on-line signals. Signals generated locally are received directly from sending distributors.

1.2 Several other functions are provided. These functions are:

1.2.1 Signal regeneration which changes input line data signals distorted 40% or less to output signals with less than 3% distortion. The regenerator assures a minimum character length of 9.8 units at 150 baud (150 wpm) and 10.6 units of 110 baud (100 wpm).

1.2.2 Detects improper received signal parity and provides power to an external parity error detection indicator lamp.

1.2.3 Half or full duplex selection - controls operation in either the half or full duplex mode.

1.2.4 Line or local tabulation - locks all sending devices during tabbing functions.

1.2.5 An output to indicate a receiving device in alarm - indicates an alarm condition for receivers. 131

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

The inputs to the circuit assembly are either EIA (RS-232-B) or nand type integrated diode transistor logic (DTL) inputs. EIA inputs are defined in Electronic Industries Association Standard RS-232-B. Each DTL input is approximately a 1.4 ma load to the device sinking current from it. At no time should any of these inputs be more positive than 8 volts or more negative than -.7 volts.

2.1.1 Received Data (Pin 20)

This input receives an EIA data signal from the signal line. This input is marking when the voltage is between OV to -25V and is spacing when the voltage is between +3V to +25V. A spacing signal greater than .5 bit in length forces the regenerator to cycle and monitor the line for the duration of one character.

2.1.2 10-11 Bit Code (Pin 29)

This input is grounded when the regenerator is operating with signals containing 10 bits per character (one stop bit). It is open or high for characters containing 11 bits (two stop bits). The device driving this input must be capable of sinking three DTL loads.

2.1.3 FX32 (Pin 16)

This input is from an external oscillator. The frequency of the oscillator must be 32 times the desired bit rate. The device driving this input must be capable of sinking two DTL loads.

2.1.4 HDX N.O. (Pin 34)

This input is normally in the 1-state. When in the full duplex mode (FDX), a low (0-state) on this input will change the logic to half duplex mode. This contact must be capable of sinking two DTL loads.

2.1.5 FDX N.O. (Pin 26)

This input is normally in the 1-state. When in the half-duplex mode (HDX) a low on this input will change the logic to the full duplex mode. This contact must be capable of sinking two DTL loads.

2.1.6 Normalize (Pin 33)

This input is normally in the 1-state. At certain times it is desirous to condition selected set logic to a predetermined state. A low input on this lead will condition the full-half duplex latch (FHDL) to the half duplex state. This input represents one DTL load.

132 2.1.7 Signal Output (Local) (Pin 13)

This input is connected to the local distributor's data signal output and represents one DTL load. The signal moves through gated logic to the proper receiving device.

2.1.8 Signal Output (Line) (Pin 27)

This input is connected to the line distributor's data signal output and represents one DTL load. The signal moves through gated logic to the proper receiving device.

2.1.9 Parity Error N.O. (Pin 25)

This input is normally in the 1-state. A low on this input will reset the parity error lamp latch (PELL) which turns off the parity error received lamp driver. The device driving this input must be capable of sinking two DTL loads.

2.1.10 Line Trouble Indication (Pin 21)

This is an EIA input from an external control device or from a data set. It identifies an abnormal line condition. An ON condition causes the Parity Error or Line Trouble lamp to light.

2.1.11 Tab N.C. (Pin 22)

This is a contact input from the typing unit indicating to a local sending device that a tabbing condition is in process. The contact must be capable of sinking two DTL loads.

2.1.12 Tab N.O. (Pin 23)

Same as Section 2.1.11.

2.1.13 Printer Local (Pin 14)

This input primarily directs the proper data signals (line or local) to the typing unit and primes certain "receiver in alarm" gates. It also inhibits the line tab and parity error outputs (ribbon shift) when the printer is in the local mode. This input represents one DTL load.

2.1.14 Printer Selectable (Pin 10)

This lead monitors the typing unit's paper supply. With a full paper supply the lead is normally in the 0-state. It should revert to the 1-state when a paper out condition exists or upon termination of a call if a low paper condition exists. This lead represents one DTL load.

2.1.15 Printer Ready (Pin 9)

This input is normally low when the printer motor is operating. It reverts to the 1-state when the motors are OFF. This information is used to prime "alarm" logic. This lead represents one DTL load. 133

2.1.16 Punch Ready (Pin 7)

This input is normally low when the punch motor is operating. When the punch motor is OFF, it reverts to the 1-state. It is used to prime "alarm" logic. The input represents one DTL load.

2.1.17 Punch Local (Pin 8)

This input directs the proper data signals (line or local) to the punch and primes certain "receiver in alarm" gates. When this lead is in the 0-state, the punch receives local data. In the 1-state and no blind condition, the punch receives line data. This lead represents one DTL load.

2.1.18 Punch Blind (Pin 6)

When this input is in the 0-state, the punch is blinded to data signals. This input represents five DTL loads.

2.1.19 Punch Selectable (Pin 4)

This lead monitors the punch tape supply. With a full tape supply the lead is normally in the 0-state. It should revert to the 1-state when a paper out condition exists or upon termination of a call if a low tape condition exists. This lead represents one DTL load.

2.2 Output Characteristics

The outputs from this assembly are either nand type diode transistor logic (DTL) or transistor driver outputs. Each output will be rated by the number of DTL loads it can sink. Each DTL load is approximately 1.4 ma.

2.2.1 Line Received Data (Pin 19)

This output follows the EIA received signal input lead. This lead is in the 0-state when the EIA input is spacing and is in the 1-state when the EIA input is marking. It is used in other system logic to indicate the presence of a long spacing signal. This output will sink 20 DTL type loads.

2.2.2 Regenerated Data (Pin 15)

This output provides a data signal derived from the received signal input lead which is practicably distortion free. This lead is in the 1-state for a MARK and in the 0-state for a SPACE. This output will sink seven loads.

2.2.3 Parity Error Received (Pin 30)

This output, normally in the 1-state, reverts to the 0-state whenever a character is detected with incorrect vertical parity. This indication is presented at the end of the errored character. This lead will sink six loads.

134 2.2.4 Full Duplex (FDX) (Pin 24)

For half duplex operation this output is in the 1-state. When a full duplex command is received, this output reverts to the 0-state. It is capable of sinking four loads.

2.2.5 Tab (Line) (Pin 31)

This output is normally in the 1-state. When a tabbing function occurs with the unit in the local and half duplex mode, the lead reverts to the 0-state until the tabbing function is completed. This indication is used in other system logic to intercept the line distributor's "PRESENT NEXT CHARACTER" (PNC) output. It will sink eight DTL loads.

2.2.6 Tab (Local) (Pin 12)

This output is normally in the 1-state. When a tabbing function occurs with the typing unit in the local mode, the lead reverts to the 0-state until the tabbing function is completed. This indication is used in other system logic to intercept the local distributor's "PRESENT NEXT CHARACTER" output. It will sink eight DTL loads.

2.2.7 Printer Serial Data (Pin 11)

This lead presents serial data derived from the incoming signal line from the line/local distributor to the printer selector magnet driver. It is in the 1-state for a marking bit and in the 0-state for a spacing bit. This output will sink seven DTL loads.

2.2.8 Punch Serial Data (Pin 3)

This lead presents serial data derived from the incoming signal line or from the line/local distributor to the punch selector magnet driver. A marking bit is in the 1-state and a spacing bit is in the 0-state. This output will sink seven DTL loads.

2.2.9 Receiver in Alarm (Pin 5)

This output indicates to external logic that a receiving device is in an alarm condition or that no receiving device is available. This lead is normally in the 1-state but changes to the 0-state when an alarm condition is present. This output will sink four DTL loads.

2.2.10 Parity Error Not(Pin 32)

This output normally in the 0-state reverts to the 1-state upon the reception of a parity errored character and remains in the 1-state until a character with the correct parity is received. This signal is used in external logic to change the color of the printed character. Eight loads may be attached to this lead.

2.2.11 Line Trouble/Parity Error Lamp (Pin 18)

This output drives a lamp located on the control strip to indicate a parity error. A parity error will cause this lead to change to the "ON" state providing power to this lamp. It remains in this state until manually reset. 135

2.2.12 Character in Process (Pin 28)

When this lead is in the 1-state, the regenerator is idling. This lead reverts to the 0-state during the time in which a character is processed through the regenerator. This output will sink one DTL load.

2.3 Size

The receive control card measures 5-3/4 x 4-1/4 inches. It is designed to mate with a standard 36 pin circuit card connector.

2.4 Options

2.4.1 10-11 Unit Code

The receive control may be changed from an eleven unit code to ten unit code by grounding Pin 29.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

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2.4.2 Half Duplex (Strap A)

The assembly may be permanently strapped for half-duplex by having strap A in place.

2.4.3 Full Duplex (Strap B)

The assembly may be permanently strapped for full duplex by having strap B in place and removing strap A.

2.4.4 Auxiliary Receiver (Strap C)

Strap C remains in place when an auxiliary receiving device, such as a reperforator, is part of the system. It is used to indicate, along with other receiving devices, a capability to receive incoming line data. If no receiving device is in the line mode, an alarm condition is generated.

2.5 Miscellaneous Requirements

2.5.1 Power Supply Requirements

V_{DC}	I ma (max)
5V to 6.6V	390 ma

2.5.2 Operating Temperature Range

0°C to 70°C (free air)

2.5.3 Storage Temperature Range

-40°C to +70°

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SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 See assembly drawing 322062 (MC062) and schematic drawing 8383 WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 General

The Receive Control card assembly is described in two parts, signal regeneration (regenerator) and data control (receive control). Refer to the timing diagrams, flow chart, and schematic 8383 WD to aid in understanding the following description. The flow chart is intended to be used as a guide to help in understanding the operation of the regenerator. It should be studied in conjunction with the circuit schematic and timing diagram. The rectangular symbols denote functions that are to be performed, and the triangular shaped symbols denote a decision point. It is not intended that any of the symbols be construed to represent logic functions. The flow chart is primarily intended to relate circuit operation with respect to time.

2.2 Regenerator

The mode of operation described first is for characters of 10 unit code. This requires a ground or 0-state on Pin 29.

Assume that the regenerator is in an idle condition. The timer is not operating because the output of the Start Gate, MLD3-6, is in the 0-state. This gate is in the 0-state when the receive signal input is MARKING continuously and the Timer Control Latch, TCL, has been reset. TCL resets at the end of each character.

When a SPACING signal (Start bit) appears at the receive signal input, Pin 20, the output of MLC1-11 switches to the 0-state. This forces the Start Gate to the 1-state, releasing the timer.

After 1/2 bit time duration, a clock pulse appears at MLD3-8. This sets a one count in the bit counter, which in turn sets TCL via MLF1-3 and MLF1-6. The output of the TCL clamps the Start Gate "ON" for a full character interval. Control of the timer is now removed from the signal line.

If the SPACING signal is not present for a full 1/2 bit interval, however, the TCL will not have been set. Consequently, as the Receive Signal Input returns to a MARK, the Start Gate reverts to a 0-state, clearing the timer to the idle state. A character, therefore, will not be regenerated.

When the SPACING signal is longer than 1/2 bit, the timer is locked on and delivers clock pulses at bit frequency. These pulses are used to

cycle the bit counter, the data flip-flop, and the parity flip-flop. The function of each of these circuits is as follows:

2.2.1 Bit Counter

The function of the bit counter, composed of four binary elements and two gates arranged to operate as a decade counter, is that of timing out a character interval. When a count of ten is reached, the output of MLF1-3 switches to the 0-state. (Refer to the diagram and timing chart of Figure 1 for information on intermediate states of the bit counter.)

2.2.2 Data Flip-Flop

Clock pulses generated by the timer process data through the Data Flip-Flop, MLD1. Incoming line data (which may be distorted) appears at the synchronous set and clears inputs of MLD1. This data is sampled and read into the data flip-flop by the clock pulses. The inverted output of the data flip-flop, distortion free, is applied to the Regenerated Data Gate, MLF2-11.

2.2.3 Parity Flip-Flop

The function of the parity flip-flop is to search for even parity on the 8 data bits of a character. The parity flip-flop changes states each time a MARK signal from the data flip-flop is read into it by the timer clock. The inverted output of the parity flip-flop is applied directly to the Parity Error Received Gate, MLF2-6, where it is sampled at the end of each character by the bit counter. The output of the gate remains in the 1-statefor correct parity or, conversely, switches to the 0-state if a parity error has been detected.

138 2.2.4 Timer Control Latch Reset

After the 10th count is reached, the timer continues counting for an interval designed to guarantee regeneration of a minimum length stop bit. When operating in the 10 unit character code, this time period is approximately 0.3 of a bit. At this time Stop Bit Regenerator Gate, MLE1-6, has three of its four inputs primed (extender inputs CR5 and CR6 primed by 10 unit code and TCL respectively) to reset the timer control latch. The remaining input is controlled by the Synchronism Gate, MLE3-8, which senses for either the presence of correct parity or the presence of a marking bit in the data flip-flop. If either is present the regenerator is considered to be in synchronism with the signal line and gate MLE3-8 is in the 1-state. Now all inputs of the stop bit regenerator gate are in the 1-state, resetting TCL and the timer. The regenerator now waits for a new character.

If the regenerator is not in apparent synchronism with the signal line, i.e., parity incorrect and no marking bit in the data flip-flop, Synchronism Gate, MLE3-8, will not permit the stop bit regenerator gate to reset TCL and the timer. The regenerator continues to run 0.3 of a bit

beyond the next clock pulse or pulses until the conditions for synchronism are achieved. Only then will TCL and the timer be reset. The regenerator logic is now conditioned for the start of a new character. It waits for the next 1/2 bit SPACING "start" signal to begin a new cycle.

For units operating with characters consisting of 11 bits, i.e., with two stop bits, Stop Bit Regenerator Gate, MLE1-6, is electrically replaced by Stop Bit Regenerator Gate MLE1-8. This is accomplished by removing the ground on Pin 29. MLE1-6 is inhibited through its CR5 input while MLE1-8 is primed through its CR3 input. The Stop Bit Regenerator Gate, MLE1-8, operates in a very similar manner to MLE1-6. Its function, however, is to time out 1.1 bit elements instead of .3 elements after the 10th count. Three inputs are used for this purpose, two from the timer and one from a latch made up of MLE3-11 and MLE2-8.

The MLE2-12 gate has inputs from the timer such that when .75 bits are sensed, the MLE3-11, MLE2-8 latch is set. Approximately .35 bits later the two inputs to MLE1 from the timer are high. If apparent synchronization is present (MLE3-8 high) the Stop Bit Regenerator Gate switches to the 0-state, resetting TCL. When TCL is reset, the MLE3-11, MLE2-8 latch is reset, and MLE1-8 is inhibited via diode CR4.

2.2.5 Parity Count Inhibit Gate

The function of the Parity Count Inhibit Gate, MLF2-3, is to prevent sampling for parity of the incoming signal during a stop bit. When the first clock pulse occurs, the stop bit of the previous character is stored by the data flip-flop. Consequently, the first clock pulse should not sample the data flip-flop for parity. Also, when operating in the 11 unit character mode, the last clock pulse of a character occurs during the stop pulse and, therefore, should not be permitted to sample the data flip-flop. During both these time periods the output of MLF2-3 is low and the parity flip-flop is inhibited.

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2.3 Receive Control

The second major function of the receive control circuit card is: to direct data received from a multiplicity of sources to the proper receiving device, to control the receiving alarm indicators, and to perform miscellaneous control functions associated with the receivers.

2.3.1 Receive Data Logic

Data is received from three sources. These are: regenerated data from the regenerator, data generated by the on-line sending distributor, and data generated by the local sending distributor. Assume a half duplex operating mode. Data received from the local sending distributor passes through MLG3-6 and primes output serial data gates associated with the printer and punch. Data associated with the line distributor passes through MLB1-3, MLB1-6 (primed in the half duplex mode) and MLF2-8. The MLF2-8 output also

1

primes serial data gates associated with the printer and punch. Receive data from the regenerator passes through MLF2-8 and also primes serial data gates associated with the punch and printer.

The input at Pin 14 is low when the printer is in the local mode, and high when it is in the on-line mode. Consequently, MLG3-11 is primed only when the printer is in the on-line mode. Thus, local data appears at Pin 11, the printer serial data output, when a printer local command appears at Pin 14, and on-line data appears at Pin 11 when an on-line command appears at Pin 14.

When the punch is in the local mode a low appears at Pin 8, and when the punch is on-line a high appears at that input. This input primes gate MLG2-6 which has as its second input the punch blind signal received at Pin 6. The punch blind signal is low when the punch is to be blinded and high when it is to be enabled. Thus, when the punch is local and enabled, only local data will appear at Pin 3, the punch serial data output. When the punch is enabled, on-line (Pin 8 high) and only on-line data will appear at Pin 3. When the input received at Pin 6 is low, signifying that the punch is to be blinded, the output at Pin 3 will remain continuously MARKING.

2.3.2 Receive Alarms

The output at Pin 5, receiver in alarm, is high when all receivers are functioning normally and low for an alarm condition. An alarm condition exists when one of the receiving devices is unable to function, i.e., out of paper, or, when no receiver is in the on-line condition during receipt of a message. The following are alarm conditions:

Condition 1: The printer is on-line, the printer motors are not yet up to speed(printer not ready, Pin 9 high), and a spacing bit is received on line. MLH2-12 is switched.

Condition 2: The printer is on-line and a paper alarm is present. MLG2-8 is switched.

Condition 3: No receiving device is in the on-line mode. MLG2-11 is switched.

Condition 4: The punch is on-line and a tape alarm is present. MLH2-6 is switched.

Condition 5: The punch is on-line, the punch motors are not yet up to speed (punch not ready, Pin 7 high), and a spacing bit is received on line. MLH1-6 is switched.

All alarm gate outputs are connected together and appear at Pin 5. For applications where a printer must be on-line for a call to be received, strap C is removed. With strap C removed, MLC2-11 will switch to an alarm condition whenever the printer is off-line.

2.3.3 Tabbing Control

The purpose of the tabbing control logic is to prevent transmission from a local reader or keyboard until response to a tabbing function is completed by the local printer. The tabbing latch, TABL, is set by a contact on the typing unit during tabbing and is reset by a contact when the tabbing is complete. The output of this latch at MLB1-8 primes the MLA1-6 and the MLG2-3 gates. The MLG2-3 gate has two inputs. The second input is primed while the printer is in the local mode. The MLA1-6 gate has three inputs. The second input is high while the printer is on-line, and a third input to the MLA1-6 gate is high when the unit is in the half duplex mode. Thus a line tab indication at Pin 31 (0-state) will be present only when the typing unit is on-line, tabbing is in process, andthe terminal is in the half duplex mode. A tab condition will be present at Pin 12 (0-state) only when the printer is in the local mode and tabulation is in process.

2.3.4 Full Duplex

A full duplex latch, FHDL, is operated directly from the typing unit. When a full duplex command is sensed, Pin 26 is shunted to ground (0-state) setting the latch. The latch is reset bhen a half duplex command at Pin 34 is sensed, or when the system is normalized by a logical zero at Pin 33. The output of the latch, MLA1-12, at Pin 24, is a logical zero for full duplex and a logical one for half duplex. The output of FHDL also primes gates MLB1-6 and MLA1-6. When in the full duplex mode, locally generated line data will not pass through MLB1-6 and, therefore, will not be copied by the local printer. When in the full duplex mode, and while a tabulation is taking place, the line tab output will remain high. Transmission by a local reader or keyboard will continue, therefore, since the system is in full duplex mode.

The system may be wired permanently full duplex or permanently half duplex. For permanent full duplex, strap B should be connected and strap A removed. For permanent half duplex operation, strap A should be connected and strap B removed. For on-line control, both straps are removed. 141

2.3.5 Parity Error Display Logic

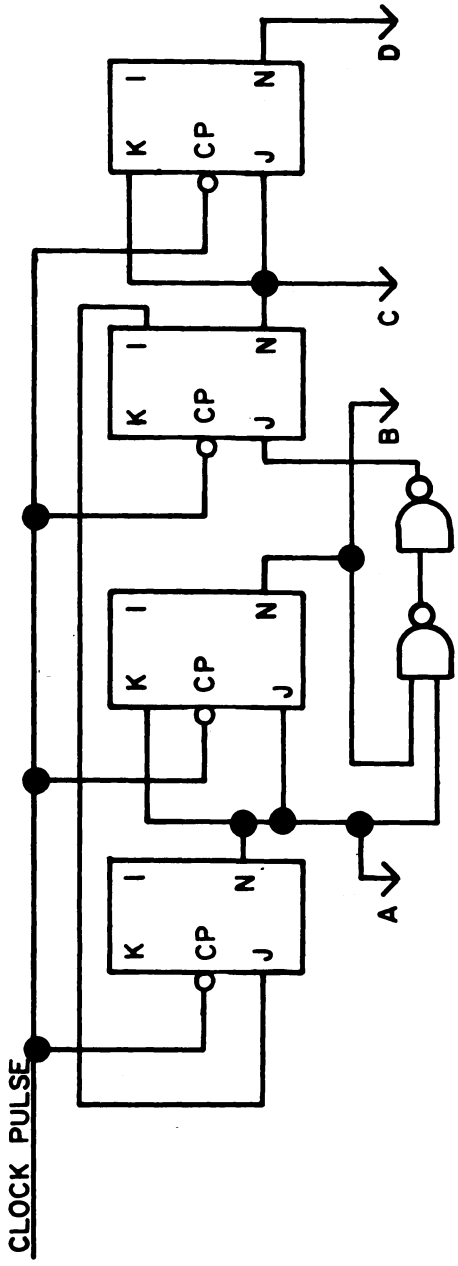
Parity errors may be displayed in either or both of two ways. These are a lamp located on tye control panel, or, by a ribbon shift to print the errored character in red. When a parity error is detected by the parity error circuitry of the regenerator, the parity error lamp latch, PELL, and the parity error ribbon latch, PERL, are both set. The output of the PELL latch drives a lamp amplifier composed of transistors Q2 and Q1, having an output at Pin 18. The output is turned ON, a logical lamp zero for a parity error. The output may also be turned ON by an EIA input (1-state) at Pin 21, the line trouble indication input. The "Parity Error or Line Trouble" output may optionally display either parity error or line trouble (Carrier Fail) or both. The PELL latch, and the associated parity error or line trouble lamp is turned OFF by a logical zero applied

at Pin 25. The logical zero is derived from a reset switch contact closure on the control panel.

As an option, the parity error causes the printing of the errored character in red via the PERL latch. The output of this latch is applied through MLA3-3 and MLA3-6 to Pin 32. A logical one at Pin 32 operates the ribbon magnet through an amplifier on the ribbon magnet amplifier card. At the end of a character, the PERL latch is reset by the regenerator or by receipt of a SPACING signal identifying the beginning of the next character. A second input to the MLA3-3 gate prevents operation of the parity error ribbon circuitry when the printer is in the local mode.

BIT COUNTER DIAGRAM AND TIMING CHART

	0	1	2	3	4	5	6	7	8	9
A	L	H	L	H	L	L	H	L	H	L
B	L	L	H	H	L	L	L	H	H	L
C	L	L	L	L	H	L	L	L	L	H
D	L	L	L	L	L	H	H	H	H	H



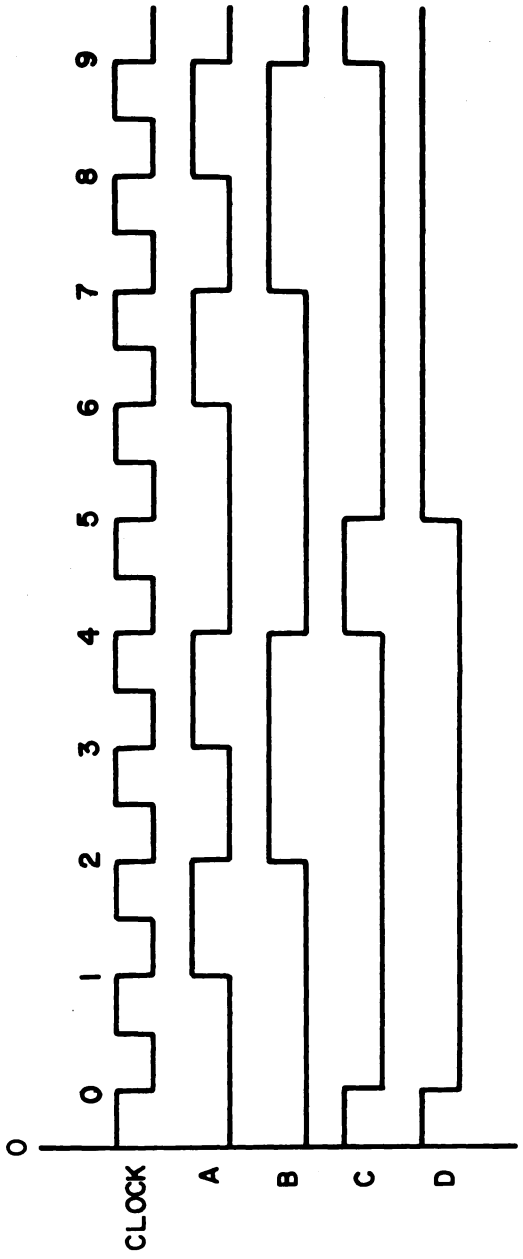


FIGURE 1

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

TIMING DIAGRAM
RECEIVING SIGNAL REGENERATOR
P/O 322062 RECEIVE CONTROL ASSEMBLY

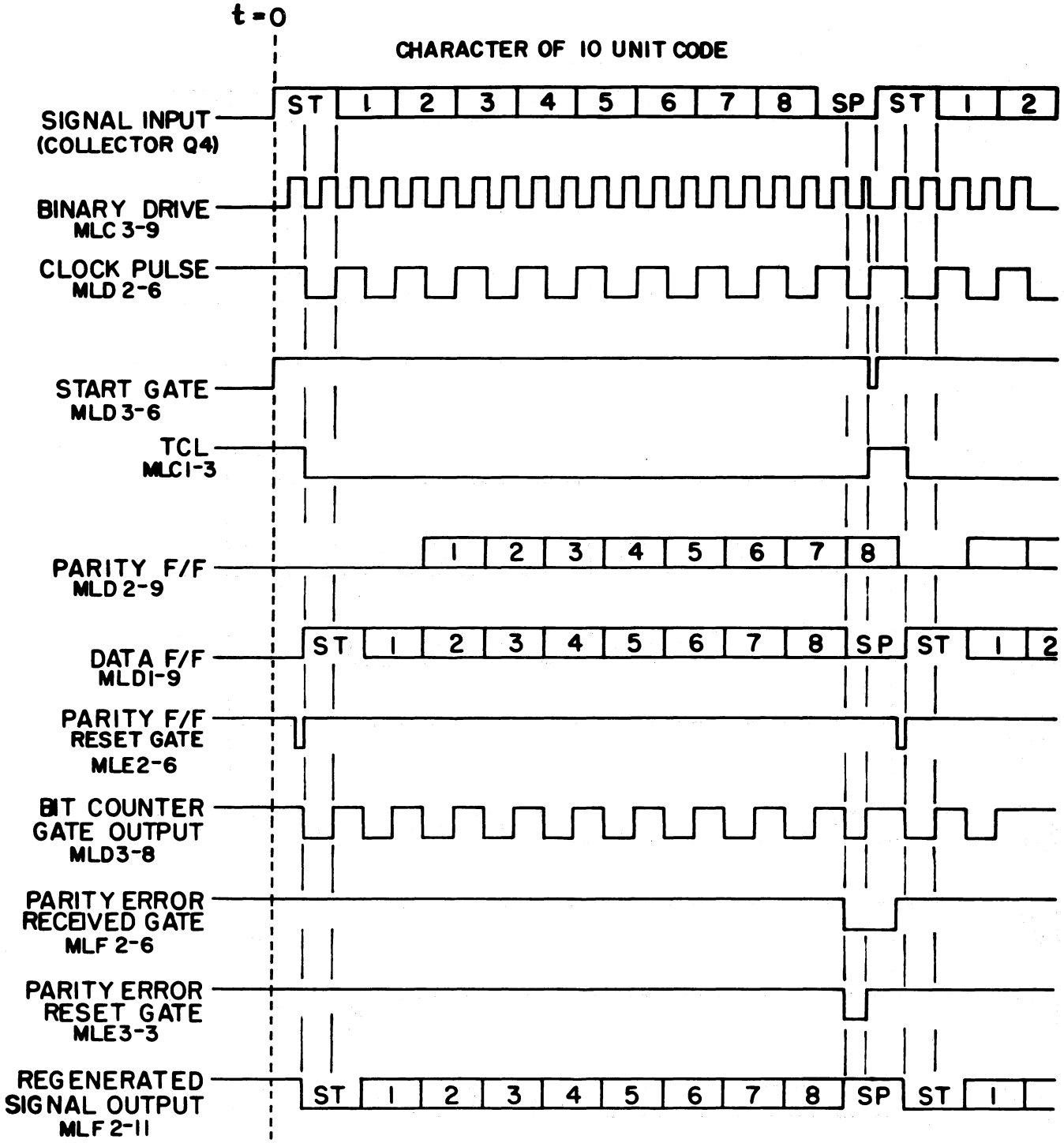


FIGURE 2

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

TIMING DIAGRAM
RECEIVING SIGNAL REGENERATOR
P/O 322062 RECEIVE CONTROL ASSEMBLY

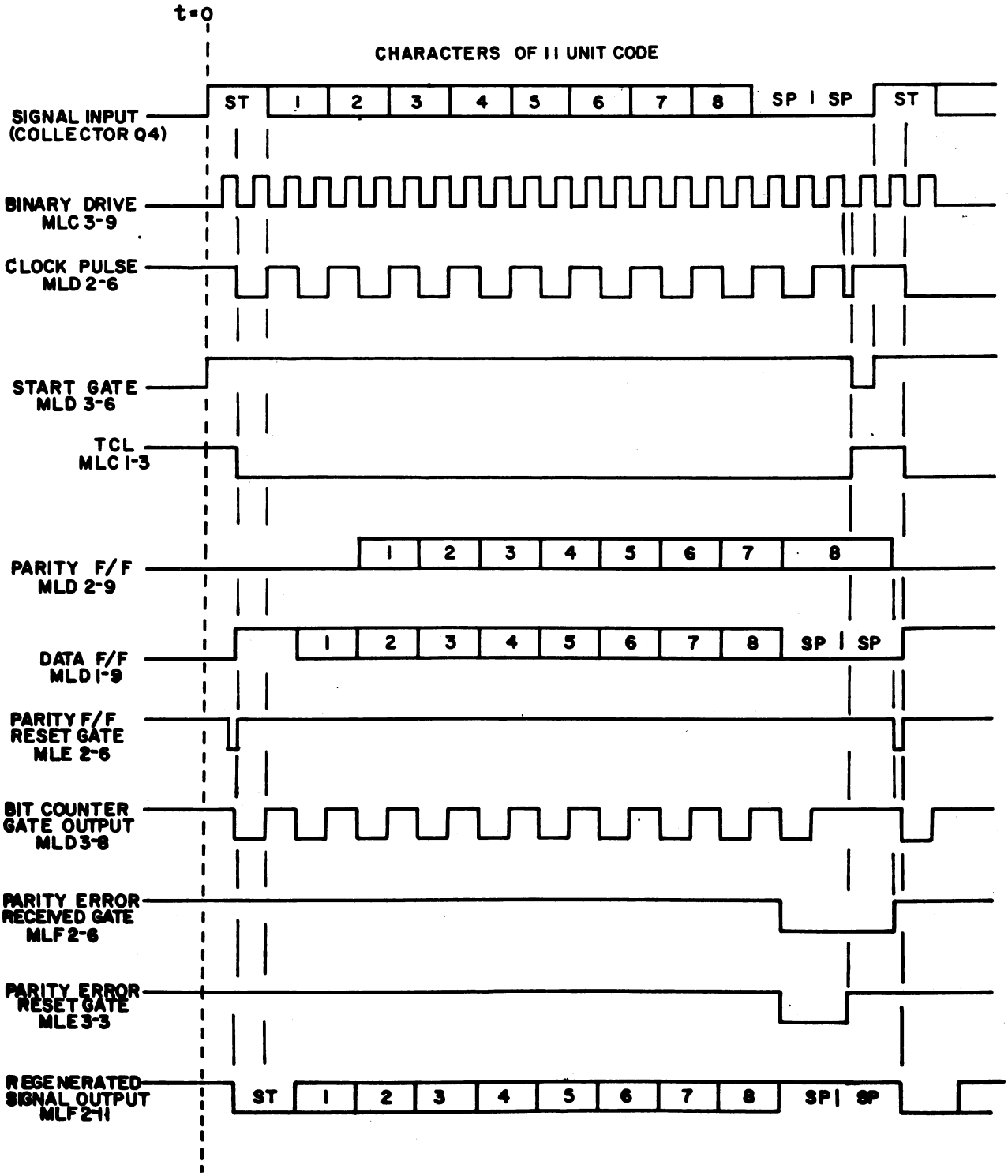


FIGURE 3

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

TIMING DIAGRAM
RECEIVING SIGNAL REGENERATOR
P/O 322062 RECEIVE CONTROL
ASSEMBLY.

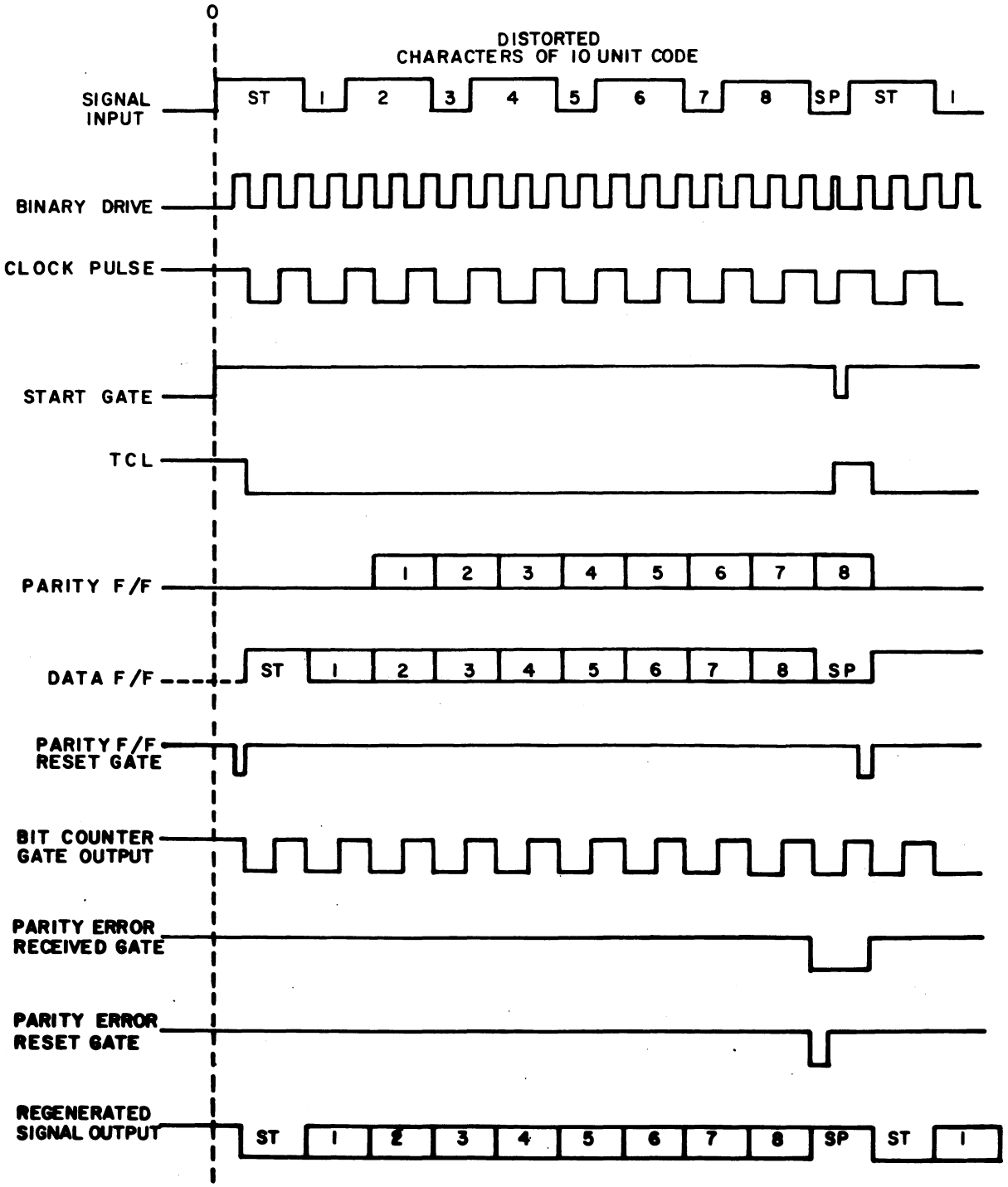
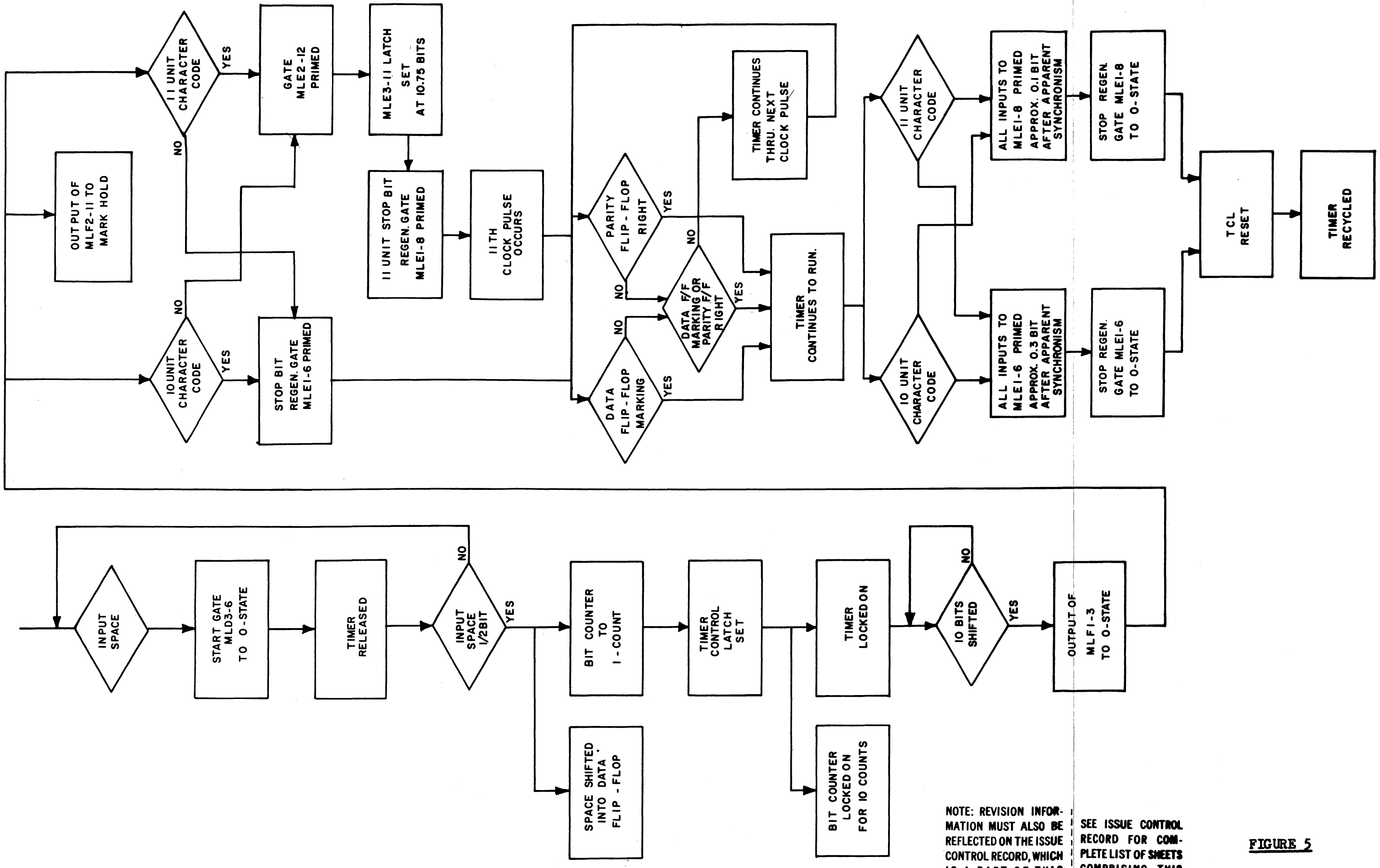


FIGURE 4

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

FLOW CHART
RECEIVING SIGNAL REGENERATOR
P/O 322062 RECEIVE CONTROL ASSEMBLY

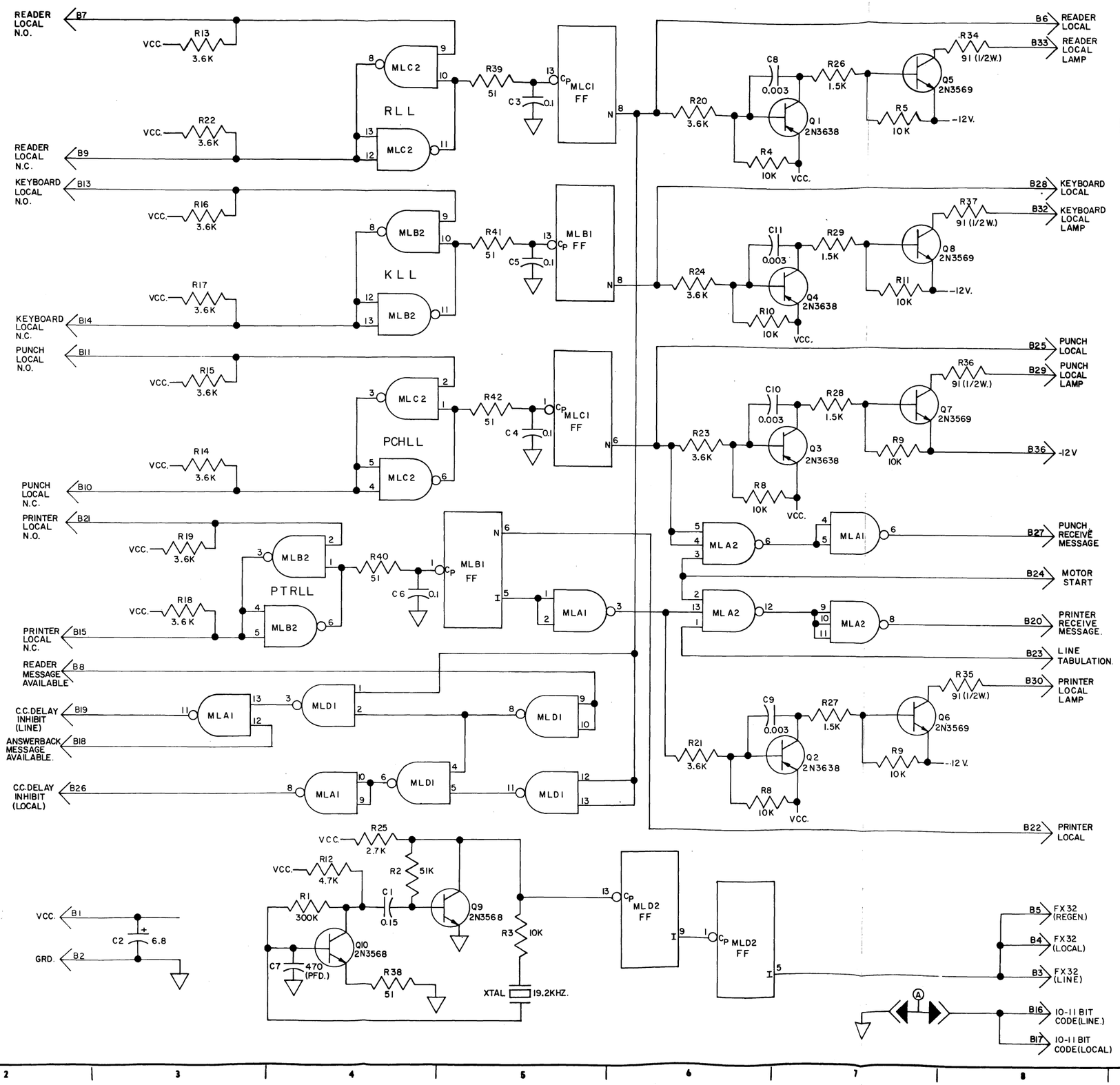


NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

FIGURE 5

NO.	NOTES.
1.	ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
4.	INDICATES FEMALE TERMINAL. INDICATES MALE TERMINAL. INDICATES CIRCUIT GROUND.
5.	REFER TO 322066 FOR ASSEMBLY INFORMATION.
6.	S-NUMBER: 61,515S
7.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD: MLA2 — ROW, COLUMN, INTEGRATED CIRCUIT
8.	THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVEL REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC AND 0V., RESPECTIVELY.
9	LOGIC NEGATION- A SMALL CIRCLE JOINED TO A LOGIG SYMBOL, INDICATES A LOGIC NEGATION.
10.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER THE GATE IS USED AS AN INVERTER.
11	VCC IS PROVIDED TO THE INTEGRATED CIRCUIT PACKAGE ON PIN 14 AND GROUND ON PIN 7, THIS APPLIES TO ALL PACKAGES.
12	REFER TO 8399WD FOR TRUTH TABLES.
13	OPTIONS: A – 10-11 BIT CODE, ADD STRAP FOR 10 BIT CODE.
14	REFERENCE CIRCUIT DESCRIPTION 8769WD-CD.
15	ABBREVIATIONS USED. C.C DELAY - CONTROL CHARACTER DELAY. N.O. - NORMALLY OPEN. N.C. - NORMALLY CLOSED. RLL - READER LOCAL LATCH. KLL - KEYBOARD LOCAL LATCH. PCHLL - PUNCH LOCAL LATCH. PTRLL - PRINTER LOCAL LATCH.



NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8386 WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R
2	10-22-68	96395

WDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D. SHEET 1

SCHEMATIC WIRING DIAGRAM FOR ASR MODE CONTROL.

APPROVALS	
D AND R	E OF M

E-NUMBER

PROD. NO. 8386 WD.

DATE 9-17-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. CHKD.

ENGD. C.A.Y. APPD.

TELETYPE CORPORATION

8386 WD

TC 484 (5-69)

WDP

CIRCUIT DESCRIPTION OF THE ASR MODE CONTROL CARD (ASSEMBLY NUMBER 322066)

TABLE OF CONTENTS

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NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

2

CIRCUIT DESCRIPTION OF THE ASR MODE CONTROL CARD (ASSEMBLY NUMBER 322066)

SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The 322066 Circuit Card Assembly is a mode control and set clock for Model 37 ASR sets operating at 150 wpm with 10 unit code (150 baud).

1.2 The modes provided on this assembly are:

A. KEYBOARD LOCAL (KBD LOCAL)

B. PRINTER LOCAL (PTR LOCAL)

C. PUNCH LOCAL (PCH LOCAL)

D. READER LOCAL (RDR LOCAL)

1.3 Each mode control circuit is associated with a switch and a 24V 30 ma lamp on the control panel located above the keyboard.

1.3.1 When the switch is lighted, it is in the "local" mode as indicated on the switch button, e.g., KBD LOCAL switch lighted means that the keyboard is in the "local" mode.

1.3.2 When the switch is not lighted, it is in the "on-line" mode, e.g., KBD LOCAL switch not lighted means that the keyboard is in the "on-line" mode.

2. GENERAL TECHNICAL DATA (All card pins appear on the "B"(non-component) side of card)

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2.1 Input Characteristics

The inputs to the assembly are positive nand type integrated Diode Transistor Logic (DTL) inputs. Each DTL input is approximately a 1.4 ma load to the device sinking current from it. At no time should any of these inputs be more positive than 8 volts or more negative than -.7 volts. Voltage levels represented by the 1-state (high) and 0-state (low) are approximately +6V and 0V respectively. A logic one (high) draws no current from the input of the logic element.

2.1.1 Keyboard Local Switch (N.O. Pin 13; N.C. Pin 14)

Mode switching (identical circuit for each mode). The momentary transfer mode switch (Pins 13, 14) generates a square pulse through a latch circuit, formed by a pair of gates, and into the toggle input of a J-K flip-flop. The flip-flop changes output state each time the mode switch is pressed. The device driving this input must be capable of sinking two DTL loads.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

2.1.2 Printer Local Switch (N.O. Pin 21: N.C. Pin 15)

See Section 2.1.1.

2.1.3 Punch Local Switch (N.O. Pin 11: N.C. Pin 10)

See Section 2.1.1.

2.1.4 Reader Local Switch (N.O. Pin 7: N.C. Pin 9)

See Section 2.1.1.

2.1.5 Motor Start (Pin 24)

This pin is low to start the printer and punch motors during "on-line" operation and is two DTL loads.

2.1.6 Line Tabulation (Pin 23)

This pin is low throughout any tabulation function which is started while the printer is "on-line" and high at all other times. The device driving this input must be capable of sinking one DTL load.

2.1.7 Reader Message Available (Pin 8)

This lead is low whenever the reader is operating. It is high at all other times. The device driving this input must be capable of sinking one DTL load.

2.1.8 Answer Back Message Available (Pin 18)

This lead is low throughout any Answer Back cycle. It is high at all other times. The device driving this input must be capable of sinking one DTL load.

2.2 Output Characteristics

2.2.1 Keyboard Local (F.F. Output Pin 28: Lamp Pin 32)

When the flip-flop output, MLB1 Pin 8 is low, the lamp associated with that mode is lighted by a lamp driver circuit Q4 and Q8 (Pin 32) which applies approximately 24 volts across the bulb.

The output of the flip-flop is also routed off the card to control other circuitry in the set and will be low during the "keyboard local" mode (Pin 28). This output is capable of driving 7 DTL loads.

2.2.2 Printer Local (F.F. Output Pin 22: Lamp Pin 30)

See Section 2.2.1.

2.2.3 Punch Local (F.F. Output Pin 25: Lamp Pin 29)

See Section 2.2.1.

WDP

2.2.4 Reader Local (F.F. Output Pin 6: Lamp Pin 33)

See Section 2.2.1.

2.2.5 Set Clock (Internal to Card)

The set clock is a crystal controlled multivibrator operating at 128 times the bit rate (19.2KHZ @ 150 baud). (See General Timing Diagram.)

2.2.6 Clock Pulse (Pins 3, 4, 5)

The set clock frequency is divided by four by a pair of flip-flops and is available as a clock pulse output of 32 times the bit rate and is capable of driving ten DTL loads.

2.2.7 10-11 Bit Code Selection (Pins 16, 17)

Strap A is provided to ground the 10 bit input lead on the electronic distributor used in the set. If this strap is removed, an 11 bit code will be generated, but a different crystal is required to obtain the correct bit rate as indicated in Section 2.2.5.

✓ 2.2.8 Control Character Delay Inhibit (Line) (Pin 19)

This output in the 0 state inhibits the line distributor from pausing for one character interval, following the transmission of a control character. This output is capable of driving eight DTL loads.

✓ 2.2.9 Control Character Delay Inhibit (Local) (Pin 26)

This output in the 0 state, inhibits the local distributor from pausing for one character interval, following the transmission of a control character. This output is capable of driving eight DTL loads.

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✓ 2.2.10 Printer Receive Message (Pin 20)

A low on this pin indicates to the printer that its motor should be started. This pin will be low when in the "printer local" mode or during tabulation on line, or when "motor start" is low. This output is capable of driving eight DTL loads.

✓ 2.2.11 Punch Receive Message (Pin 27)

A low on this pin indicates to the punch that its motor should be started. This pin will be low when in the "punch local" mode, or when "motor start" is low. This output is capable of driving eight DTL loads.

2.3 Mechanical Requirements

The 322066 card assembly is a standard 5-3/4 inch by 4-1/4 inch 36-pin circuit card which is inserted into a 36-pin edge card connector.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR [redacted] PLETE LIST OF SHEETS COMPRISING W.D.

2.4 Power Supply Requirements

Vcc (DC)	Current Maximum
+5.0V to +6.6V (+5.25V Nom.)	180 ma
+11.65V to +13.75V (+12.5V Nom.)*	200 ma
-11.13V to -13.88V (-12.5V Nom.)	200 ma

* +12.5 Volts is used for the lamps.

2.5 Temperature Range

The ambient temperature range for operation is from 0°C to 70°C in free air. Non-operating storage temperature is from -40°C to 70°C.

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SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly and schematic drawings 322066 (MC066)and 8386 WD.

1.2 Logic symbols and truth table 8399 WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 Mode Switching

Each mode switch is a momentary contact transfer switch assembly (break before make) containing a lamp indicator. During mode change, a normally closed contact opens first and enables the input to the associated gate, which is part of a latch arrangement. The input of the gate is held low, however, by the other half of the latch associated with the normally open contact. Next, the normally open contact closes, driving the input of its associated gate low and switching the output high. The output of the gate associated with the normally closed contact then switches low, causing a high to low transition on the input to the J-K flip-flop, changing its state. (The output of the J-K flip-flop changes state each time a high to low transition occurs on the input.) See the timing diagram on Figure 1.

When the mode switch is released, the normally open contact returns to its open condition and enables the input to its associated gate. Next, the normally closed contact returns to its closed condition, putting a low input on its gate, which returns the output of the latch to a high. This low to high transition occurs on the input to the J-K flip-flop, but has no effect on its output.

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The output of the flip-flop drives a lamp through an amplifier. The output also leaves the card to control other circuitry.

2.2 Lamp Driver

A low input to a lamp driver provides a current path through the 3.6K resistor and from the base of a PNP transistor. The transistor turns on, and provides a bias current through the 1.5K ohm resistor to turn on the NPN transistor. This transistor acts as a switch connecting the lamp from +12.5 volts supply, through a 91 ohm limiting resistor, to the -12.5 volt supply. Thus the lamp is turned on.

2.3 Set Clock

2.3.1 The set clock is a crystal controlled, astable multivibrator composed of Q9 and Q10 operating at 128 times the bit rate. The transistors are arranged as grounded emitter inverting amplifiers with R38 providing some stabilization and feedback for Q10 and R2 providing bias for Q9. R1 provides collector feedback and base bias current for Q10. C1 couples the output of Q10 to the base

input of Q9. A quartz crystal provides feedback from the collector of Q9 through current limiting resistor R3 and into the base of Q10 at the critical frequency of the crystal. A negative transition on the Q10 base momentarily turns it off, thus causing a positive transition to be coupled by C1 into the Q9 base, momentarily turning it on and causing a negative transition to be coupled through the crystal and again momentarily turn Q10 off. C1 decouples oscillations of higher harmonics that might occur due to stray capacitances associated with the crystal.

The output of Q9 is also connected to the input of the J-K flip-flop where every negative transition causes a change in the state of its output, thus dividing the frequency in half. This signal is again divided in half by the other J-K flip-flop. The clock signal leaves the card as Fx32.

2.4 Motor Control

Punch and printer motors are turned on whenever the units are either in the "local" mode, or when a message is being received "on-line". Additionally, the typing unit motors are held "on" while tabulating "on-line", even though a message has been completed.

2.4.1 A "motor start" signal, signifying that a message is present "on-line", enters the assembly and is gated with the punch local signal and is then inverted, so that the "Punch Receive Message" output will be low when a "motor start" signal is received, or when the punch is in the "local" mode.

2.4.2 The "motor start" lead is also gated with the "printer local" signal and the "line tabulation" signal and is then inverted. Thus the "Printer Receive Message" output will be low when a "motor start" signal is received, when the printer is in the "local" mode, or while "line tabulation" is taking place.

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2.5 Control Character Delay Inhibit

The control character delay is a 13 bit marking interval following the transmission of every control character. This delay is necessary to provide sufficient time for the printer to execute any one of its control functions before beginning to receive the next character.

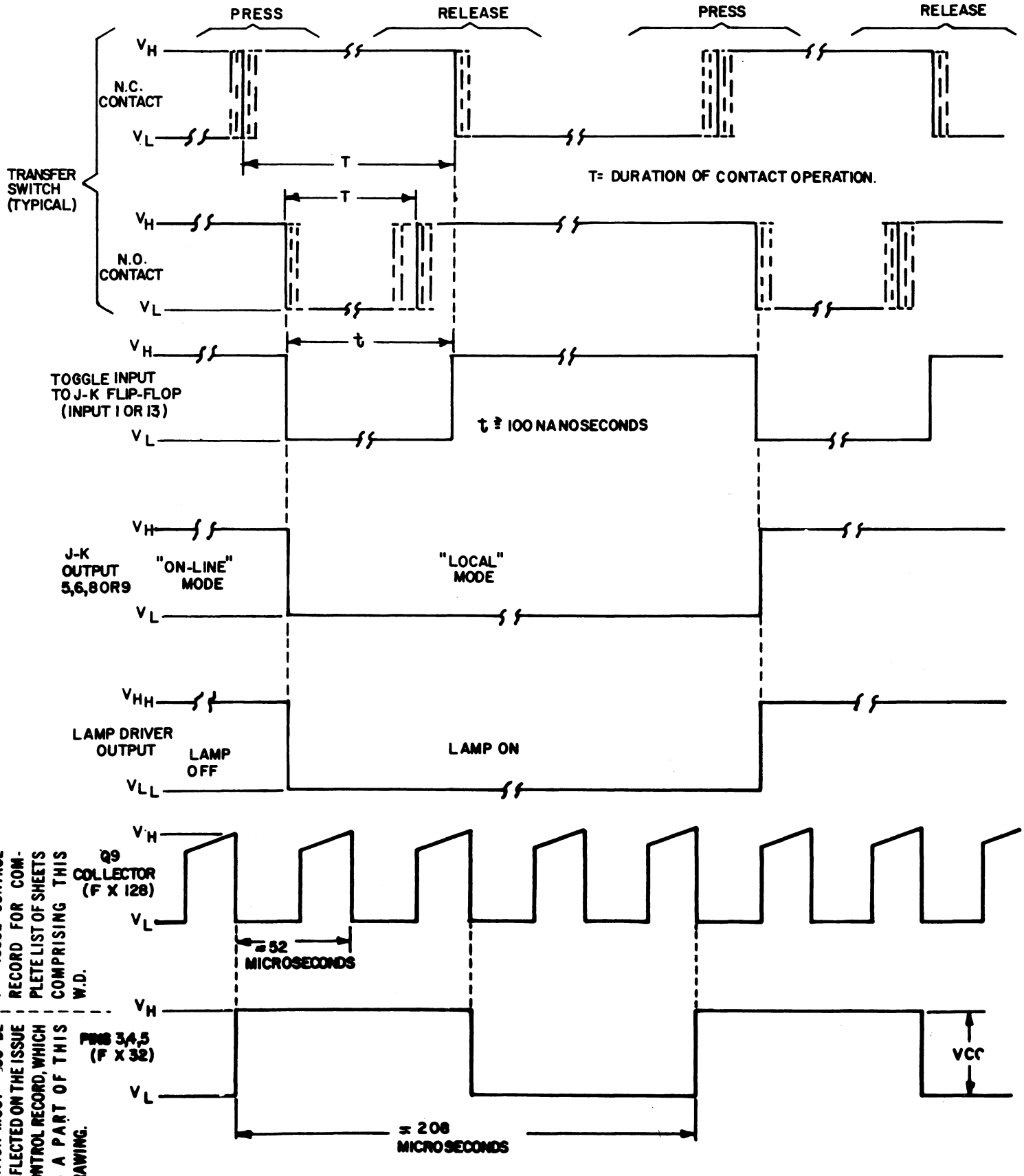
Low states on Pins 19 and 26 inhibit the delay feature on the line and local distributors respectively.

The delay is disabled during all keyboard transmission. It is enabled whenever the reader or Answer Back is sending. With the reader in the idle condition, Reader Message Available Pin 8 is high keeping Inputs 2 and 4 of MLD1 low. The Answer Back also idle, Answer Back Message Available Pin18 is high. Under these conditions both Pins 19 and 26 are low disabling the delay during either line or local keyboard transmission.

2.5 (Continued)

Answer Back Message Available Pin 18 switching low at the start of the Answer Back message forces MLA1-11 high enabling the delay for all control characters sent from the Answer Back. With the reader operating in the local mode both inputs to MLD1-6 will be high forcing Pin 26 high, thereby enabling the delay for all control characters sent from the reader. In this mode MLD1-1 is low disabling the CC delay for on line operation of the keyboard. Switching the Reader to the on line mode reverses the conditions of MLD1-1 and 5 which in return reverses the states of Pins 19 and 26 once reader MA comes on indicating the start of a Reader Message.

GENERAL TIMING DIAGRAM



NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

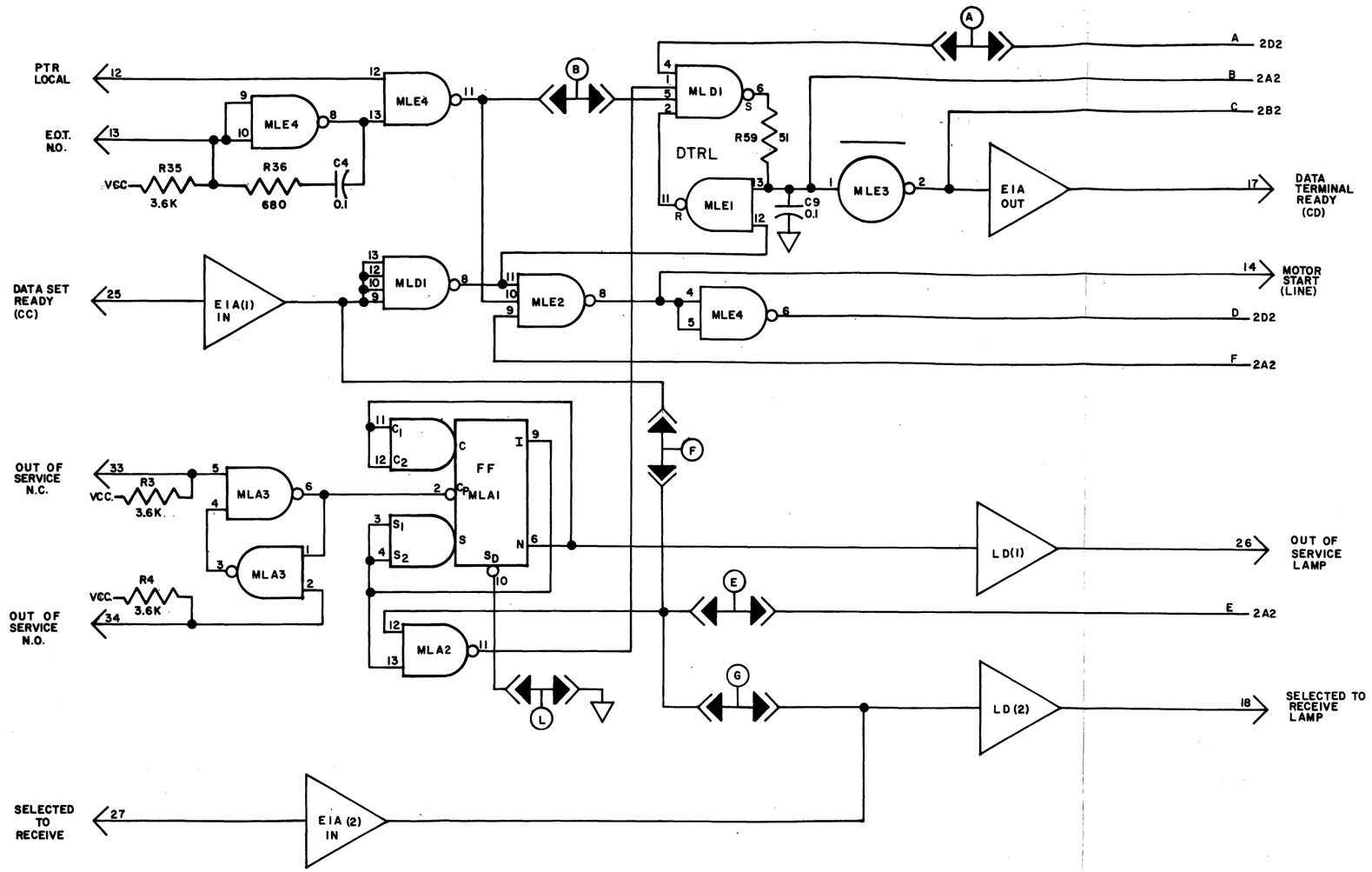
ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

FIGURE 1

NO.	NOTES
1.	ALL VOLTAGES DC. UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
4.	INDICATES FEMALE AND INDICATES MALE TERMINALS
5.	REFER TO 322068 FOR ASSEMBLY INFORMATION.
6.	S NUMBER: 61,521S.
7.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD: ML D 2 — ROW, COLUMN, INTEGRATED CIRCUIT
8.	CROSS REFERENCE NOTATION ON SCHEMATIC 3 B 4 — ROW, COLUMN, SHEET
9.	LOGIC NEGATION: A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
10.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER, THE GATE IS USE AS AN INVERTER.
11.	VCC IS PROVIDED TO THE INTEGRATED CIRCUIT PACKAGE ON PIN 14 AND GROUND ON PIN 7, THIS APPLIES TO ALL PACKAGES.
12.	SEE 8399 WD. FOR TRUTH TABLES.
13.	THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC. AND 0V., RESPECTIVELY.
14.	CARD OPTIONS: STRAP MUST BE ADDED TO OBTAIN OPTION.

STRAP		OPTION
A	—	ALARM DISCONNECT.
B	—	EOT DISCONNECT.
C	—	PRIVATE LINE MOTOR CONTROL DISCONNECT.
D	—	PRIVATE LINE MOTOR CONTROL ENABLE.
E	—	PRIVATE LINE OUT OF SERVICE ENABLE.
F	—	DATAPHONE OUT OF SERVICE ENABLE.
G	—	PRIVATE LINE OUT OF SERVICE ENABLE.
H	—	BREAK DETECT DISABLE.
K	—	SEND BREAK ON PARITY ERROR.
L	—	OUT OF SERVICE DISABLE.
M	—	SEND BREAK DISABLE
Y	—	PROCEED CONTROL DISABLE

15.	REFERENCE CIRCUIT DESCRIPTION. 8388WD-CD.
16.	ABBREVIATIONS USED: MCL - MOTOR CONTROL LATCH. MTL - MARK TIME LATCH. RIL - RECEIVE INTERRUPT LATCH. PCL - PROCEED CONTROL LATCH. DTRL - DATA TERMINAL READY LATCH.
17.	INDICATES CIRCUIT GROUND.



NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8388WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 1

SCHEMATIC WIRING DIAGRAM FOR CHANNEL CONTROL

APPROVALS	
D AND R	E OF M

E-NUMBER

PROD. NO. 8388 WD.

DATE 3-29-68

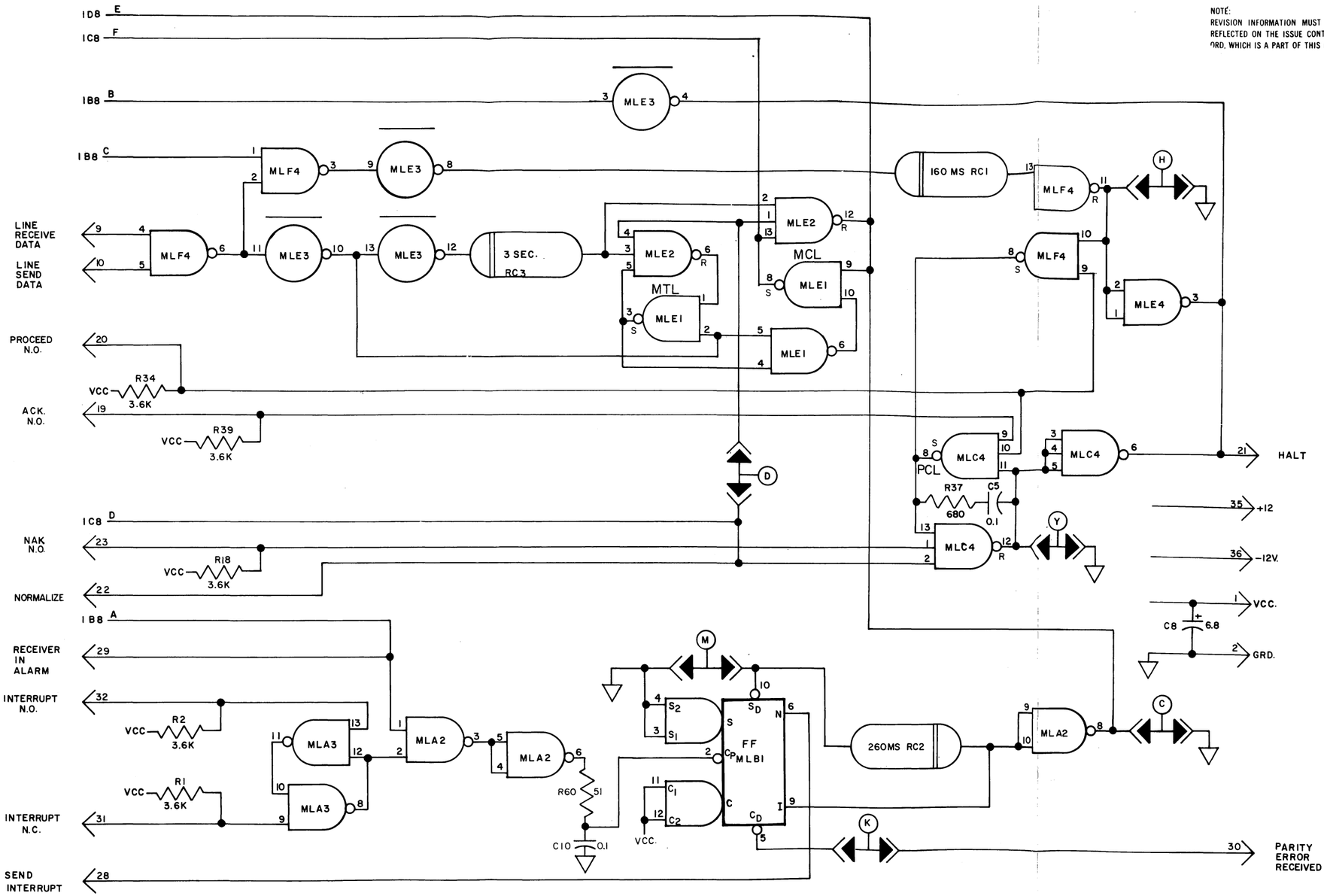
P.D. FILE NO. G-A354AA

DRAWN W.P.B.	CHKD.
ENGD. C.A.Y.	APPD.

TELETYPE CORPORATION

8388WD

TC 484 (3-68)



NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8388WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R
2	2-21-69	96903

WDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 2

SCHEMATIC WIRING DIAGRAM FOR CHANNEL CONTROL

APPROVALS	
D AND R	E OF M
W.K	

E-NUMBER

PROD. NO. 8388 WD.

DATE 3-29-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. CHKD.

ENGD. C.A.Y. APPD.

TELETYPE CORPORATION

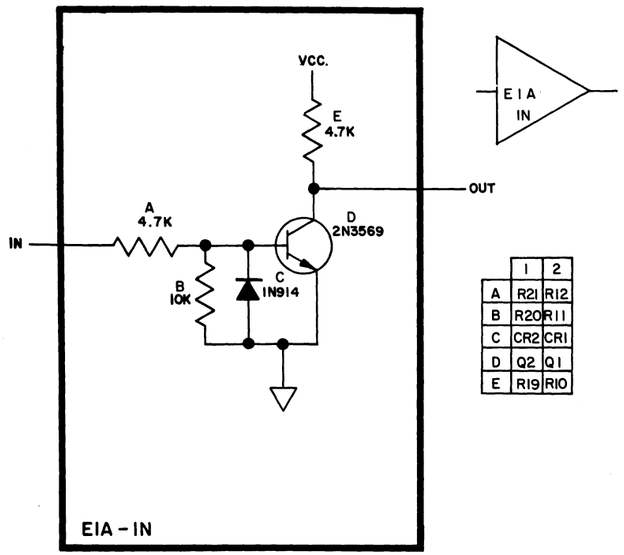
8388WD

2

TC 434 (3-68)

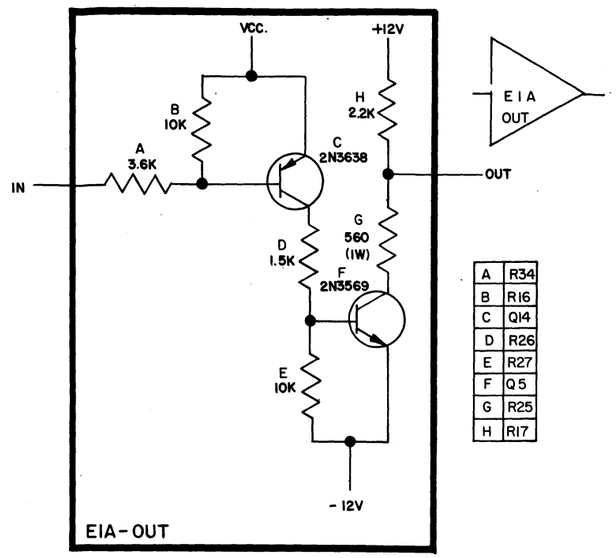
NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8388WD		
REVISIONS		
ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R



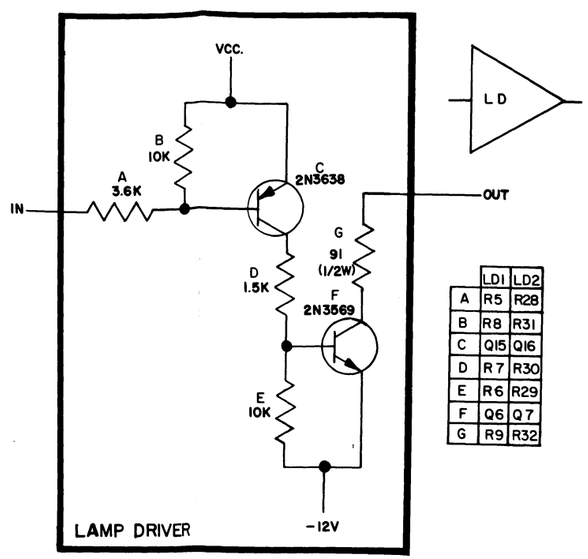
EIA IN

	1	2
A	R21	R12
B	R20	R11
C	CR2	CR1
D	Q2	Q1
E	R19	R10



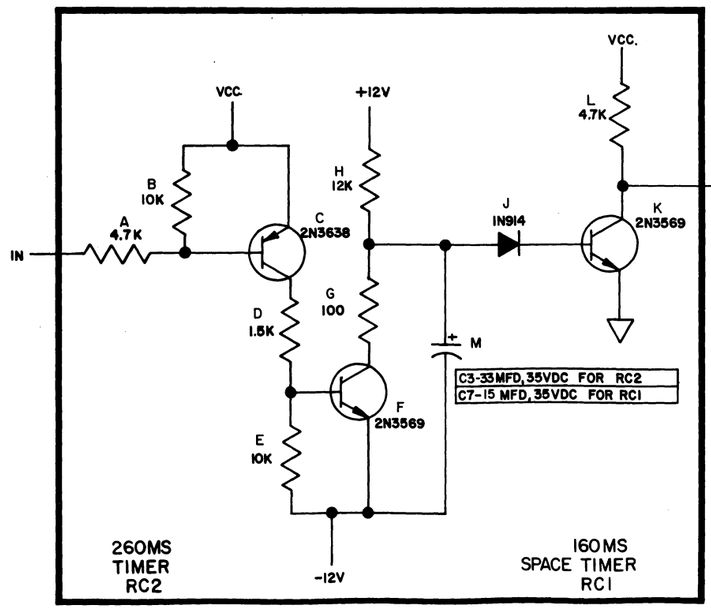
EIA OUT

A	R34
B	R16
C	Q14
D	R26
E	R27
F	Q5
G	R25
H	R17



LD

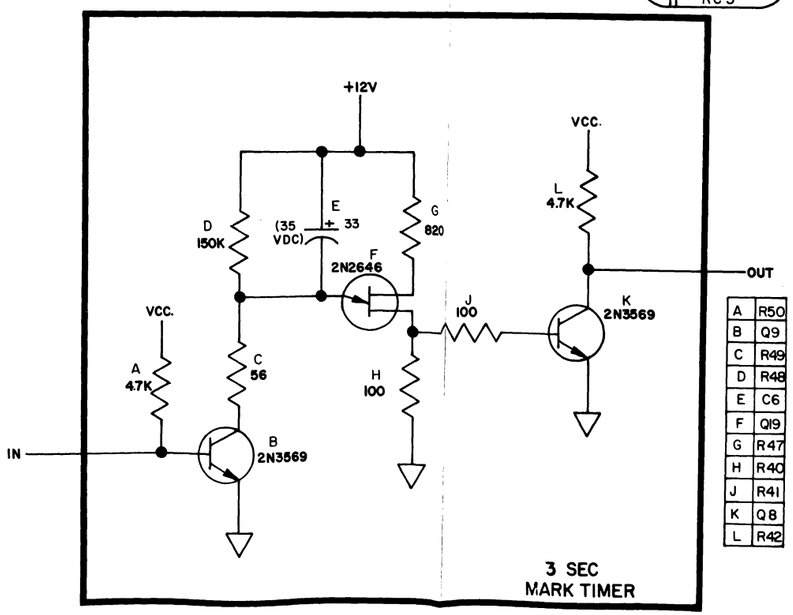
	LD1	LD2
A	R5	R28
B	R8	R31
C	Q15	Q16
D	R7	R30
E	R6	R29
F	Q6	Q7
G	R9	R32



160MS-RC1
260MS-RC2

	RC1	RC2
A	R53	R22
B	R51	R24
C	Q17	Q13
D	R45	R15
E	R46	R13
F	Q10	Q3
G	R44	R14
H	R43	R16
J	CR4	CR3
K	Q11	Q4
L	R52	R23
M	C7	C3

3 SEC.
RC3



A	R50
B	Q9
C	R49
D	R48
E	C6
F	Q19
G	R47
H	R40
J	R41
K	Q8
L	R42

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 3

SCHEMATIC
WIRING DIAGRAM
FOR
CHANNEL
CONTROL

APPROVALS	
D AND R	E OF M
1-2-68	

E-NUMBER	
PROD. NO.	8388WD.
DATE	1-2-68
P.D. FILE NO.	G-A364AA
DRAWN R J P	CHKD.
ENGD. C A Y	APPD.

TELETYPE
CORPORATION

8388WD

TC 434 (5-63)

CIRCUIT DESCRIPTION OF THE CHANNEL CONTROL CARD (ASSEMBLY NUMBER 322068)

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NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

1

CIRCUIT DESCRIPTION OF THE CHANNEL CONTROL CARD (ASSEMBLY NUMBER 322068)

SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The 322068 Circuit Card Assembly provides information to the data set or other line interface unit about the receiving status of the terminal and accepts information about the line connection status of the terminal.

1.2 Additional Features

Timed Send interrupt generation

Timed Receive interrupt detection

On-Line Motor start control for switched or non-switched service

On-Line transmission control

Out of service, do not answer

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

The inputs to the assembly are positive nand type integrated Diode Transistor Logic (DTL) inputs. Each DTL input is approximately a 1.4 ma load to the device sinking current from it. At no time should any of these inputs be more positive than 8 volts or more negative than - .7 volts. Voltage levels represented by the 1-state (high) and 0-state (low) are approximately +6V and 0V respectively. A logic one (high) draws no current from the input of the logic element. 49

2.1.1 Line Receive Data (Pin 9)

This pin is high when data is not being received or when the signal line is MARKING, and goes low when the signal line is SPACING. Interrupt, a space on line of at least 195 m.s., will appear on this pin.

2.1.2 Line Send Data (Pin 10)

This pin is high when data is not being sent or when a mark is being sent, and will go low when space is sent on line.

2.1.3 Proceed N.O. (Pin 20)

This lead is normally high and goes low when the proceed switch is operated. This low will reset the Proceed Control Latch (PCL).

2.1.4 ACK N.O. (Pin 19)

This lead is normally high and goes low when an ACK character is detected in the printer function box. This low will reset the Proceed Control Latch (PCL).

2.1.5 NAK N.O. (Pin 23)

This lead is normally high and goes low whenever a NAK character is detected in the printer function box. This low will set the Proceed Control Latch (PCL).

2.1.6 Receiver in Alarm (Pin 29)

This lead is normally high and goes low when a line receiver goes into an alarm condition. A low on Pin 29 starts a SEND INTERRUPT signal and resets the Data Terminal Ready Latch (DTRL).

2.1.7 Interrupt Switch (N.O. Pin 32)(N.C. Pin 31)

These pins accept a break-before-make transfer switch, with the common terminal grounded. Operating the switch starts a send interrupt signal.

2.1.8 Parity Error Received (Pin 30)

A low on this pin starts a send interrupt signal.

2.1.9 Printer Local (Pin 12)

This pin must be made low when the printer function box is "off-line" (local).

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2.1.10 EOT N.O. (Pin 13)

This pin must be made low momentarily when the ASCII character EOT is detected by the printer function box.

2.1.11 Data Set Ready (Pin 25) (EIA Lead CC)

The voltage, current, impedance and logic characteristics of this lead are defined by EIA Specification RS232B.

2.1.12 Out of Service Switch (N.O. Pin 34) (N.C. Pin 33)

These pins accept a break-before-make transfer contact with grounded common terminal. Operating the switch turns on the out of service lamp, and causes the line interface unit (e.g. Dataphone Data Set) not to answer any calls.

2.1.13 Selected to Receive (Pin 27)

The voltage, current, and impedance characteristics of this lead are defined by Section 4 of EIA Specification RS232B.

2.1.13 (Continued)

When the lead is "ON", the set will be prepared to receive a message and the "selected to receive" lamp will light.

2.2 Channel Control Outputs

2.2.1 Normalize (Pin 22)

This lead is low when there is no on-line call in process. The lead is used to restore circuits affecting on-line operation to a pre-selected "Normal" state after a call.

2.2.2 Send Interrupt (Pin 28)

This lead goes low for approximately 200 to 350 m.s. when the SEND INTERRUPT circuit is operated.

2.2.3 Halt (Pin 21)

This lead goes low when sending on-line is not permitted.

2.2.4 Selected to Receive Lamp (Pin 18)

See Section I, Paragraph 2.1.13 above.

2.2.5 Out of Service Lamp (Pin 26)

See Section I, Paragraph 2.1.12 above.

2.2.6 Motor Start (Pin 14)

This pin goes low when a call is in process, and is used to start all set motors. 151

2.2.7 Data Terminal Ready (Pin 17) (EIA Lead CD)

The voltage, current, impedance, and logic characteristics of this lead are defined by EIA Specification RS232B.

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly and Schematic Drawing 322068 (MC068) and 8388WD, respectively.

1.2 Logic symbols and truth tables per 8399WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 MOTOR CONTROL

The MOTOR START lead (Pin 14) low, starts all set motors. The conditions permitting "MOTOR START" are variable by strap option on the channel control card.

Output 8 of MLE2 controls "MOTOR START" and will be low only when Inputs 9, 10 and 11 of MLE2 are high.

MLE2 Input 9 controlled by MCL Section II, Paragraph 2.2.3 below
MLE2 Input 10 controlled by EOT Section II, Paragraph 2.2.2 below
MLE2 Input 11 controlled by DSR Section II, Paragraph 2.2.1 below

2.2 Switched Service Motor Control

In switched service, "MOTOR START" is controlled by "DATA SET READY" Pin 25 (EIA Lead CC). If the set motors are to be stopped or kept from starting by some condition in the terminal, "DATA TERMINAL READY" (Pin 17 - EIA Lead CD) will be turned off. The line interface unit must recognize DTR off as a request for "Disconnect" when DSR is on, and as a request for "DO NOT ANSWER" when DSR is off.

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2.2.1 DATA SET READY (DSR) (EIA LEAD CC)

When Pin 25, "DATA SET READY" is high (per EIA Specification RS232B), amplifier A-1 is turned on, holding Inputs 9, 10, 12 and 13 of MLD1 low. Output 8 of MLD1 drives Input 11 of MLE2 high.

If Inputs 9 and 10 of MLE2 are also high, "MOTOR START" (Pin 14) will turn on (low).

Amplifier A-1 output is also connected to Strap F, to control the "OUT OF SERVICE" option. See Section II, Paragraph 3.2.3 below.

2.2.2 End of Transmission (EOT)

Input 10 of MLE2 will be low during the time that "EOT N.O." (Pin 13) is low and "PRINTER LOCAL" (Pin 12) is high. If Strap "B" is installed, the same signal will reset DTRL, turning off "DATA TERMINAL READY" (Pin 17 - EIA Lead CD).

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2.2.3 Motor Control Latch (MCL)

For switched service, MCL is held reset, by installing Strap C, holding Input 9 of MLE2 high.

2.3 Private Line Motor Control (Non-Switched Service)

In non-switched service, DSR (Pin 25) may be on continuously, indicating that the line interface unit is always ready to operate. The set motors will run continuously.

If this condition is undesirable, the optional idle line motor turn off circuit may be enabled by removing Straps C, F and M, and installing Straps D and E.

2.3.1 Data Set Ready

The line interface unit should keep Data Set Ready (Pin 25) ON continuously, keeping Input 11 of MLE2 high (See Section II, Paragraph 2.2.1 above).

2.3.2 End of Transmission (EOT)

Output 11 of MLE4 will be momentarily low when EOT is detected (See Paragraph 1.12 above). Input 10 of MLE2 will be low, turning off "MOTOR START" (Pin 14) and turning on "NORMALIZE" (Pin 22) through MLE4 Output 6. Strap "D", installed, allows this signal to set MCL and MTL. MCL, Set, holds Input 9 of MLE2 low, keeping "MOTOR START" (Pin 14) off.

2.3.3 Idle Line Turn-Off

Timer E, nominally 3 seconds, sets the MARK TIMER LATCH (MTL) and the MOTOR CONTROL LATCH (MCL) when timed out. MCL, Set, holds Input 9 of MLE2 low, keeping "MOTOR START" (Pin 14) off. Timer E is saved (kept from timing out), by low (Spacing) signals on Pin 9, "LINE RECEIVE DATA", or Pin 10 "LINE SEND DATA". Either of these low inputs will force Output 6 of MLF4 high, Output 10 of MLE3 low, and Output 12 of MLE3 high. (MLE3 Output 12, low, shunts the base of Q9, allowing Timer E to time out. MLE3-12, high, allows Q9 to turn on, with base current through R50. The high state of MLE3 Output 12 will be voltage limited to the base emitter drop of Q9, about 0.6 volts. Measurements to determine the "ON" or "OFF" state of inverter MLE3-12 must be made at MLE3 Input 13). 153

2.3.3.1 Automatic Motor Turn Off

Uninterrupted marking (high) on line data Pins 9 and 10 for 3 seconds (nominal) allows Timer E to time out, setting MTL and MCL. Input 9 of MLE2 is held low by MCL Set and the motors stop.

2.3.3.2 Re-start from Automatic Stop

2.3.3.2.1 REMOTE Re-Start

A spacing signal (low) on either Pin 9 or Pin 10 resets MTL and saves Timer E. MTL, Reset, places a high on Input 4 of MLE1. When Pin 9 "LINE RECEIVE DATA" and Pin 10 "LINE SEND DATA" are both high, Input 5 of MLE1 will also be high. With Inputs 4 and 5 of MLE1 high, Output 6 of MLE1 will go low, resetting MCL. MCL Reset places a high on Input 9 of MLE2, and the set motors will start.

Since the set motors are not started until the signal line (Pins 9 and 10) is again marking in both directions, the receiving devices at the called terminal will detect a single ASCII "DELETE" character.

2.3.3.2.2 LOCAL Re-Start

The set motors are re-started in an originating terminal by sending INTERRUPT.

When INTERRUPT is sent, (see Section II, Paragraph 5 below) Inputs 9 and 10 of MLA2 are high, forcing Output 8 low, and resetting MCL. MCL Reset places a high on Input 9 of MLE2. If EIA Lead CC (Data Set Ready) is not off, and EOT is not received, the set motors will start. The receivers in the calling terminal do not detect spacing on line when INTERRUPT is sent. No "Hit" characters are generated.

The called station set motors are started on RECEIVE INTERRUPT as described in Section II, Paragraph 2.3.3.2.1 above. Receivers in the called station will detect one ASCII "Delete" character.

3. TERMINAL STATUS (DATA TERMINAL READY)

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Data Terminal Ready (Pin 17 - EIA Lead CD) is driven by amplifier B. A low input to amplifier B drives Pin 17 negative, indicating to the line interface unit that the terminal is not ready to operate.

3.1 General

Three optional conditions are available to turn off Data Terminal Ready

Receiver in Alarm	Section II, Paragraph 3.2.1
EOT	Section II, Paragraph 3.2.2
Out of Service	Section II, Paragraph 3.2.3

Any one of these conditions will reset DTRL, placing a high on Input 1, of MLE3, forcing Output 2 of MLE3 and the input of amplifier B low. This turns off Data Terminal Ready. The reset condition must be removed before DTRL can be set. DTRL is set by a low on Output 8 of MLD1, which is low when Data Set Ready, EIA Lead CC, Pin 25 is OFF (Negative on Pin 25).

If Data Set Ready (Pin 25) is on continuously, as in non-switched service, DTRL cannot be set and none of the terminal status options should be used.

3.2. Additional Outputs

DTRL Set output is connected to Input 3 of MLE3 to perform a transmitter control function. See TRANSMITTER CONTROL, Section II, Paragraph 4 below.

Output 2 of MLE3 is connected to Input 1 of MLF4 to inhibit detection of RECEIVED INTERRUPT when Pin 17, Data Terminal Ready, is low.

3.2.1 Receiver in Alarm

RECEIVER IN ALARM (Pin 29) is low when the condition of the line receivers prevents terminal operation, e.g. Paper out etc. See Specification Number 61434 for a description of the conditions on RECEIVER IN ALARM.

Strap A, installed, permits RECEIVER IN ALARM, low, to reset DTRL.

Pin 29, low, also initiates SEND INTERRUPT. See Section II, Paragraph 5 below for a description of the SEND INTERRUPT circuit.

3.2.2 EOT Received On Line (See Section II, Paragraph 2.2.2)

3.2.3 Out of Service

3.2.3.1 General

The Out of Service option allows the operator to disable the terminal. This may be desirable during routine maintenance. (Changing forms, printer ribbons, etc.)

The option is enabled by removing Strap "L", and is operative only when the terminal is idle. The idle condition of the terminal is determined on the basis of strap options depending on the type of service in which the terminal is being used.

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3.2.3.2 Operation

The lighted "OUT OF SERVICE" transfer switch is connected to Pins 33 and 34. Cycling the switch produces a single positive to negative transition on the toggle input of the "OUT OF SERVICE" flip-flop, MLA1 Input 2, causing the flip-flop to change state. When Output 6 of MLA1 is low, the "OUT OF SERVICE" lamp will be lighted.

The inverse output of MLA1, Output 9, is connected to Input 13 of MLA2 and will be high when the "OUT OF SERVICE" lamp is lit.

When Input 12 of MLA2 is also high, Output 11 of MLA2 will be forced low, resetting DTRL. DTRL, reset, turns off Data Terminal Ready (Pin 17).

Three straps are provided for optional control of MLA2 Input 12, depending on the type of service in which the terminal is being used.

3.2.3.2 (Continued)

Strap F installed: "OUT OF SERVICE" reset DTRL when "Data Set Ready" EIA lead CC, Pin 25, is off. Used in switched service.

Strap G installed: "OUT OF SERVICE" resets DTRL when "Selected to Receive" Pin 27, is off. Used in some non-switched services.

Strap E installed: "OUT OF SERVICE" resets DTRL when MCL is set. The set motors are stopped when MCL is set. Used with idle line turn off, in non-switched service.

4. TRANSMITTER CONTROL

HALT, Pin 21 is provided to inhibit on line transmission. The signal acts on the send control circuit (8382WD-CD;KSR sets or 8381WD-CD; ASR Sets) to light the "PROCEED" lamp when transmission is permitted.

The "HALT" signal should inhibit all transmitting devices except the answerback. This allows the answerback in a called terminal to generate the character which removes "HALT" (ACK).

"HALT", Pin 21 may be operated by the RECEIVE INTERRUPT circuit; see Section II, Paragraph 6 below.

4.1 "HALT", Pin 21, is controlled by the PROCEED CONTROL LATCH, (PCL). When PCL is set, Inputs 3, 4, and 5 of MLC4 are high and Output 6 is low, holding "HALT", Pin 21, low. PCL, reset, forces MLC4 Output 6 high, but "HALT" Pin 21 may be held low by "RECEIVE INTERRUPT". See Section II, Paragraph 6 below.

4.2 PCL Set (HALT in Effect)

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4.2.1 NAK

Detection of the ASCII character NAK causes a contact closure on Pin 23, "NAK N.O.", setting PCL.

4.2.2 NORMALIZE

The "NORMALIZE" output (Pin 22) is derived from the Motor Start lead Pin 14. When Motor Start is high, indicating no MOTOR START, Inputs 4 and 5 of MLE4 are high and Output 6 of MLE4 is low, indicating "NORMALIZE". NORMALIZE sets PCL.

4.2.3 Received interrupt- Detection of interrupt signal sets PCL.

4.3 Proceed Control Latch (PCL) Reset (HALT not in effect)

4.3.1 ACK

Detection of the ASCII character ACK causes a contact closure on Pin 19, "ACK N.O.", resetting PCL.

4.3.2 PROCEED Switch

The normally open PROCEED switch, connected to Pin 20, when operated, resets PCL Operation of the PROCEED switch assumes that "HALT" (Pin 21) will go high.

4.4 PCL Disable

PCL may be held reset by installing Strap Y. This will prevent operation of "HALT" by PCL. Install Strap H to inhibit operation of HALT by RIL.

5. SEND INTERRUPT

The INTERRUPT switch, a break-before-make transfer switch, is connected to Pins 31 and 32. Cycling the switch produces a single positive to negative transition on Input 2 of MLA2. This transition is inverted twice by MLA2-3 and MLA2-6, then integrated by the network C-10 - R60 and applied to the toggle input of MLB1. MLB1 is primed by having "clear" Inputs 11 and 12 connected to Vcc and "Set" Inputs 3 and 4 grounded. This prime causes the negative going transition on Input 2 to drive the Normal output, Output 6, low. Output 6 is connected to Pin 28, send interrupt. Output 9, the inverted output, goes high when Output 6 goes low.

Output 9, high, removes the bias current sink for Q13, which turns off, turning off Q3. Q3 off allows C3 to charge through R16, with a time constant of 330 milliseconds. When the voltage at the anode of CR3 reaches approximately +1.2 volts with respect to ground, Q4 turns on with bias current through R16. The time required to reach turn on will be .806 (330) milliseconds or about 263 milliseconds, nominal. 157

Q4, turned on, holds Input 10 of MLB1, the set direct input, low. This drives MLB1 Output 6 high, ending the INTERRUPT, and forces MLB1 Output 9 low. This turns on Q13 and Q3, capacitor C3 discharges through R14 and Q3, and Q4 turns off. When Q4 turns off, the low on MLB1, Input 10 is removed, MLB1 remains set, with Output 6 high, and Output 9 low, until another positive to negative transition is detected at MLB1 Input 2.

The SEND INTERRUPT circuit is also triggered, as described above, when "RECEIVER IN ALARM" (Pin 29) is low. For the conditions under which "RECEIVER IN ALARM" is low, see Specification No. 61,434.

6. RECEIVED INTERRUPT

RECEIVED INTERRUPT timer RC1 controls PCL, which can operate "HALT" (Pin 21).

"INTERRUPT" is detected on Pin 9, LINE RECEIVE DATA, and is defined as a continuous Space on Line of more than 205 ms. LINE SEND DATA (Pin 10) must not contain the "SEND INTERRUPT" signal, generated byMLB1 and RC2.

6. (Continued)

Pin 9, "LINE RECEIVE DATA" is low when the received data lead from the line interface unit is spacing. Output 6 of MLF4 will be high, holding Input 2 of MLF4 high. If DTRL is set, indicating that the terminal is ready to operate, Input 1 of MLF4 will also be high, and output 3 of MLF4 will be forced low. This drives Output 8 of MLE3 high, removing the bias current sink for Q17, the input transistor of RC1. Q17 turns off, turning off Q10. Q10 off allows C7 to charge through R43. When the anode of CR4 reaches approximately +1.2V DC with respect to ground, Q11 turns on with bias current through R43.

C-7 charges to +1.2V in approximately .806 (12K ohms)(15 mfd) = 144 ms.

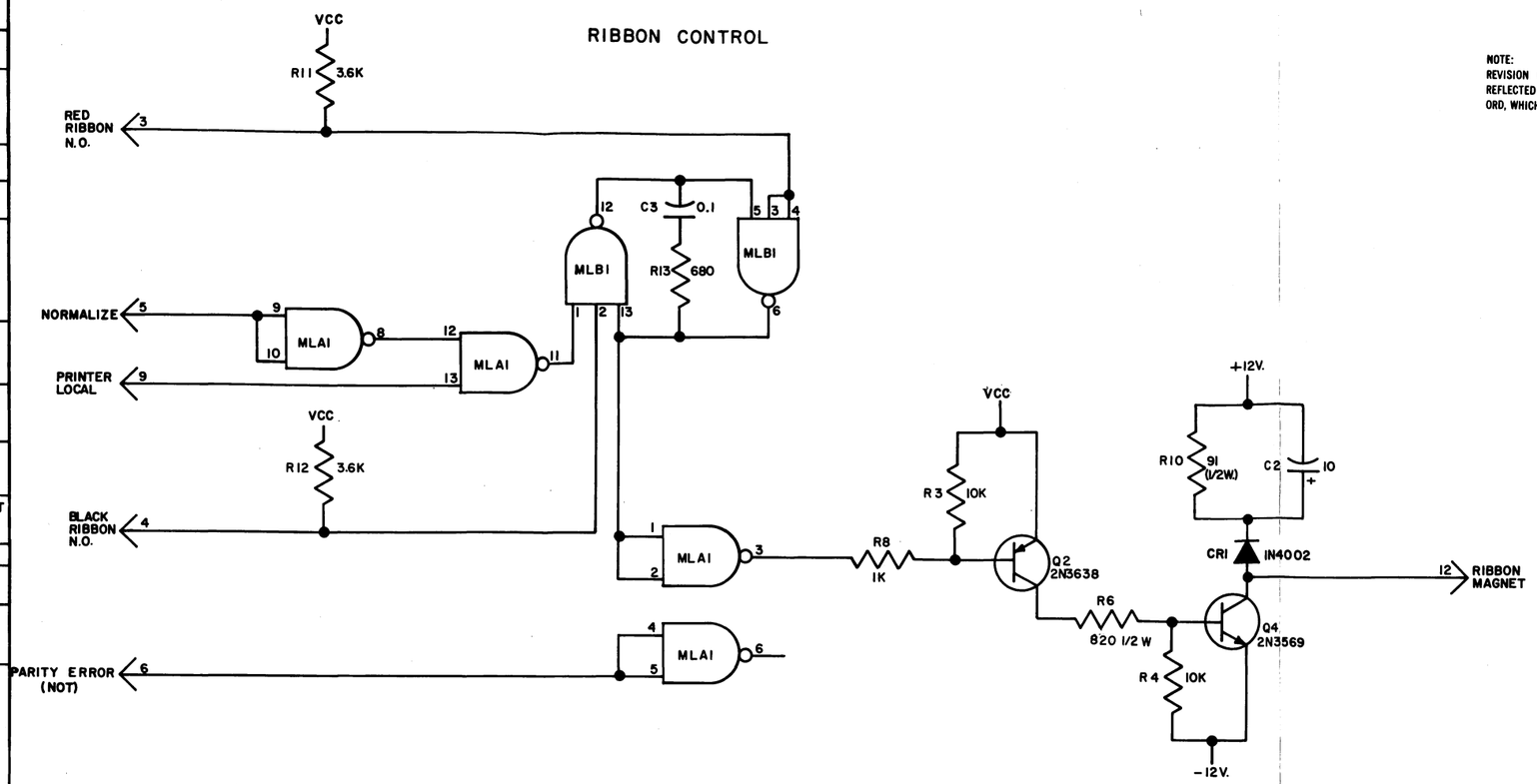
Q11, turned on, sets PCL, forcing "HALT" low.

"HALT", low, should act on the send control card (8381WD-CD) to turn off the "PROCEED" lamp, and inhibit transmission from keyboard (KSR Sets) or keyboard and reader (ASR Sets).

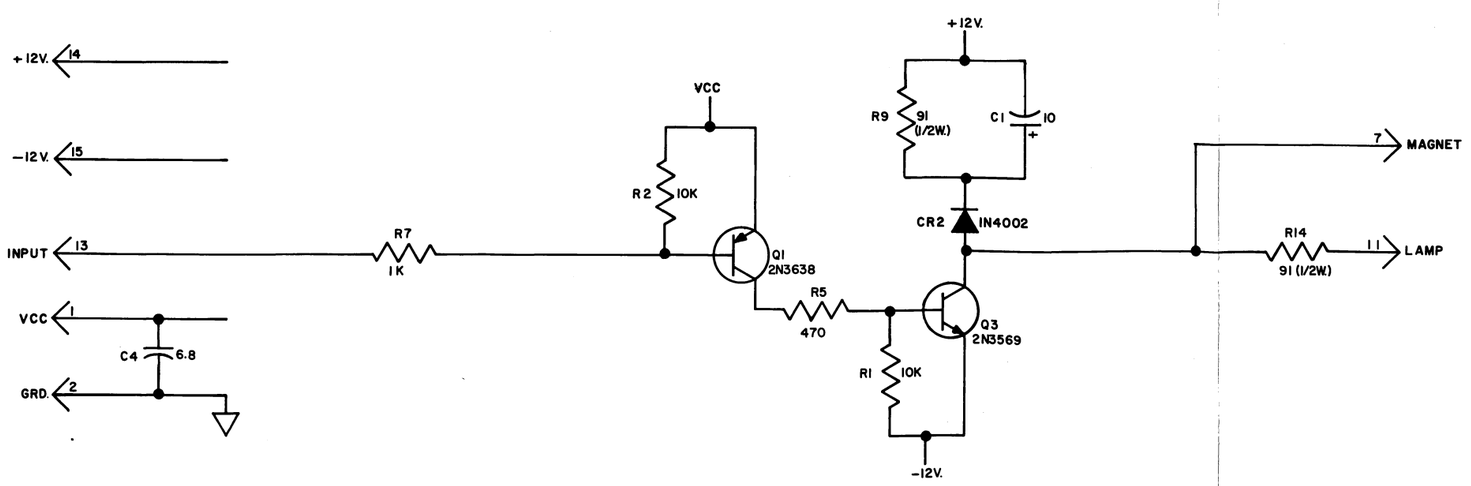
The "RECEIVE INTERRUPT DETECTION" circuit may be disabled by installing Strap H.

NO.	NOTES
1.	ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICRO FARADS UNLESS OTHERWISE SPECIFIED.
4.	INDICATES FEMALE AND INDICATES MALE TERMINAL
5.	REFER TO 322070 FOR ASSEMBLY INFORMATION.
6.	S NUMBER: 61,510 S.
7.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD: ML D 2 — ROW, COLUMN, INTEGRATED CIRCUIT
8.	THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC. AND 0V., RESPECTIVELY.
9.	LOGIC NEGATION- A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
10.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER, THE GATE IS USED AS AN INVERTER.
11.	VCC IS PROVIDED TO THE INTEGRATE CIRCUIT ON PIN 14 AND GROUND ON PIN 7, THIS APPLIES TO ALL PACKAGES.
12.	REFER TO 8399WD FOR TRUTH TABLES.
13.	REFERENCE CIRCUIT DESCRIPTION 8389 WD-CD.
14.	INDICATES CIRCUIT GROUND.

RIBBON CONTROL



AUXILIARY AMPLIFIER



NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8389WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET-1

SCHEMATIC WIRING DIAGRAM FOR TWO COLOR RIBBON CONTROL

APPROVALS

D AND R	E OF M
HBK	

E-NUMBER

PROD. NO. 8389WD.

DATE 4-19-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. | CHKD. RBK

ENGD. R.E.L. | APPD. REH

TELETYPE CORPORATION

8389WD

TC 484 (5-68)

CIRCUIT DESCRIPTION OF THE TWO COLOR RIBBON CONTROL CARD (ASSEMBLY NUMBER 322070)

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NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF THE TWO COLOR RIBBON CONTROL CARD (ASSEMBLY NUMBER 322070)

SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The 322070 Two Color Ribbon Control Card performs the function of ribbon color selection (red or black) upon receipt of proper control signals.

1.2 Additional Features

1.2.1 An additional driver is available for application as a solenoid driver or lamp driver. (Optional suggested use would be to light a lamp upon receipt of SHIFT IN or OUT code.)

1.2.2 The ribbon mechanism is reset to black ribbon at the end of a call ("ON-LINE" mode).

1.3 Ribbon Magnet

The ribbon magnet sinks a steady state current of 230 ma DC (nominal) when a logic zero is present on MLA1 Pin 3 and is in the off state when a logic one is present.

1.4 Auxiliary Driver

When operating as a solenoid driver, the DC resistance of the winding must be at least 110 ohms in order to stay within the safe operating area of Q3. If operated as a lamp driver, a 24 volt DC lamp must be used, (recommended lamp Part No. 327061). 212

1.5 Two-Color Ribbon (Option)

The two-color ribbon control card is an option. It must be provided whenever two-color printing is a terminal requirement. The card plugs into a pre-wired printed circuit card connector and requires no field assembly or adjustment.

2. GENERAL TECHNICAL DATA

2.1 Input-Output Data

2.1.1 The ribbon magnet driver converts the integrated circuit logic inputs to current levels appropriate for ribbon magnet operation.

A logic one is defined as a voltage level between +5.0 volts and +6.6 volts (usually a logic one approximates the integrated circuit supply voltage). A logic one draws no current from the input of the logic element.

Signal voltages between circuit ground potential and +0.5 volts are considered logic zero. Logic currents that flow into the signal source are a function of the element driven, supply voltage, and the value of pull-up resistor used, if any. For additional loading information refer to the manufacturer's specification.

2.2 Input Characteristics

2.2.1 Red Ribbon N.O. (Pin 3)

This input is normally high except during receipt of a red ribbon signal. In Model 37 application, Pin 3 is connected to a N.O. stunt box contact which closes for approximately 20 ms when red printing is desired. The driving source must be capable of sinking approximately two DTL loads. (One DTL load approximately equals 1.4 ma.)

2.2.2 Normalize (Pin 5)

The NORMALIZE input resets the ribbon mechanism to black ribbon when the printer is ON-LINE. This input is high at all times except when a NORMALIZE signal is present. The driving source must be capable of sinking one DTL load.

2.2.3 Printer Local (Pin 9)

This input is low when the printer is operated in the LOCAL mode and high in the ON-LINE mode. The driving source must be capable of sinking one DTL load.

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2.2.4 Black Ribbon N.O. (Pin 4)

This input is normally high except during receipt of a BLACK RIBBON signal. In Model 37 application, Pin 4 is connected to a stunt box contact which closes for approximately 20 ms when black printing is desired. The driving source must be capable of sinking one DTL load.

2.2.5 Parity Error Not (Pin 6)

The PARITY ERROR NOT input is low (LOCAL or ON-LINE mode) as long as proper coding exists and high when a parity error exists. The driving source must be capable of sinking one DTL load.

2.2.6 Input-Auxiliary Driver (Pin 13)

The input characteristics were designed to be compatible with DTL integrated circuit logic elements. A logic one (high) input causes current to flow through the load. A logic zero (low) results in no current flow through the load. The driving source must be capable of sinking approximately three DTL Loads.

2.2.7 Input Ribbon Magnet Driver (MLA1 Pin 3)

Refer to Section I - 2.2.6.

2.3 Output Characteristics

2.3.1 Auxiliary Driver

The auxiliary driver circuit is a two stage amplifier designed to operate full on or full off without intermediate levels. The collector circuit of Q3 contains a transient suppression network consisting of CR2, R9 and C1. When used as a lamp driver, R14 limits lamp surge current to a value within safe operating limits.

2.3.2 Ribbon Magnet

The ribbon magnet driver is a two stage amplifier designed to operate full on or full off without intermediate levels. The collector circuit of Q4 contains a transient suppression network consisting of CR1, R10, and C2. The output circuit is matched to the ribbon magnet assembly. The impedance values of the output circuit have been chosen to provide equal pick-up and drop-out times at some level of ribbon magnet armature spring tension.

2.4 Mechanical Requirements

The 322070 Card Assembly is a standard 15 pin circuit card which is inserted into a 15 pin edge card connector.

2.5 Power Supply Requirements

Vcc (DC)	Current (ma) Max.
+5.0V - +6.6V	125 ma
+11.65V - +13.75V (+12.5V Nom.)	500 ma
-11.13V to -13.88V (-12.5V Nom.)	500 ma

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2.6 Temperature Range

The operating temperature range is from 0°C to 70°C in free air. The storage temperature range is from -40°C to +70°C.

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly and schematic drawings 322070 (MC070) and 8389 WD.

1.2 Logic symbols and truth table 8399 WD.

2. DETAILED DESCRIPTION

2.1 Ribbon Magnet Driver

Assume the printer is "ON-LINE" and a terminal is receiving and printing data in black, (ribbon magnet de-energized). Under these conditions Pins 3, 5, 9, 4 are high, Pin 6 is low, MLA1 Pin 3 is high, MLB1 Pin 13 is low, and MLB1 Pin 12 is high. Assume a "RED RIBBON" bit sequence has been detected by the stunt box and Pin 3 goes low for approximately 20 ms. Latch MLB1 Pin 13 changes states. MLB1 Pin 13 is high, MLB1 Pin 12 is low, and MLA1 Pin 3 is low. A low level (logic zero) input to the ribbon magnet driver causes collector current to flow through R4 and R6. The current flow through R4 results in a positive signal at the base of Q4 (NPN transistor). Q4 is turned full on and the ribbon magnet assembly is energized. The printer now prints the data in red. The ribbon magnet will remain energized until the end of the transmitted message at which time a "NORMALIZE" pulse (low) resets MLB1 (Pin 13 low, Pin 12 high) or a "BLACK RIBBON" bit sequence is detected by the stunt box and Pin 4 goes low for approximately 20 ms.

Assume a "NORMLIZE" pulse (low) has been received on Pin 5. A low on
215 MLA1 Pin 11 resets MLB1 latch (Pin 12 high, Pin 13 low) and MLA1 Pin 3 is now high. Collector current ceases to flow through R4 which results in a negative going pulse at the base of Q4. Q4 is turned off and the ribbon magnet is de-energized. The ribbon magnet assembly has been reset to black printing.

If a "BLACK RIBBON" bit sequence detected by the stunt box causes Pin 4 to go low while printing in red, MLB1 latch is reset (Pin 12 high, Pin 13 low) and MLA1 Pin 3 high. Q4 is now in the "off" state and the ribbon magnet is de-energized. The ribbon magnet assembly has been reset to black printing.

In the "LOCAL" or "ON-LINE" mode, a PARITY ERROR results in a shift from black ribbon to red ribbon. The driver and ribbon magnet assembly is capable of switching from black to red and from red to black within one character time. The ribbon magnet is energized when Pin 6 goes high (MLA1 Pin 6 low). The "PARITY ERROR NOT" input has direct control over the driver when Pin 6 is high.

When operating in "LOCAL" mode, Pin 9 is low and MLA1 gate is disabled (MLA1 Pin 11 high). MLB1 latch is now under direct control of the "Red Ribbon" and "Black Ribbon" inputs.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

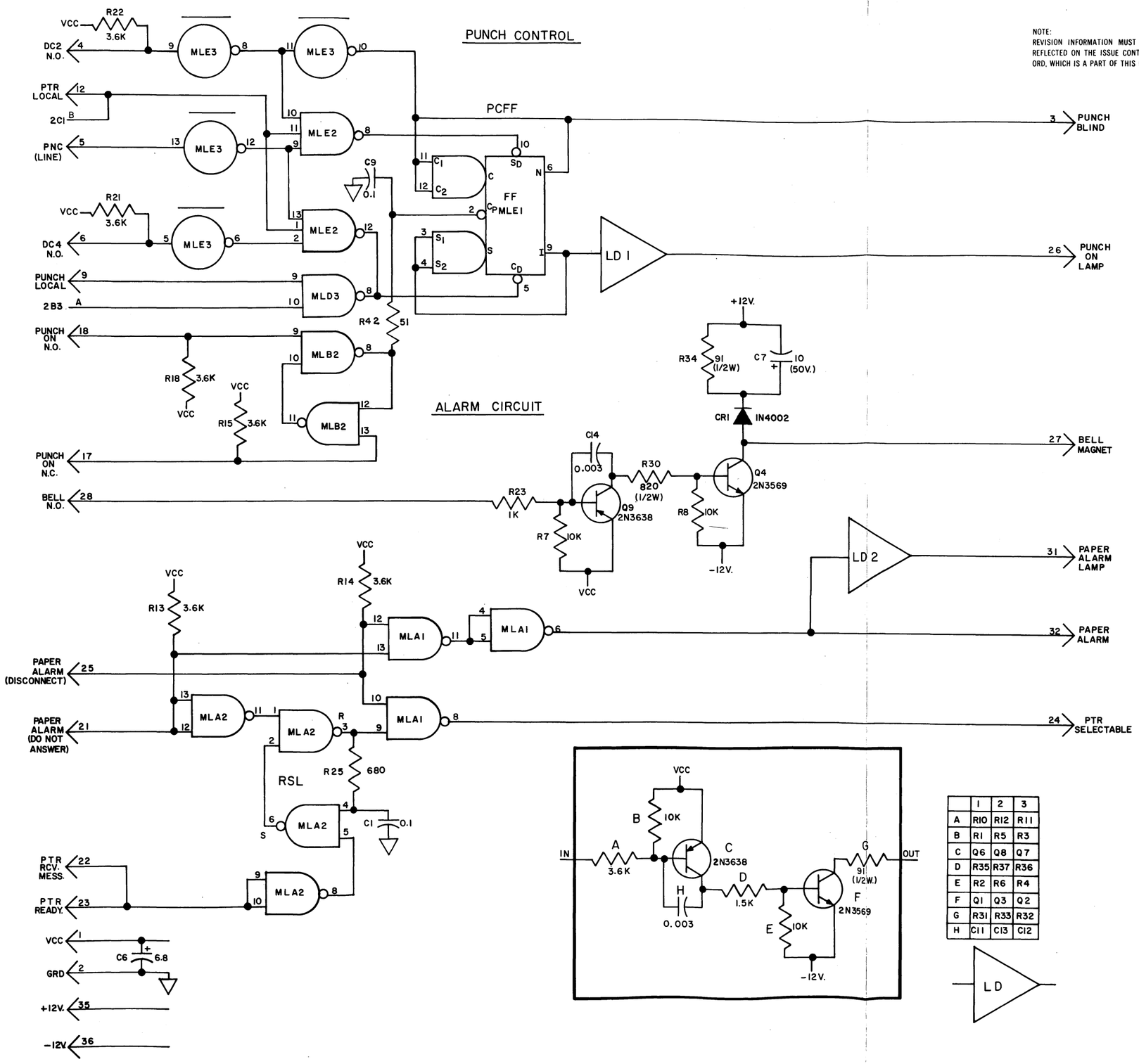
SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

R13 and C3 constitute an RC noise filter. Noise voltages caused by stunt box contact closures or undesirable bounce are integrated so MLB1 latch does not switch to the wrong state.

The transient suppression network consisting of CR1, R10 and C2 dissipates the energy stored in the ribbon magnet winding when Q4 is turned off. This network prevents large inductive voltage spikes from avalanching Q4 collector to emitter.

The two stage auxiliary driver is identical to the ribbon magnet driver. Refer to Section I - 2.2.6 and 2.3.1 for information concerning input and output characteristics, respectively.

NO.	NOTES
1.	ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTOR 1/4W. AND RESISTANCE VALUE IN OHMS, ULESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
4.	INDICATES FEMALE AND INDICATES MALE TERMINALS
5.	REFER TO 322079 FOR ASSEMBLY INFORMATION.
6.	S NUMBER: 61,520 S.
7.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD. ML B2 — ROW, COLUMN, INTEGRATED CIRCUIT
8.	CROSS REFERENCE NOTATION ON SCHEMATIC: 3B4 — ROW, COLUMN, SHEET
9.	LOGIC NEGATION - A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATE A LOGIC NEGATION.
10.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER THE GATE IS USED AS AN INVERTER.
11.	VCC IS PROVIDED TO THE INTEGRATED CIRCUITS ON PIN 14, AND GROUND ON PIN 7. THIS APPLIES TO ALL PACKAGES.
12.	REFER TO 8399WD FOR TRUTH TABLES.
13.	REFERENCE CIRCUIT DESCRIPTION 8395WD-CD.
14.	ABBREVIATIONS USED: RSL- RECEIVER SELECTABLE LATCH. PCFF- PUNCH CONTROL FLIP-FLOP. MCL - MANUAL CONTROL LATCH. ACL - AUTOMATIC CONTROL LATCH. ASL - AUTOMATIC STOP LATCH. ACDM - AUTOMATIC CONTROL DISABLE MATRIX. RAL - READER AUTOMATIC LATCH RAFF - READER AUTOMATIC FLIP-FLOP. MASL - MESSAGE AVAILABLE STORAGE LATCH.
15.	INDICATES CIRCUIT GROUND.



	1	2	3
A	R10	R12	R11
B	R1	R5	R3
C	Q6	Q8	Q7
D	R35	R37	R36
E	R2	R6	R4
F	Q1	Q3	Q2
G	R31	R33	R32
H	C11	C13	C12

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8395WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 1

SCHEMATIC WIRING DIAGRAM FOR ALARMS AND AUTOMATIC CONTROL

APPROVALS

D AND R	E OF M

E-NUMBER

PROD. NO. 8395 WD

DATE 5-27-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. CHKD.

ENGD. C.A.Y. APPD.

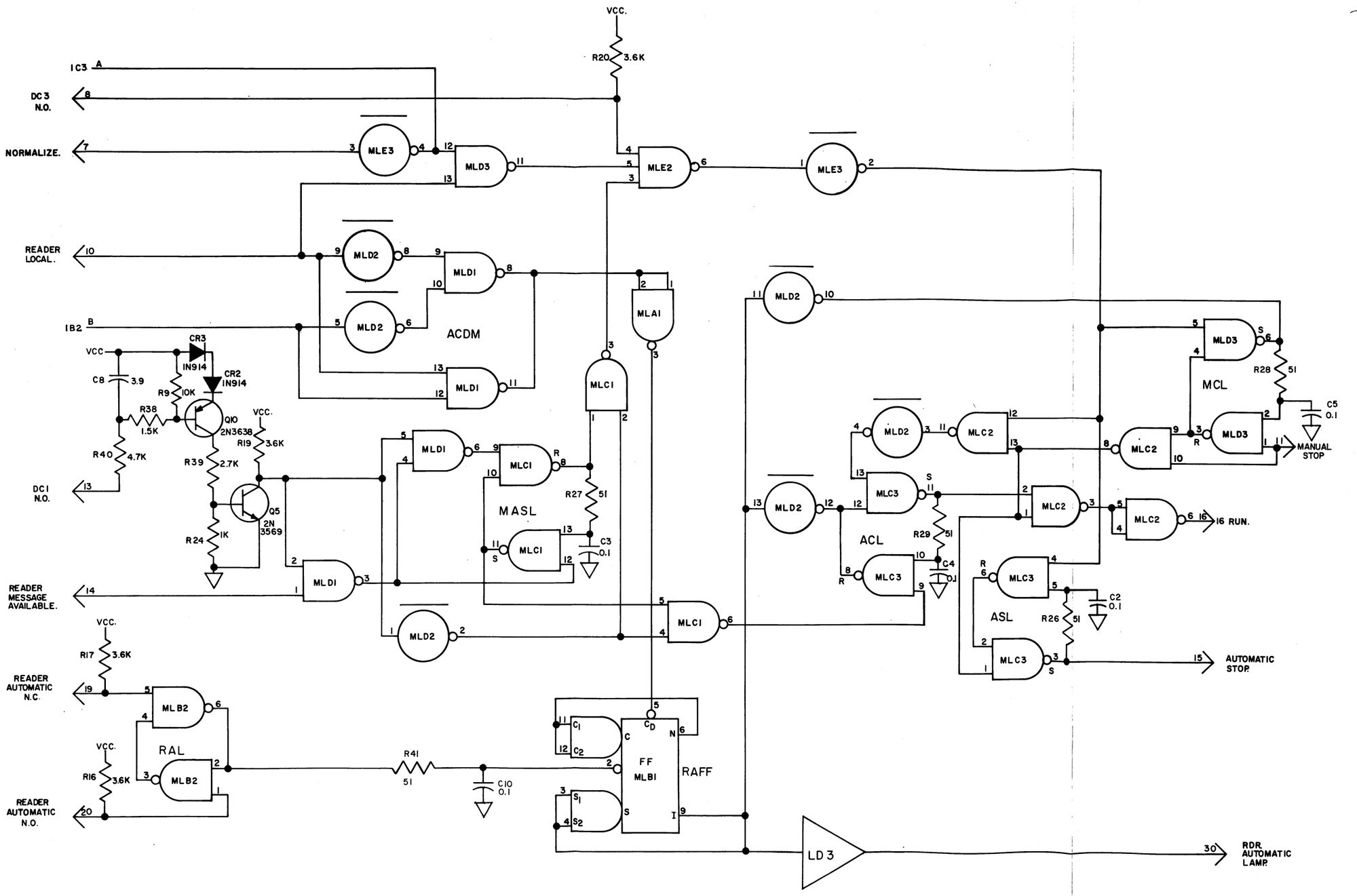
TELETYPE CORPORATION

8395WD

SEE SHEET 1 FOR NOTES.

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

READER CONTROL



8395WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 2

SCHEMATIC WIRING DIAGRAM FOR ALARMS AND AUTOMATIC CONTROL

APPROVALS

D AND R	E OF M
HJK	

E-NUMBER

PROD. NO. 8395 WD.

DATE 3-2-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B.	CHKD.
ENGD. C.A.Y.	APPD.

TELETYPE CORPORATION

8395WD

TC 454 (5-68)

CIRCUIT DESCRIPTION OF THE ALARMS AND AUTOMATIC CONTROL CARD (ASSEMBLY NUMBER 322079)

TABLE OF CONTENTS

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CIRCUIT DESCRIPTION OF THE ALARM AND AUTOMATIC CONTROL CARD (ASSEMBLY NUMBER 322079)

SECTION I

GENERAL TECHNICAL DATA

1. BASIC FUNCTION

The 322079 Alarms and Automatic Controls Card provides:

1.1 Bell driver

1.2 Logically controlled paper alarm circuit

1.3 Automatic punch and reader control circuit which allow these devices to be turned on or off by a pulse from a printer stunt box contact closure.

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

The inputs to the circuit assembly are integrated Diode Transistor Logic (DTL) inputs. Each DTL input is approximately a 1.4 ma load to the driver sinking current from it. At no time should any of these inputs be more positive that +6.6 Volts or more negative than -.7 Volts. Voltage levels represented by the 1-state (high) and 0-state (low) are approximately +6V and 0V respectively. A logic one (high) draws no current from the input of the logic element.

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2.1.1 DC3 N.O. (Pin 8)

This input is normally high and goes low for a nominal period of 20 milliseconds, each time the printer receives the Reader turn off (DC3) control character. The device driving this input must be capable of sinking two DTL loads.

2.1.2 Normalize (Pin 7)

This input is high when the Printer and Punch motors are running in the "on-line" mode, and low at all other times. The device driving this input must be capable of sinking one DTL load.

2.1.3 Reader Local (Pin 10)

This input is high when the Reader is in the "on-line" mode, and low when it is in the "local" mode. The device driving this input must be capable of sinking three DTL loads.

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2.1.4 Printer Local (Pin 12)

This input high or low indicates that the printer is in the "on-line" or "local" mode respectively. The device driving this input must be capable of sinking four DTL loads.

2.1.5 DC1 N.O. (Pin 13)

This input is normally high, switching low for a nominal period of 20 milliseconds, each time the printer receives the Reader turn on (DC1) control character. The device driving this input must be capable of sinking one DTL load.

2.1.6 Reader Message Available (Pin 14)

This input is low any time a message is being sent from the Reader. It switches low at the beginning of a message and remains low throughout the entire duration of a message. The device driving this input must be capable of sinking one DTL load.

2.1.7 Reader Automatic (Pins 19, 20)

Pins 19 and 20 are connected to the N.C. and N.O. side of a "break" before "make" transfer switch respectively. Everytime the switch is operated a negative step, followed by a positive step on release, appears at the MLB-6 to 2 side of the RAL latch. Each input sinks current equal to two DTL loads when low.

2.1.8 Manual Stop (Pin 11)

189 This input is normally low keeping the MCL latch reset. It switches high whenever the Reader Bat Handle is moved from the STOP to RUN position. The device driving this input must be capable of sinking two DTL loads.

2.1.9 DC2 N.O. (Pin 4)

This input rests high, switching low for a nominal period of 20 milliseconds every time the Printer receives the "Punch ON" (DC2) control character. The device driving this input must be capable of sinking two DTL loads.

2.1.10 Line PNC (Pin 5)

This input is low during the time that the "Line Distributor" is idle. It goes high at the beginning of the start bit of each character sent "on-line" and remains high for the duration of the character, before reverting low. The device driving this input must be capable of sinking one DTL load.

2.1.11 DC4 N.O. (Pin 6)

This input is normally high, and goes low for a nominal period of 20 milliseconds each time the Printer detects the "PUNCH OFF" (DC4) control character. The device driving this input must be capable of sinking two DTL loads.

2.1.12 Punch Local (Pin 9)

This input high or low indicates that the Punch is in the "on-line" or "local" mode respectively. The device driving this input must be capable of sinking one DTL load.

2.1.13 Punch On (Pins 17, 18)

Pins 17 and 18 are connected to the N.C. side of a break-before-make transfer switch, respectively. Each time the switch is operated, a negative step, followed by a positive step on release, appears at the MLB2-8 to 12 side of the latch formed by MLB2-8 and MLB2-11. Each input sinks current equal to two DTL loads when low.

2.1.14 Bell N.O. (Pin 28)

Any low on this input results in the turn on of the bell driver consisting of Q9 and Q4 which causes the bell to ring. The device driving this input must be capable of sinking 4.5 ma.

2.1.15 Paper Alarm (Disconnect) (Pin 25)

A low on this input indicates a "low paper" or "paper out" condition on the printer. It is used to simultaneously light the Paper Alarm Lamp, and remove the "Printer Selectable" condition, thereby causing an immediate "on line" disconnect. The device driving this input must be capable of sinking three DTL loads. 190

2.1.16 Paper Alarm (Do Not Answer) (Pin 21)

This input switching low during the course of "on line" operation, due to a low paper or paper out condition of the Printer, causes the removal of "Printer Selectable" at the end of a call and prevents establishing another call until the Paper Alarm condition is removed. The device driving this input must be capable of sinking three DTL loads.

2.1.17 Printer Receive Message (Pin 22)

This input is low whenever the Printer Motor is running. The device driving this input must be capable of sinking one DTL load.

2.2 Output Characteristics

The outputs from this assembly are either Diode Transistor Logic or transistor driver outputs. Each output will be rated by the number of DTL loads it can sink. Each DTL load is approximately 1.4 ma.

2.2.1 Punch Blind (Pin 3)

When this output is in the 0 state the punch is blinded. If it is in the 1 state the punch is unblinded and capable of receiving a message. This output will sink ten DTL loads.

2.2.2 Bell Magnet (Pin 27)

This output connects to one side of the Bell coil winding. It is +12V when the Q_4 drive transistor is off and -12V when the Bell coil is energized.

2.2.3 Paper Alarm Lamp (Pin 31)

This output is used to light a Paper Alarm Lamp located on the control panel, by applying 24V across a bulb.

2.2.4 Paper Alarm (Pin 32)

This output is low whenever a Printer Paper Alarm condition exists, and high at all other times. This output will sink six DTL loads.

2.2.5 Printer Selectable (Pin 24)

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This output is normally low indicating that the printer is selectable for "on line" operation. Should a Paper Alarm (Disconnect) condition occur this lead will immediately switch high indicating Printer not selectable. If, during the course of an "on line" call, a Paper Alarm (Do Not Answer) condition occurs, the Printer Selectable lead will go high at the end of the call, indicating printer not selectable, and prevent establishment of another call until the Paper Alarm condition has been remedied. This output will sink eight DTL loads.

2.2.6 Run (Pin 16)

A low or high on this output indicates that the Reader is running or not running respectively. This output will sink eight DTL loads.

2.2.7 Automatic Stop (Pin 15)

This output low, indicates that the Reader has been stopped automatically. This output will sink eight DTL loads.

2.2.8 Reader Automatic Lamp (Pin 30)

This output is used to light the Reader Automatic Lamp, by applying 24V across a bulb.

2.2.9 Printer Ready (Pin 23)

This output is a turn about of the Printer Receive Message input.

2.2.10 Punch On Lamp (Pin 26)

This output turns on a lamp when the punch is not blinded. The output will sink up to 60 ma to the -12V supply when on.

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 See assembly drawing 322079 (MC 079) and schematic drawing 8395WD and 8399WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 General

The alarms and automatic control card contains four fundamentally independent logic systems. These are: Automatic Reader Control, Automatic Punch Control, Paper Alarm Logic, and Bell Driver.

3. READER CONTROL, GENERAL

3.1 The Reader runs or stops, depending on the state of the "RUN" output, Pin 16. (See Table 1)

3.11 Pin 16 low, Reader Runs

3.12 Pin 16 high, Reader Stops

3.2 The "RUN" output follows two control latches; AUTOMATIC CONTROL LATCH (ACL) MANUAL CONTROL LATCH (MCL).

3.2.1 MANUAL STOP Pin 11, low, sets MCL when the Reader bat handle switch is at "Stop" or "Free". When the bat handle is at "RUN", Pin 11 is high.

193 3.2.2 AUTOMATIC STOP Pin 15, is low when the reader has been stopped by any of the automatic control signals. When AUTOMATIC STOP goes low, the reader should stop immediately.

3.3 Reader Automatic Lamp, Pin 30

The Automatic Reader Control Circuit is enabled when the "READER AUTOMATIC" lamp is lit. The lamp is lit by a low input to the lamp driver from J-K flip-flop MLB1, Pin 9. MLB1 is disabled by a low input on Pin 5, from AUTOMATIC CONTROL DISABLE MATRIX (ACDM) output, MLA1 Pin 3. This output will be high when the Reader and the associated character detector (printer stunt box) are both on line or both local. When not disabled by ACDM, MLB1, may be toggled by the Reader Automatic Latch (RAL), under control of the READER AUTOMATIC switch.

The NORMALIZE input (Pin 7 low) will inhibit a "RUN" output while the reader is ON LINE (Pin 10 high), but will not prevent selection of READER AUTOMATIC.

4. READER START

4.1 Manual Start

4.1.1 Bat handle at STOP, reader not running. If the reader is not running, RUN is high, and inputs 1 and 2 of MLC2 must be high. Input 1 of MLD3 is low when the bat handle is at STOP, holding MCL Set.

When the bat handle is moved to RUN, MANUAL STOP, Pin 11 goes high. With MCL still set (SET side low, RESET side high), inputs 9 and 10 of MLC_2 are both high, forcing MLC_2 Pin 8 low. MLC_2 input 1 is now low, operating the RUN lead, (Pin 16 low.)

4.1.2 Bat handle at Run, reader not running. If the reader is not running, RUN is high, and inputs 1 and 2 of MLC_2 must be high MANUAL STOP (Pin 11) is high since the bat handle is in the RUN position. ACL and MCL which produce the run inputs to MLC_2 must both be in the reset state (RESET side low, SET side high).

When the bat handle is moved to STOP, MANUAL STOP (Pin 11) goes low setting MCL. Inputs 1 and 2 of MLC_2 remain high. Moving the bat handle back to the RUN position (Pin 11 high) forces MLC_2 output 8 low causing the reader to run (Pin 16 low). The low on MLC_2 output 8 sets ACL (MLC_2 input 2 high) and resets ASL (Pin 15 high).

4.2 Automatic Start

The following conditions are necessary before initiating Automatic Reader Start.

A. The bat handle may be at RUN or STOP.

B. READER AUTO must be enabled (lamp lit) and, if "on-line", not normalized.

C. The Reader must not be running.

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4.2.2 If the reader is not running, inputs 1 and 2 of MLC_2 are both high, and Reader Message Available Pin 14 is high. The collector of Q5 rests high, in the absence of a "reader start code detected" signal on Pin 13. Inputs 1 and 2 of MLD1 are high, forcing MLD1 output 3 low. This holds the Message Available Storage Latch (MASL) Reset.

A low output on the collector of Q5 will occur about 10 milliseconds after a low input has been applied at Pin 13. The low output on Q5 collector, applied to MLD1 inputs 5 and 2, removes the Reset input to MASL. MASL remains reset. The low output on Q5 collector is also applied to input 1 of MLD2, forcing MLD2 output 2 high and MLD1 input 4 high. MLC1 input 5, connected to the set output of MASL, is also high. This forces output of 6 MLC1 low, setting ACL. ACL set output is connected to MLC2 input 2 and forces RUN (Pin 16) low, starting the reader. As a result, Reader Message Available (Pin 14) will be made low by the control logic associated with the reader. This will ordinarily happen within a few microseconds of Run (Pin 16) going low, but will not effect MASL, since both the set and reset inputs to MASL are held high by the low on the collector of Pin 15.

About 10 milliseconds after READER START CODE DETECTED, Pin 13 goes high, the collector of C5 will go high. This will force MLD_2 output 2 low and allow MLD1-3 to follow READER MESSAGE AVAILABLE and control the slate of MASL. Due to the action of network C3-R27, MASL cannot respond to the changed state of READER MESSAGE AVAILABLE for about 100 microseconds, while MLD2 output 2 responds within 100 nanoseconds to force output 6 of MCL1 high.

5. READER STOP

5.1 Manual Stop

5.1.1 The following conditions are necessary before initiating manual Reader Stop.

A. Bat handle at RUN, Reader running.

B. If the reader is running, input 1 of input 2 or MLC2 is low, holding the RUN output (Pin 16) low.

5.1.1.1 If input 1 of MLC2, low, is holding RUN (Pin 16) low, the reader will be stopped by a low on MANUAL STOP Pin 11. Input 1 of MLC2 can be held low only by output 8 of MLC2, which is low only when inputs 9 and 10 of MLC2 are both high. This indicates that MCL is set, and MANUAL STOP (Pin 11) is high. If MANUAL STOP (Pin 11) is made low, MLC2 output 8 and MLC2 input 1 will go high, and the reader will stop.

5.1.1.2 If input 2 of MLC_2, low, is holding Run (Pin 16) low, ACL must have been set by a DC_1. Since ACL could not have been set while output 8 of MLC_2 was low. Since MANUAL STOP (Pin 11) is high, MCL must be reset. Therefore MLC_2 input 1 is high.

195 When the bat handle is moved from RUN to STOP, MANUAL STOP (Pin 11) goes low setting MCL (MLD3-6 low). When the bat handle is moved from Stop to Run with MCL set output of MLC_2 goes low, resetting ACL (MLC3-11 high). When the bat handle is moved once again from run to stop MLC_2 output 8 goes high and stops the reader (Pin 16 - high).

This situation comes about only when the reader has been started manually, stopped automatically, and then restarted automatically.

5.1.2 Bat Handle at Stop, Reader Running

If the reader is running, either input 1 or input 2 of MLC2 is low. With the bat handle at STOP, MANUAL STOP (Pin 11) is low, forcing output 8 of MLC2 and input 1 of MLC2, high. Input 2 of MLC2 and the SET output of ACL are low, holding RUN (Pin 16) low. With MANUAL STOP (Pin 11) low, MCL is set. When the bat handle is moved to RUN, MANUAL STOP goes high. With the reset output of MCL already high, output 8 of MLC2 is forced low. This keeps RUN low and resets ACL through MLC2-11 and MLD2-4. When the bat handle is moved back to STOP, MANUAL STOP goes low, forcing MLC2 output 8 high, stopping the reader.

5.2 Automatic Stop

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

5.2.1 The following conditions are necessary before initiating Automatic Reader Stop.

A. At RUN or STOP

B. READER AUTO must be enabled (if "on-line", it must be NORMALIZED)

C. The Reader must be Running

5.2.2 If the reader is running, RUN (Pin 16) is low, and either input 1 or input 2 of MLC2 is low.

When any of the 3 inputs of MLE2 output 6 are low, output 2 of MLE3 will be low. MLE3 output 2 low, resets MCL, sets ASL, and, through MLC2-11 and MLD2-4, resets ACL. Inputs 1 and 2 of MLC2 will be high and the reader stops.

5.2.3 Normalize

The "Normalize" lead, Pin 7, is low throughout the time that the terminal is not connected on line. NORMALIZE, Pin 7, low, forces MLE3 output 4 high. When READER LOCAL, Pin 10, is also high, output 1 of MLD3 will force input 5 of MLE2 low, stopping the reader.

5.2.4 Reader Stop Code Detected (DC3)

A low input on Pin 8 will stop the reader by forcing input 4 of MLE2 low. This lead is used for a READER STOP CODE DETECTED input (normally ASCII character DC3).

5.2.5 Reader Start Code Detected (DC1)

When the READER START character (normally ASCII DC1) is sent by the reader, as in an exchange of messages between two automatic terminals, the reader in the sending terminal must be stopped. The operation is similar to AUTOMATIC START Section 4.2. 196

If the reader is running, READER MESSAGE AVAILABLE Pin 14 will be low. In the absence of a READER START CODE DETECTED input on Pin 13, READER MESSAGE AVAILABLE low will set MASL, forcing input 1 of MLC1 high. About 10 milliseconds after READER START CODE DETECTED (Pin 13) goes low the collector of Q5 goes low, blocking further input to MASL. At the same time, input 1 of MLD2 goes low, forcing output 2 of MLD2 high. This enables gates MLC1-3 and MLC1-6. With the MASL Set, MLC1-6 remains high while MLC1-3 goes low, forcing input 3 of MLE2 low, stopping the reader.

About 10 milliseconds after the READER START CODE DETECTED input is removed, the collector of Q5 goes high, restoring control of MASL to the READER MESSAGE AVAILABLE input (Pin 14) and forcing output 2 of MLD2 low, disabling gates MLC1-3 and MLC1-6. Due to the action of network R27-C3, MASL cannot respond to the changed input from READER MESSAGE AVAILABLE for about 100 microseconds, while MLD2-2 operates in about 100 nanoseconds to disable the output gates.

6. PUNCH CONTROL

6.1 General

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

1

The automatic punch control circuit blinds or unblinds the punch. Local (off-line) control is by the lighted switch on the control panel. "ON-LINE" control is by the switch or by the function box contacts.

6.2 Detailed Description

6.2.1 The control output of the automatic punch control circuit is on Pin 3, punch blind. Punch blind (Pin 3 low) must operate on the Receive Control Card (8383 WD - CD) to inhibit serial signal input to the punch receiver device card.

Pin 26 PUNCH ON lamp is driven by LD_1 when the punch is not blind LD_1 and Pin 3 are also driven by the two alternate outputs of the punch control flip-flop MLE1.

6.2.2 MLE1 has two alternate states, ON and OFF. MLE1 output 6 low defines the OFF state, during which the punch is blind and the PUNCH ON lamp is not lit. MLE1 output 9 low defines the ON state, during which the PUNCH ON lamp is lit, and the punch is unblinded.

6.2.2.1 The MLE1 toggle input (input 2) is controlled by the PUNCH ON switch. Operating the PUNCH ON switch produces a high-low-high toggle input to the flip-flop. If there are no direct set or direct clear inputs (Inputs 5 and 10 both high), operating the PUNCH ON switch will change the state of MLE1 from ON to OFF or from OFF to ON.

6.2.2.2 The MLE1 clear direct input, input 5, is controlled by MLD3 output 8 and MLE2 output 12. When either of these outputs is low, MLE1 will be turned OFF (Punch Blind).

6.2.2.3 MLD3 output 8 is low when Pin 9, Printer Local is high indicating that the printer is on line, and MLE3 output 4, connected to MLD3 input 10, is high, indicating that "Normalize" (Pin 7) is low. NORMALIZE is low when no call is in process on line.

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MLE2 output 12 is low when DC4 N.O. (Pin 6) is low and the gate is enabled by having inputs 1 and 13 high. MLE2 input 1 is high when Pin 12, PRINTER LOCAL is high, indicating that the printer is "on-line".

MLE2 input 13 is high when Pin 5, LINE PNC, is low. LINE PNC low during a function box contact closure on Pin 6 indicates that the DC4 does not result from a character sent by the line distributor. LINE PNC is high for a total of 22 bit times, when the line distributor has sent a control character, such as DC_4.

6.2.3 The MLE1 set direct input, input 10, is controlled by MLE2 output 8. When MLE2 output 8 goes low MLE1 will be turned ON (Punch unblind).

6.2.3.1 MLE2 output 8 goes low when DC2 N.O. (Pin 4) is low, and the gate is enabled by having inputs 9 and 11 high. MLE2 input 11 is high when PRINTER LOCAL Pin 12 is high, indicating that the printer is ON LINE. MLE2 input 9 is high when line PNC (Pin 5) is low. Line PNC is high for a total of 22 bit times when the line distributor has sent a control character, such as DC2. LINE PNC low during a DC2 function box contact closure on Pin 4 indicates that the DC2 does not result from a character sent by the line distributor.

6.2.3.2 MLE3 output 10 goes low when the DC2 input on Pin 4 is low, holding punch blind (Pin 3) low, without regard for the state of MLE1. Nominal function box contact timing for the M37 printer shows that the function box contact does not re-open until the stop bit of the character space following the detected character which caused the function box contact closure. This arrangement of MLE3 output 10 insures that the punch will not actually be unblinded until the signal line is marking, thus preventing a "hit" character when DC2 unblinds the punch.

6.3 No provision for punch motor control is made on this card. See channel control, 8388 WD - CD for details of on line punch motor control.

7.0 Bell Driver

7.1 The bell driver circuit is a two state amplifier, designed to operate full ON or OFF without intermediate levels.

A logic zero applied to the input of Q9 results in a positive going pulse at the base of Q4. As a result, Q4 is turned ON and approximately 24 volts DC is applied to the bell winding. The bell (collector current of Q4) current rises exponentially to a nominal value of 230 ma. The rise time of the current waveform is determined by the inductance and series resistance of the bell winding.

A logic one applied to the input of Q9 causes Q9 collector current to decrease to zero. As a result, a negative going pulse appears at the base of Q4. Q4 is now in the "OFF" state. The bell winding discharges its energy through CR_1 and the discharge network R34, C7. The pickup and dropout times are not adjustable and for a given bell are a function of the charge network, discharge networkds and winding inductance which determine the electrical time constant.

8.0 Paper Alarm

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8.1 During normal set operation the paper alarm lamp is off and a logic one (high) appears at Pin 32, the Paper Alarm output. There are two paper alarm signals. One of these calls for immediate action by the set logic, and the other calls for delayed action at the end of the message being received. The two paper alarm inputs appear at Pin 25, Paper Alarm (disconnect), and at Pin 21, Paper Alarm (Do Not Answer), respectively. When either of these inputs is low, gate MLA1-11 switches. The output is inverted by MLA1-6, and is applied to the alarm lamp amplifier (LD2) and the paper alarm output at Pin 32. A logical zero for a paper alarm causes the Alarm Lamp Amplifier Q8 and Q3 to conduct and turn on the Alarm Lamp.

8.2 The Paper Alarm (Disconnect), at Pin 25, also switches MLA1-8. A logical one appears at Pin 24, the Selectable output. Set logic takes immediate "alarm" action.

With a message in process, a logical zero appears at Pin 22. This signal is transferred to Pin 23 as an output, and is also applied to inverter MLA2-8. The output of MLA2-8 goes high. With no alarm present, the output of MLA2-11 is low which switches MLA2-3 high. At this time, since logical one signals appear at both inputs of MLA2-6, its output is low,

latching MLA2-3 high. When a Paper Alarm (DO NOT ANSWER) appears at Pin 21, the logical zero is inverted by MLA2-11. MLA2-3, however, will not switch since its other input (input 2) remains low. When the message being received is complete, however, MLA2-8 switches low, which in turn switches MLA2-6 high. This now sets MLA2-3 low and MLA2-6 high. The Selectable output (Pin 24) switches high, which generates a delayed alarm.

TABLE I

READER OPERATION WITH AUTOMATIC CONTROL

1. MANUAL START

1.1 Bat handle at "STOP"
Move bat handle to "RUN"

1.2 Bat handle at "RUN"
Move bat handle to "STOP", then back to "RUN"

2. MANUAL STOP

2.1 Bat handle at "RUN"
Move bat handle to "STOP". If the reader was started by automatic control, the reader will not stop. Move the bat handle back to "RUN" and then return to "STOP". The reader will stop.

2.2 Bat handle at "STOP"
Move the bat handle to "RUN", then back to "STOP". The reader will stop.

3. AUTOMATIC CONTROL

3.1 Enabling Automatic Control

3.1.1 Reader and Typing Unit must be either on line or local, together.

3.1.2 Reader Automatic Lamp must be lit

3.1.3 Bat handle may be at "RUN or "STOP"

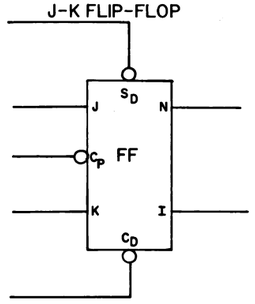
200

3.2 Starts when DC1 is received

3.3 Stops when DC1 is sent by the Reader or when DC3 is received.

NO.	NOTES
1.	GRAPHICAL SYMBOLS AND THE ASSOCIATED TRUTH TABLES ILLUSTRATED ON THIS PAGE ARE TYPICAL SYMBOLS USED IN TELETYPE CORPORATION APPARATUS.
2.	LOGIC NEGATION - A SMALL CIRCLE (O) DRAWN AT THE POINT WHERE A SIGNAL LINE JOINS A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
3.	STATE DESIGNATIONS: I - STATE = +6V O - STATE = 0V
4.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER THE GATE IS USED AS AN INVERTER.
5.	ABBREVIATIONS USED: O - LOW STATE (MORE NEGATIVE) I - HIGH STATE (MORE POSITIVE) X - STATE OF INPUT DOES NOT AFFECT STATE OF CIRCUIT NC - NO CHANGE U - INDETERMINATE STATE N_M - STATE OF N AT TIME M. $\overline{N}_M$ - INVERSION OF STATE OF N AT TIME M.

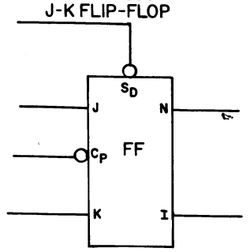
326852 J-K FLIP-FLOP



ASYNCHRONOUS TRUTH TABLE 326852

S_D	C_D	N	I
I	I	NC	NC
O	I	I	O
I	O	O	I
O	O	I	I

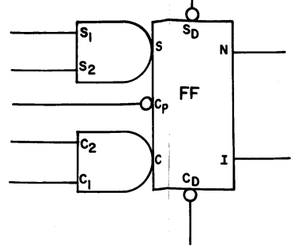
326853 J-K FLIP-FLOP



ASYNCHRONOUS TRUTH TABLE 326853

S_D	N	I
I	NC	NC
O	I	O

326845 CLOCKED FLIP-FLOP



ASYNCHRONOUS TRUTH TABLE 326845

C_D	S_D	N	I
I	I	NC	NC
I	O	I	O
O	I	O	I
O	O	I	I

SYNCHRONOUS TRUTH TABLE 326845

S_1	S_2	C_1	C_2	N
O	X	O	X	NC
O	X	X	O	NC
X	O	O	X	NC
X	O	X	O	NC
O	X	I	I	O
X	O	I	I	O
I	I	O	X	I
I	I	X	O	I
I	I	I	I	U

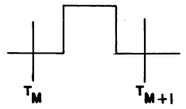
J-K TRUTH TABLES (CONNECT S_2 TO I, C_2 TO N)

T_M		T_{M+1}
S_1	C_1	N
O	O	N_M
I	O	I
O	I	O
I	I	$\overline{N}_M$

J-K TRUTH TABLE BOTH TYPES

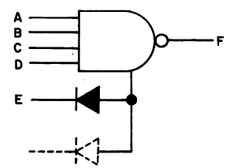
T_M		T_{M+1}
J	K	N
O	O	N_M
I	O	I
O	I	O
I	I	$\overline{N}_M$

CLOCKED PULSE WAVE FORM



ASYNCHRONOUS INPUTS, DIRECT SET (S_D) AND DIRECT CLEAR (C_D), OVERRIDE THE SYNCHRONOUS INPUTS. THEY ARE INDEPENDENT OF ALL OTHER INPUTS.

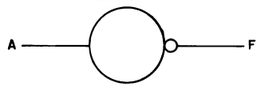
NAND GATE



A	B	C	D	E	F
I	I	I	I	I	O
I	O	O	O	O	I
O	O	O	O	O	I
O	I	I	I	I	I

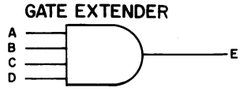
A,B,C,D OR E LOW(O) CAUSES F TO GO HIGH (I)

INVERTER



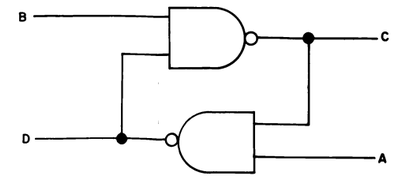
A	F
O	I
I	O

GATE EXTENDER



$E = A \cdot B \cdot C \cdot D$

SET-RESET FLIP-FLOP UTILIZING NAND GATES



A	B	C	D
O	O	I	I
O	I	O	I
I	O	I	O
I	I	NC	NC

8399 WD

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	5-3-68	19208-R

LOGIC SYMBOLS AND TRUTH TABLES

APPROVALS	
D AND R	E OF M
E-NUMBER	
PROD. NO. 8399WD	
DATE 2-12-68	
P.D. FILE NO. G-A354AA	
DRAWN RJP	CHKD.
ENGD. MJR	APPD.

TELETYPE CORPORATION

8399WD

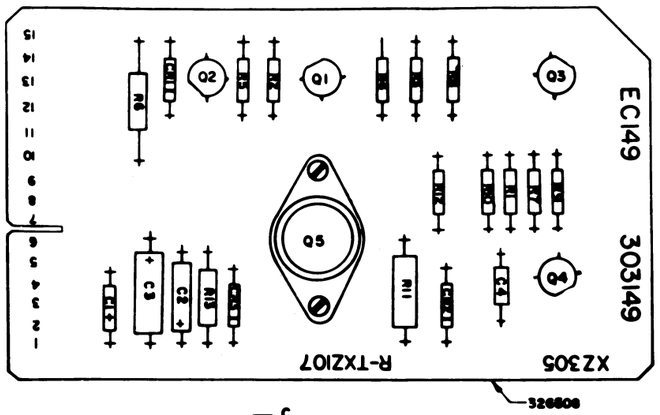
TC 484 (3-68)

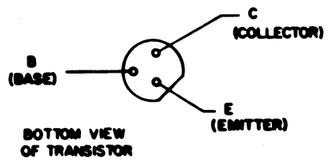
NO. NOTES

1 SEE SPECIFICATION MR2.001 FOR CIRCUIT BOARD REQUIREMENTS.

2 REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY

3 ASSOCIATED SCHEMATICS 8370WD





BOTTOM VIEW OF TRANSISTOR

CIRCUIT CARD EC

REF DESIG.	TELETYPE PART NO	TOTAL QTY	NAME AND DESCRIPTION	LOCATING FUNCTION
R1-2	315958	2	RES. FIXED 3.6K	1/4W
R3	320275	1	" " 10K	1/4W
R4	315954	1	" " 1.5K	1/4W
R5	320275	1	" " 10K	1/4W
R6	182514	1	" " 91	1/2W
R7	315958	1	" " 3.6K	1/4W
R8	320275	1	" " 10K	1/4W
R9	320276	1	" " 470	1/4W
R10	321507	1	" " 1.8K	1/4W
R11	139336	1	" " 150	2W
R12	321213	1	" " 1K	1/4W
R13	118724	1	" " 220	1/2W
C1	327831	1	CAPACITOR DISC 6.8 MFD 6V DC	
C2	326591	1	" TANT. 3.9 MFD 35V DC	
C3	326592	1	" TANT. 33 MFD 35V DC	
C4	326752	1	" .03 MFD 50V DC	
Q2	324656	1	TRANSISTOR 2N3569	
Q1-3-4	315931	1	" 2N3638	
Q5	326594	1	" 2N3767	
CR1	321939	1	DIODE 1N4002	
CR2	197464	1	" 1N914	
CR3	321949	1	" 1N4002	
	326508	1	BOARD, ETCHED CIRC.	
	3598	2	NUT	
	154335	2	SCREW	
	107116	2	LOCKWASHER	

303149

REVISIONS

ISSUE	DATE	AUTH. NO.
6	11-15-68	96464-1

WDP

SHEET 1

RECEIVING DEVICE

APPROVALS

R AND D	E OF M

E-NUMBER

PROD NO 303149

DATE 8-11-67

R&D FILE G-A354AA

DRAWN R.J.P. | CHKD

ENGD. M.J.R. | APPD.

TELETYPE CORPORATION

303149

NO. NOTES

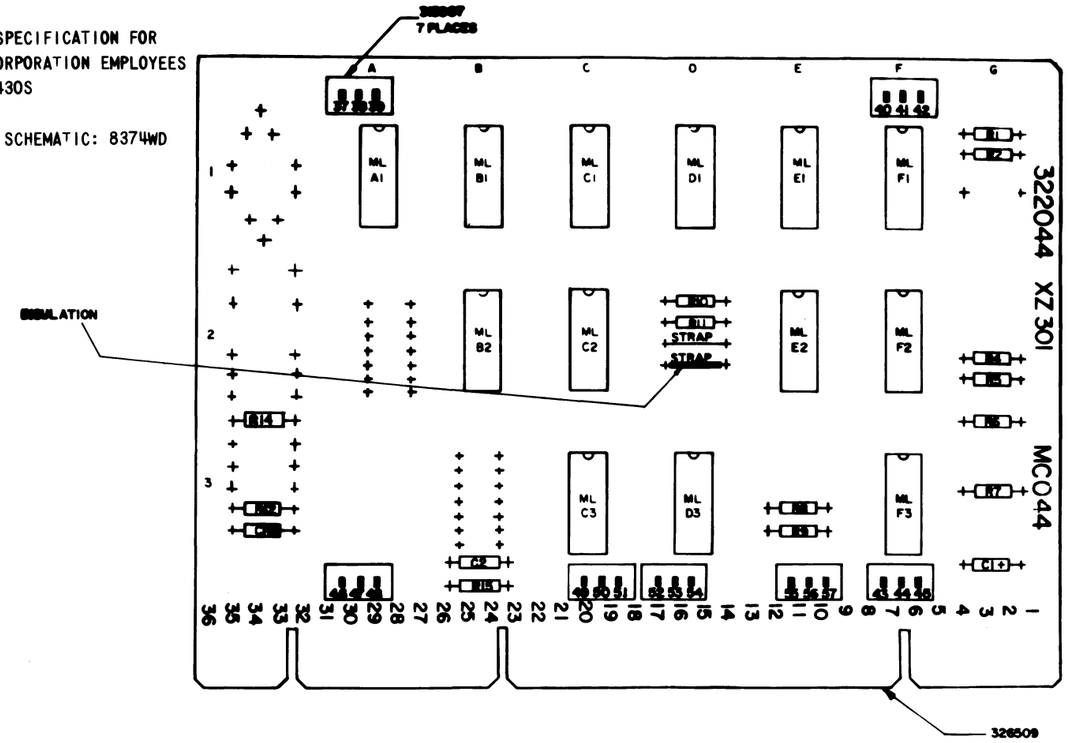
1 INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD

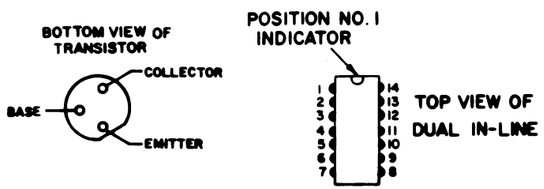
ML D 2
- ROW
- COLUMN
- INTEGRATED CIRCUIT

2 SEE SPECIFICATION MR2.001 FOR CIRCUIT BOARD REQUIREMENTS.

3 REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY: 61,430S

4 ASSOCIATED SCHEMATIC: 8374WD





CIRCUIT CARD EC

REF DESIG.	TELETYPE PART NO	TOTAL QTY	NAME AND DESCRIPTION	LOCATING FUNCTION
ML A1	326830	1	INTEGR. CIRC.	
ML B1	326862	1	" "	
ML C1	326862	1	SAME AS ML B1	
ML D1	326846	1	INTEGR. CIRC.	
ML E1	326846	1	SAME AS ML D1	
ML F1	326846	1	" " "	
ML B2	326846	1	" " "	
ML C2	326846	1	" " "	
ML E2	326846	1	" " "	
ML F2	326846	1	" " "	
ML C3	326832	1	INTEGR. CIRC.	
ML D3	326846	1	SAME AS ML D1	
ML F3	326846	1	" " "	
R1-R2	315958	2	RESISTOR 3.6K 1/4 W	
R12	315955	1	" 2.2K 1/4 W	
R14	31597 1	1	" 680 1/4 W	
R4-R11	315958	8	" 3.6K 1/4 W	
C1	327831	1	CAPACITOR 6.8MFD 6V DC	
CR1	197464	1	DIODE 1N914	
	39603RM	2	STRAP 24 GA .007"	
	315967	7	CONTACT STRIP	
	326509	1	CIRCUIT BOARD	
R15	315947	1	RESISTOR 51 1/4 W	
		1	INSULATION	
C2	312385	1	CAPACITOR 1 MFD 10V	

322044

REVISIONS

ISSUE	DATE	AUTH. NO.
6	11-15-68	96464

WDP

SHEET 1

KEYBOARD CONTROL LOGIC

APPROVALS

R AND D	E OF M

E-NUMBER

PROD NO 322044

DATE 11-9-67

R&D FILE G-A354AA

DRAWN R.J.P. CHKD

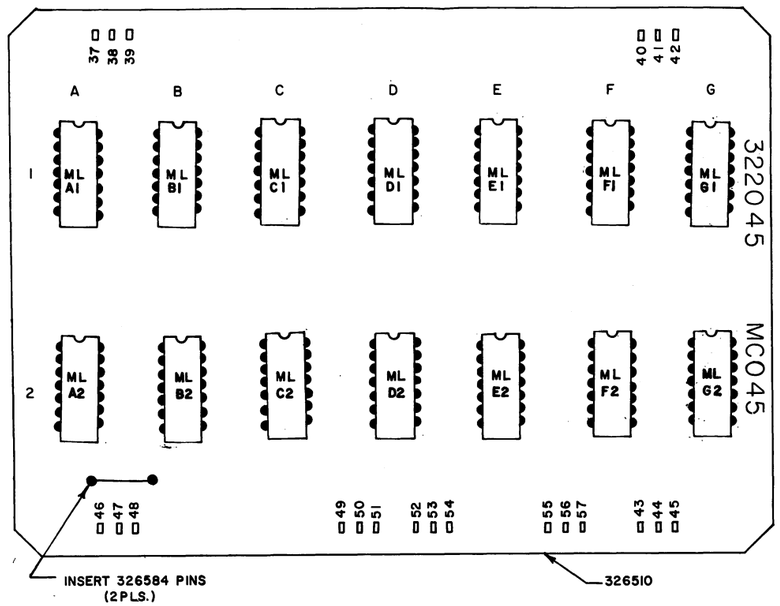
ENGD. C.A.Y. APPD.

TELETYPE CORPORATION

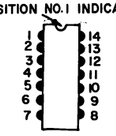
322044

TC 474 (1-66)

NO.	NOTES
1.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD. ML D 2 ROW COLUMN INTEGRATED CIRCUIT
2.	SEE SPECIFICATION MR2.001 FOR CIRCUIT BOARD REQUIREMENTS
3.	REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY 81508S.
4	ASSOCIATED SCHEMATICS ARE: 8375 W D.
5.	STRAP TO BE ADDED AFTER TESTING HAS BEEN COMPLETED.



TOP VIEW DUAL-INLINE
POSITION NO.1 INDICATOR



CIRCUIT CARD MC045

REF. DESIG.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
MLA1	326833	2	INTEGRATED CIRCUIT 833	
MLB1			SAME AS MLA1	
MLC1	326830	3	INTEGRATED CIRCUIT 830	
MLD1	326845	1	INTEGRATED CIRCUIT 845	
MLE1	326846	7	INTEGRATED CIRCUIT 846	
MLF1			SAME AS MLE1	
MLG1			SAME AS MLE1	
MLA2			SAME AS MLC1	
MLB2			SAME AS MLC1	
MLC2	326862	1	INTEGRATED CIRCUIT 862	
MLD2			SAME AS MLE1	
MLE2			SAME AS MLE1	
MLF2			SAME AS MLE1	
MLG2			SAME AS MLE1	
	315946	21	CONTACT, CONNECTOR	
	326510	1	CIRCUIT BOARD	
	326584	2	PINS, FORMED	

322045

REVISIONS

ISSUE	DATE	AUTH. NO.
1	4-15-68	19208 R
2	1-22-69	96747

SHEET 1 OF 2 WDP

CHARACTER COUNTER

APPROVALS

R AND D	E OF M

E-NUMBER

PROD NO. 322045

DATE 1-22-68

R&D FILE G-A354 AA

DRAWN W.P.B. CHKD

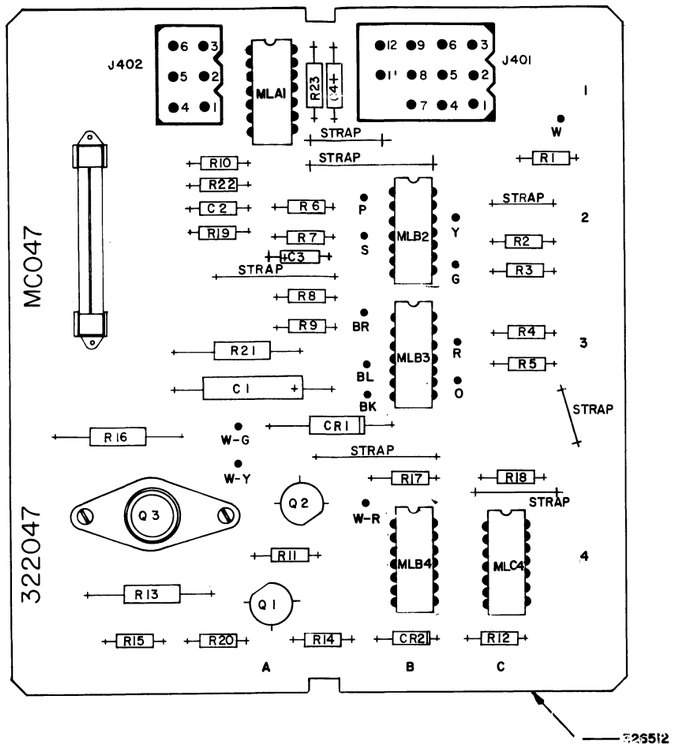
ENGD. C.A.Y. APPD.

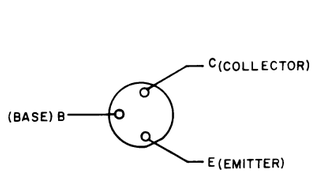
TELETYPE CORPORATION

322045

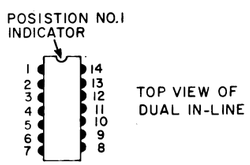
TC 637(1-67)

NO.	NOTES
1.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD. ML D 2 ROW COLUMN INTEGRATED CIRCUIT
2.	SEE SPECIFICATION MR2.001 FOR CIRCUIT BOARD REQUIREMENTS
3.	REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY 61429S
4	ASSOCIATED SCHEMATICS ARE: 8376WD.





BOTTOM VIEW OF TRANSISTOR



TOP VIEW OF DUAL IN-LINE

CIRCUIT CARD MC047

REF. DESIG.	TELETYPE PART NO	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
R1-9	315960	9	RESISTOR FIXED 5.6K 1/4W	
R11	320275	1	RESISTOR FIXED 10K 1/4W	
R12	315971	1	RESISTOR FIXED 680 OHM 1 4W	
R13	199839	1	RESISTOR FIXED 220 OHM 3W	
R14 15	321213	2	RESISTOR FIXED 1K 1 4W	
R16	326303	1	RESISTOR FIXED.68 OHM 1W	
R17 19	315958	3	RESISTOR FIXED 3.6K 1 4W	
R20 22	315948	2	RESISTOR FIXED 100 OHM 1 4W	
R21	143658	1	RESISTOR FIXED 150 OHM 1 2W	
R10,23	315972	2	RESISTOR,FIXED 22K,1/4W	
C1	326590	1	CAPACITOR 10 MFD	
C2	312385	1	CAPACITOR 0 1 MFD	
C3-4	327831	2	CAPACITOR 6.8 MFD, 6VDC	
CR1	321949	1	DIODE IN4002	
CR2	197464	1	DIODE IN914	
MLA1	326846	4	INTEGRATED CIRCUIT	
MLB2			SAME AS MLA1	
MLB3			SAME AS MLA1	
MLB4			SAME AS MLA1	
MLC4	326845	1	INTEGRATED CIRCUIT	
Q1	324656	1	TRANSISTOR 2N3569	
Q2	315931	1	TRANSISTOR 2N3638	
Q3	326594	1	TRANSISTOR 2N3767	
	39603RM	7	STRAP 1.2 INCH	
	171595	2	FUSE HOLDER	
	117176	1	FUSE 1/2 AMP. SL BL	
	182641	17	CONNECTOR PINS (MALE)	
	326584	13	CONNECTOR PINS (MALE)	
	326512	1	CIRCUIT BOARD	
	182650	1	6 PIN PLUG J402	
	182647	1	12 PIN PLUG J401	
	51637	4	SCREW 4-40	
	151880	4	NUT	
	3640	4	LOCKWASHER	

322047

REVISIONS

ISSUE	DATE	AUTH. NO.
1	3-25-68	19101-R
2	6-7-68	95788
3	8-23-68	96117
4	1-3-69	96485
5	2-27-69	96898
6	6-2-69	96898-1-RC

WDP

SHEET 1 OF 2

ANSWER BACK DRIVER

APPROVALS

P AND D	E OF M
HJK	

E-NUMBER

PROD NO 322047

DATE 12-20-67

RBD FILE G-354AA

DRAWN WPB	CHKD
ENGD. REL	APPD

TELETYPE CORPORATION

322047

TC 637(1 67)

NO. NOTES

1 INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD:

ML D 2

ROW

COLUMN

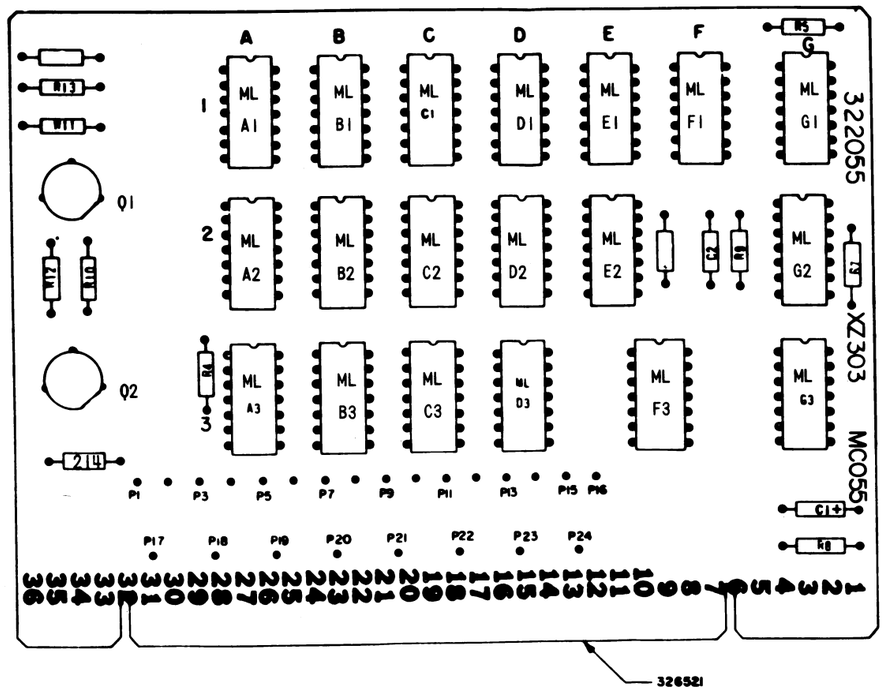
INTEGRATED CIRCUIT

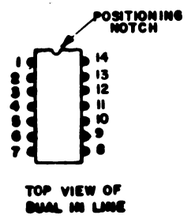
2 REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY. SEE: MR2.001 FOR CIRCUIT BOARD REQUIREMENTS.

3 SEE: 61,509S

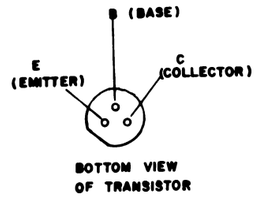
4 ASSOCIATED SCHEMATIC: 8380WD

5 STRAPS ARE TO BE ADDED AFTER TESTING HAS BEEN COMPLETED.





TOP VIEW OF DUAL IN LINE



BOTTOM VIEW OF TRANSISTOR

CIRCUIT CARD EC

REF. DESIG.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
R4-R5	315955	2	RESISTOR 2.2K OHMS	PULL-UP
R6-R9	321213	4	RESISTOR 1K OHMS	PULL-UP
	320275	2	RESISTOR 10k OHMS	BIAS
R12	315954	1	RESISTOR 1.5K OHMS	DRIVE
R13	315958	1	RESISTOR 3.6K OHMS	DRIVE
R14	137438	1	RESISTOR 100 OHMS (1/2W)	COL. LOAD
R15	315973	1	RESISTOR 3.3K OHMS	TIMING
C2	312385	1	CAPACITOR 1 MFD	TIMING
Q1	315931	1	TRANSISTOR 2N3638	AMPLIFIER
Q2	324656	1	TRANSISTOR 2N3569	AMPLIFIER
MLA1	326846	12	QUAD-2 INPUT GATE	STEERING
MLA2			SAME AS MLA1	
MLA3	326852	4	DUAL J-K FLIP-FLOP	COUNTER
MLB1			SAME AS MLA1	
MLB2			SAME AS MLA1	
MLC1			SAME AS MLA1	
MLC2			SAME AS MLA1	
MLC3			SAME AS MLA3	
MLD1			SAME AS MLA1	
MLD2			SAME AS MLA1	
MLD3			SAME AS MLA3	
MLE1			SAME AS MLA1	UP-DOWN LATCH
MLE2			SAME AS MLA1	
MLF1			SAME AS MLA1	
MLF3	326830	2	DUAL 4-INPUT GATE	ZERO STOP
MLG1	327844	1	DUAL 4-INPUT GATE	POWER PULSE
MLG2			SAME AS MLA1	
MLG3			SAME AS MLF3	
P1-24	326584	24	PIN, FORMED	
C1	327831	1	CAPACITOR 6.8 MFD	(6VDC) FILTER
	39603RM	8	STRAP 1.2" 24GA	
	326521	1	CIRCUIT BOARD	
MLB3			SAME AS MLA3	

322055

REVISIONS

ISSUE	DATE	AUTH. NO.
—3	11-15-68	96464

WDP

SHEET 1

COUNTER CONTROL

(BIDIRECTIONAL)

APPROVALS

R AND D	E OF M

E-NUMBER

PROD NO. 322055

DATE 6-11-67

R&D FILE G-A354AA

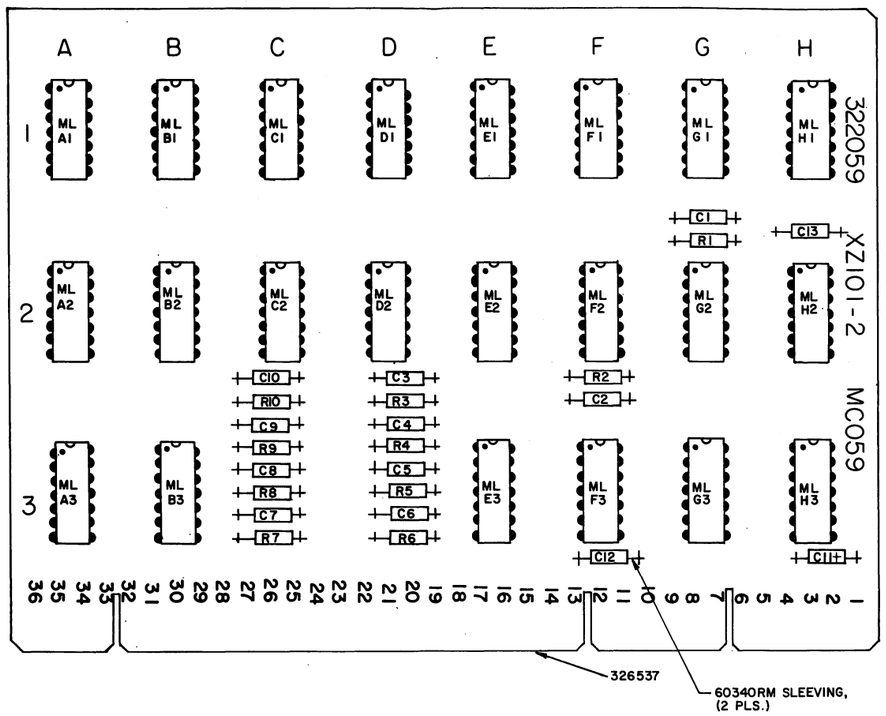
DRAWN D.P.	CHKD.
ENGD. C.A.Y.	APPD.

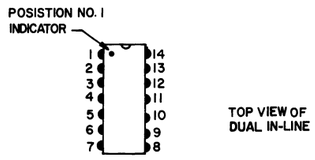
TELETYPE CORPORATION

322055

TC 474 (1-66)

NO.	NOTES
1.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD ML D 2 ROW COLUMN INTEGRATED CIRCUIT
2.	SEE SPECIFICATION MR 2.001 FOR CIRCUIT BOARD REQUIREMENTS.
3.	REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY:
4.	ASSOCIATED SCHEMATICS ARE 8371WD.
5.	CIRCUIT DESCRIPTION 8371WD-CD.
6.	ALL CHARACTERS ARE TO BE SILK SCREENED IN WHITE, RED, OR BLACK ENAMEL.
7.	CHARACTER HEIGHT .120-12 POINTS NEWS GOTHIC.





CIRCUIT CARD MC 059

REF. DESIG.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
MLA1	326853	3	INTEGRATED CIRCUIT 853	
MLA2			SAME AS MLA1	
MLA3	326852	5	INTEGRATED CIRCUIT 852	
MLB1	326833	1	INTEGRATED CIRCUIT 833	
MLB2			SAME AS MLA3	
MLB3	326846	8	INTEGRATED CIRCUIT 846	
MLC1	326830	2	INTEGRATED CIRCUIT 830	
MLC2			SAME AS MLA3	
MLD1			SAME AS MLC1	
MLD2			SAME AS MLA3	
MLE1			SAME AS MLA1	
MLE2			SAME AS MLA3	
MLE3			SAME AS MLB3	
MLF1	326862	2	INTEGRATED CIRCUIT 862	
MLF2			SAME AS MLB3	
MLF3			SAME AS MLB3	
MLG1	326832	1	INTEGRATED CIRCUIT 832	
MLG2			SAME AS MLB3	
MLG3			SAME AS MLF1	
MLH1			SAME AS MLB3	
MLH2			SAME AS MLB3	
MLH3			SAME AS MLB3	
R1-10	315948	10	RESISTOR, FIXED 100 OHM, 1/4W.	
C1,2,12,13	171583	4	CAPACITOR, .003MFD.	
C3-10	312385	8	CAPACITOR, 0.1MFD.	
C11	327831	1	CAPACITOR, 6.8MFD.	
	326537	1	CIRCUIT BOARD, ETCHED.	
	60340RM	2	SLEEVING.	

322059

REVISIONS

ISSUE	DATE	AUTH. NO.
1	3-10-69	19888 R

SHEET 1 OF 2

DISTRIBUTOR

APPROVALS

R AND D	E OF M
LBM	

E-NUMBER

PROD NO. 322059

DATE 6-18-68

R&D FILE G-A354AA

DRAWN W.P.B.	CHKD.
ENGD. A.B.	APPD.

TELETYPE CORPORATION

322059

TC 637(1-67)

NO. NOTES

1 INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD

ML D 2

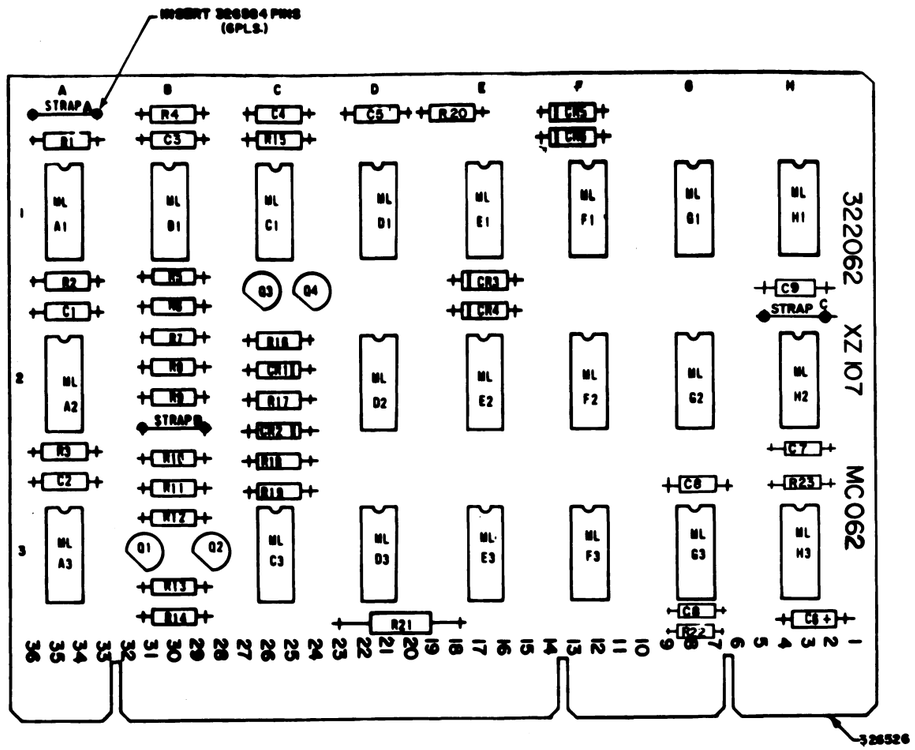
ROW
COLUMN
INTEGRATED CIRCUIT

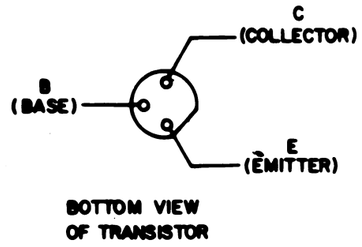
2 SEE SPECIFICATION MR2.001 FOR CIRCUIT BOARD REQUIREMENTS.

3 REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY: 61,434S

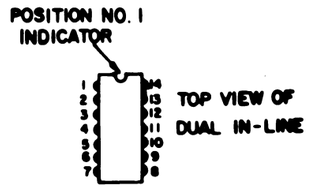
4 ASSOCIATED SCHEMATIC: 8383WD

5 STRAPS A,B, AND C ARE TO BE ADDED AFTER TESTING HAS BEEN COMPLETED.





BOTTOM VIEW OF TRANSISTOR



CIRCUIT CARD EC

REF. DESIG.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
MLA1	326862	1	INTEGR. CIRC. 862	
MLB1	326846	1	" " 846	
MLC1	326846	1	" " 846	
MLD1	326845	1	" " 846	
MLE1	396830	1	" " 830	
MLF1	326846	1	" " 846	
MLG1	326852	1	" " 852	
MLH1	326852	1	" " 852	
MLA2	326846	1	" " 846	
MLD2	326853	1	" " 853	
MLE2	326862	1	" " 862	
MLF2	326846	1	" " 846	
MLG2	326846	1	" " 846	
MLH2	326862	1	" " 862	
MLA3	326846	1	" " 846	
MLC3	326853	1	" " 853	
MLD3	326832	1	" " 832	
MLE3	326846	1	" " 846	
MLF3	326853	1	" " 853	
MLG3	326846	1	" " 846	
MLH3	326830	1	" " 830	
R1	315958	1	RES.FIXED. 3.6K	1/4W
R2	315986	1	" " 6.2K	1/4W
R3-R4	315971	2	" " 680	1/4W
R5-R6	315959	2	" " 4.7K	1/4W
R7-R10	315958	4	" " 3.6K	1/4W
R11	320275	1	" " 10 K	1/4W
R12	315958	1	" " 3.6K	1/4W
R13	315954	1	" " 1.5K	1/4W
R14	320275	1	" " 10 K	1/4W
R15.22.23	315948	3	" " 100	1/4W
R16-R17	320275	2	" " 10 K	1/4W
R18-R19	315959	2	" " 4.7K	1/4W
R20	315971	1	" " 680	1/4W
R21	182514	1	" " 91	1/2W
C1.3.7.8	312385	5	CAPACITOR .1 MFD	12V DC
C4.8.9	171583	3	" .003	100V DC
C5	312385	1	" .1 MFD	12V DC
C6	327831	1	" 6.8 MFD	6V DC
Q1	324858	1	TRANSISTOR 2N3569	
Q2	315931	1	" 2N3638	
Q3-4	324658	2	" 2N3569	
CR1-6	197464	6	DIODE IN914	
	39803RM	3	STRAP - NOTE 5	
	326584	6	FORMED PIN	
	326526	1	CIRCUIT BOARD	

322062

REVISIONS

ISSUE	DATE	AUTH. NO.
4	11-15-68	96464

WDP

SHEET 1

RECEIVE CONTROL

APPROVALS

R AND D	E OF M

E-NUMBER

PROD NO 322062

DATE 12-12-67

R&D FILE G-A354AA

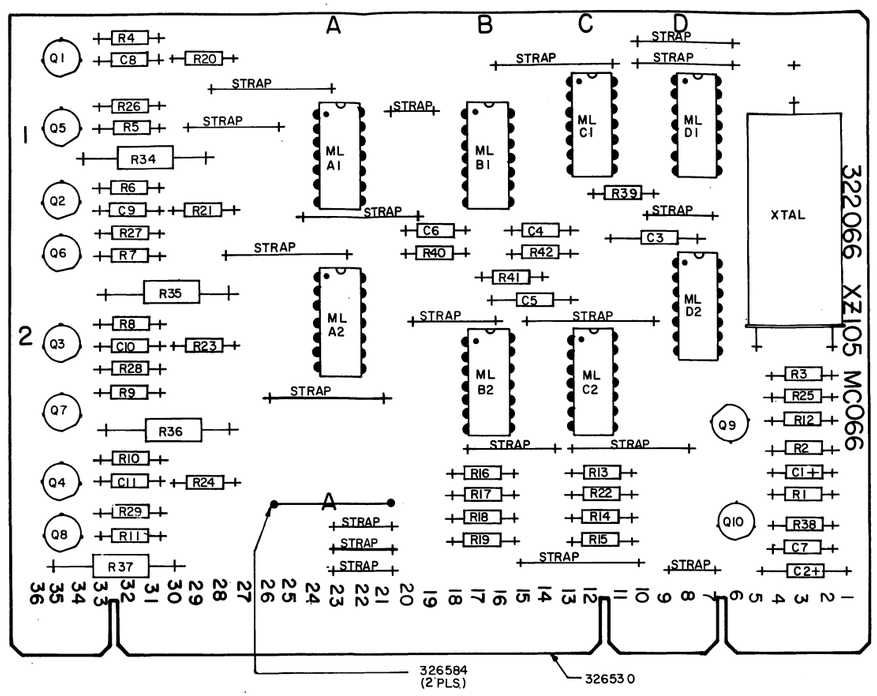
DRAWN R.J.P.	CHKD
ENGD. A.B.	APPD.

TELETYPE CORPORATION

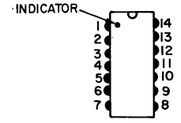
322062

TG 670 (1-66)

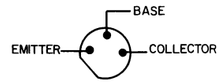
NO.	NOTES
1.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD. ML D 2 — ROW / COLUMN / INTEGRATED CIRCUIT
2.	SEE SPECIFICATION MR 2.001 FOR CIRCUIT BOARD REQUIREMENTS.
3.	S NUMBER: 61,515S
4.	ASSOCIATED SCHEMATIC: 8386 WD.
5.	STRAP A IS TO BE ADDED AFTER TESTING HAS BEEN COMPLETED.
6.	ALL CHARACTERS ARE TO BE SILK SCREENED IN WHITE, BLACK, OR RED ENAMEL.
7.	CHARACTER HEIGHT .120 - 12 POINTS NEWS GOTHIC.



TOP VIEW OF



BOTTOM VIEW OF TRANSISTOR.



CIRCUIT CARD MC 066

REF. DESIG.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
MLA1	326846	4	INTEGRATED CIRCUIT 846	
MLA2	326862	1	INTEGRATED CIRCUIT 862	
MLB1	326853	3	INTEGRATED CIRCUIT 853	
MLB2			SAME AS MLA1	
MLC1			SAME AS MLB1	
MLC2			SAME AS MLA1	
MLD1			SAME AS MLA1	
MLD2			SAME AS MLB1	
R1	315974	1	RESISTOR, FIXED 300K, 1/4W.	
R2	321510	1	RESISTOR, FIXED 51K, 1/4W.	
R3-11	320275	9	RESISTOR, FIXED 10K, 1/4W.	
R12	315959	1	RESISTOR, FIXED 4.7K, 1/4W.	
R13-24	315958	12	RESISTOR, FIXED 3.6K, 1/4W.	
R25	315956	1	RESISTOR, FIXED 2.7K, 1/4W.	
R26-29	315954	4	RESISTOR, FIXED 1.5K, 1/4W.	
R34-37	182514	4	RESISTOR, FIXED 910HM, 1/2W.	
R38-42	315947	5	RESISTOR, FIXED 510HM, 1/4W.	
C1	310926	1	CAPACITOR, 0.15MFD.	
C2	327831	1	CAPACITOR, 6.8MFD.	
C3-6	312385	4	CAPACITOR, 0.1 MFD.	
C7	315976	1	CAPACITOR, 470 PFD.	
C8-11	171583	4	CAPACITOR 0.003 MFD.	
Q1-4	315931	4	TRANSISTOR, 2N3638	
Q5-8	324656	4	TRANSISTOR, 2N3569	
Q9-10	315930	2	TRANSISTOR, 2N3568	
XTAL	327276	1	CRYSTAL, 19.2 KHZ.	
	39603RM	10	STRAP, 24AWG. 1.2"	NOTE 5
	39603RM	4	STRAP, 24AWG. 0.7"	
	39603RM	4	STRAP, 24AWG. 0.9"	
	39603RM	2	STRAP, 24AWG. 0.6"	
	326584	2	PIN, FORMED	
	326530	1	CIRCUIT BOARD	

322066

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	3-25-68	19127-R
2	6-7-68	95788
3	6-17-68	95839
4	8-15-68	96098
5	10-22-68	96395
6	1-22-69	96747

WDP

SHEET 1 OF 2

ASR MODE CONTROL

APPROVALS

R AND D	E OF M
HSK	

E-NUMBER

PROD NO. 322066

DATE 9-20-68

R&D FILE G-A354AA

DRAWN W P B | CHKD.

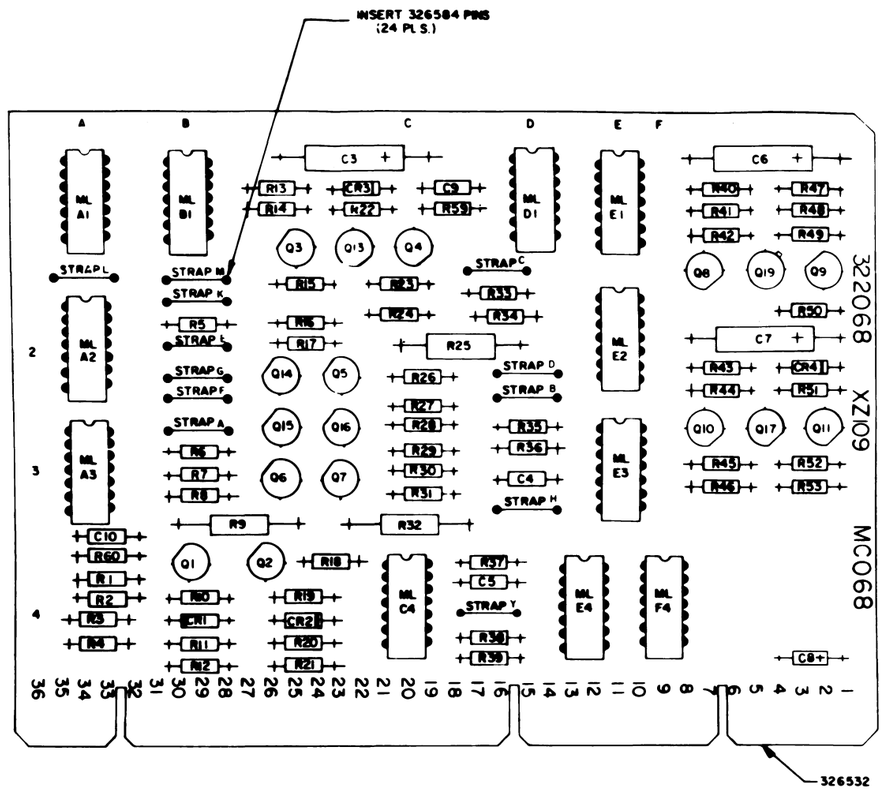
ENGD. C A Y | APPD.

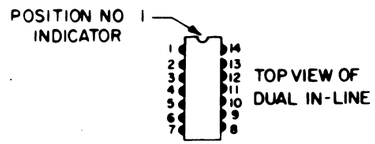
TELETYPE CORPORATION

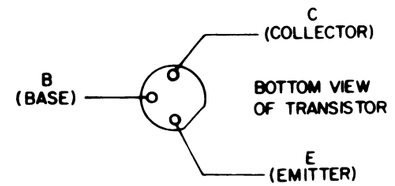
322066

TC 637 (1-67)

NO.	NOTES
1.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD ML D 2 ROW COLUMN INTEGRATED CIRCUIT
2.	SEE SPECIFICATION MRE.001 FOR CIRCUIT BOARD REQUIREMENTS
3.	REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY 65213
4.	ASSOCIATED SCHEMATICS ARE : 0388WB.
5.	STRAPS ARE TO BE ADDED AFTER TESTING HAS BEEN COMPLETED.







CIRCUIT CARD MC 068

REF DESIG.	TELETYPE PART NO	TOTAL QTY	NAME AND DESCRIPTION	LOCATING FUNCTION
MLA1	326845	1	INTEGRATED CIRCUIT 845	
MLB1	326845	1	INTEGRATED CIRCUIT 845	
MLD1	326830	1	INTEGRATED CIRCUIT 830	
MLE1	326846	1	INTEGRATED CIRCUIT 846	
MLA2	326846	1	INTEGRATED CIRCUIT 846	
MLE2	326862	1	INTEGRATED CIRCUIT 862	
MLA3	326846	1	INTEGRATED CIRCUIT 846	
MLE3	326836	1	INTEGRATED CIRCUIT 836	
MLC4	326862	1	INTEGRATED CIRCUIT 862	
MLE4	326846	1	INTEGRATED CIRCUIT 846	
MLF4	326846	1	INTEGRATED CIRCUIT 846	
R1-4	315958	4	RESISTOR,FIXED 3.6K 1/4w	
R55	315947	1	RESISTOR,FIXED 51 Ω 1/4w	
R5	315958	1	RESISTOR,FIXED 3.6K 1/4w	
R6	320275	1	RESISTOR,FIXED 10K 1/4w	
R7	315954	1	RESISTOR,FIXED 1.5K 1/4w	
R8	320275	1	RESISTOR,FIXED 10K 1/4w	
R9	182514	1	RESISTOR,FIXED 91 Ω 1/2w	
R10	315959	1	RESISTOR,FIXED 4.7K 1/4w	
R11	320275	1	RESISTOR,FIXED 10K 1/4w	
R12	315959	1	RESISTOR,FIXED 4.7K 1/4w	
R13	320275	1	RESISTOR,FIXED 10K 1/4w	
R14	315948	1	RESISTOR,FIXED 100 Ω 1/4w	
R15	315954	1	RESISTOR,FIXED 1.5K 1/4w	
R16	320275	1	RESISTOR,FIXED 10K 1/4w	
R17	315955	1	RESISTOR,FIXED 2.2K 1/4w	
R18	315958	1	RESISTOR,FIXED 3.6K 1/4w	
R19	315959	1	RESISTOR,FIXED 4.7K 1/4w	
R20	320275	1	RESISTOR,FIXED 10K 1/4w	
R21-3	315959	3	RESISTOR,FIXED 4.7K 1/4w	
R24	320275	1	RESISTOR,FIXED 10K 1/4w	
R25	171441	1	RESISTOR,FIXED 560 Ω 1w	
R26	315954	1	RESISTOR,FIXED 1.5K 1/4w	
R27	320275	1	RESISTOR,FIXED 10K 1/4w	
R28	315958	1	RESISTOR,FIXED 3.6K 1/4w	
R29	320275	1	RESISTOR,FIXED 10K 1/4w	
R30	315954	1	RESISTOR,FIXED 1.5K 1/4w	
R31	320275	1	RESISTOR,FIXED 10K 1/4w	
R32	182514	1	RESISTOR,FIXED 91 Ω 1/2w	
R33	320275	1	RESISTOR,FIXED 10K 1/4w	
R34-5	315958	2	RESISTOR,FIXED 3.6K 1/4w	
R36-7	315971	2	RESISTOR,FIXED 680 Ω 1/4w	
R38-9	315958	2	RESISTOR,FIXED 3.6K 1/4w	
R40-1	315948	2	RESISTOR,FIXED 100 Ω 1/4w	
R42	315959	1	RESISTOR,FIXED 4.7K 1/4w	
R43	321545	1	RESISTOR,FIXED 12K 1/4w	
R44	315948	1	RESISTOR,FIXED 100 Ω 1/4w	
R45	315954	1	RESISTOR,FIXED 1.5K 1/4w	
R46	320275	1	RESISTOR,FIXED 10K 1/4w	
R47	315952	1	RESISTOR,FIXED 820 Ω 1/4w	
R48	326601	1	RESISTOR,FIXED 150K 1/4w	
R49	326598	1	RESISTOR,FIXED 56 Ω 1/4w	
R50	315959	1	RESISTOR,FIXED 4.7K 1/4w	
R51	320275	1	RESISTOR,FIXED 10K 1/4w	
R52-3	315959	2	RESISTOR,FIXED 4.7K 1/4w	
R60	315947	1	RESISTOR,FIXED 51 Ω 1/4w	
Q1-11	324656	11	TRANSISTOR 2N3569	
Q13-17	315931	5	TRANSISTOR 2N3638	
Q19	321512	1	TRANSISTOR 2N2646	
CR1-4	197464	4	DIODE 1N914	
C9	312385	1	CAPACITOR .1 MFD 10V DC	
C3	326592	1	CAPACITOR 33 MFD	
C4-5	312385	2	CAPACITOR 1 MFD 10V DC	
C6	326592	1	CAPACITOR 33 MFD 35V DC	
C7	300027	1	CAPACITOR 15 MFD 35V DC	
C10	312385	1	CAPACITOR 1 MFD 10V DC	
	39603RM	12	STRAP .700 24 AWG NOTE 5	
	326584	24	FORMED PIN	
	326532	1	CIRCUIT BOARD	
C8	327831	1	CAPACITOR 6.8 MFD 6V DC	

322068

REVISIONS

ISSUE	DATE	AUTH. NO.
5	8-2-68	95997
5A	1-22-69	96747
5B	1-23-69	96771
6	11-15-68	96464
7	2-19-69	96464-1

SHEET 1 OF 2

CHANNEL CONTROL

APPROVALS

R AND D	[illegible] M
L&M	

E NUMBER

PROD NO 322068

DATE 1 2 68

RBD FILE G A354AA

DRAWN W P B	CHKD
ENGD C A Y	APPD D E H

TELETYPE CORPORATION

322068

TC 687(1-67)

NO. NOTES

1 INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD

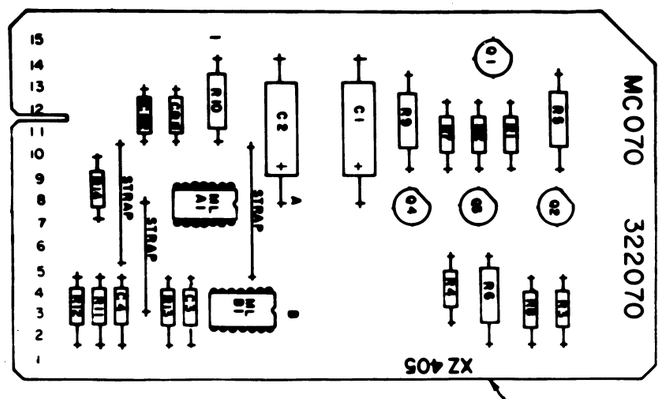
ML D 2

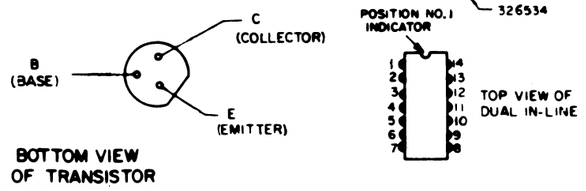
ROW
COLUMN
INTEGRATED CIRCUIT

2 SEE SPECIFICATION MR2.001 FOR CIRCUIT BOARD REQUIREMENTS.

3 REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY: 61,510S

4 ASSOCIATED SCHEMATIC IS 8389WD





THIS IS NOT USED ON SERIES CARDS

CIRCUIT CARD EG

	REF. DESIG.	TELETYPE PART NO.	NOMN. QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
R1,2,3,4		320775	4	RES., FIXED 10K	1/4W
	R5	137602	1	" " 470	1/2W
	R7, R8	321213	2	" " 1K	1/4W
R9,R10,R11,R12		182514	3	" " 91	1/2W
		315958	2	" " 3.6K	1/4W
	R13	315871	1	" " 680	1/4W
	R6	137439	1	" " 820	1/2W
	C1, C2	326580	2	CAPACITOR .10 MFD	50V DC
	C3	312385	1	" 0.1 MFD	10V DC
	C4	327831	1	" 6.8 MFD	6V DC
CR1,CR2		321949	2	DIODE IN4002	
	Q1, Q2	315931	2	TRANSISTOR 2N3638	
	Q3, Q4	324656	2	" 2N3568	
	MLA1	326846	1	INTEGR. CIRC. 846	
	MLB1	326862	1	" " 862	
		39603BM	2	STRAPS 1.20"	
		39603BM	1	1.15"	
		326534	1	CIRCUIT BOARD	

322070

REVISIONS

ISSUE	DATE	AUTH. NO.
4	11-15-68	86565

SHEET 1

TWO COLOR
RIBBON
CONTROL

APPROVALS

R AND D	E OF M
LEM	

E-NUMBER

PROD NO 322070

DATE 11-14-67

R&D FILE G-A354AA

DRAWN W.P.B. CHKD

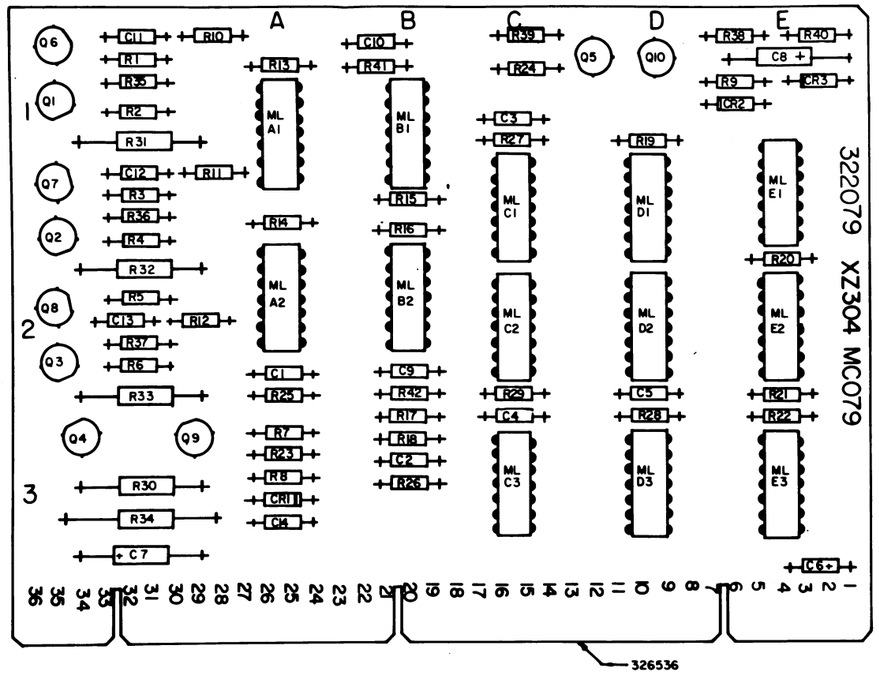
ENGD. R.E.L. APPD

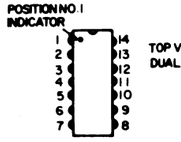
TELETYPE
CORPORATION

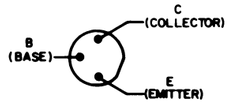
322070

TC 474 1-66)

NO	NOTES
1.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD ML D 2 ROW COLUMN INTEGRATED CIRCUIT
2.	REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY. SEE MR2001 FOR CIRCUIT BOARD REQUIREMENT.
3.	REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY. 61,520S
4.	ASSOCIATED SCHEMATICS : 8395WD







*R 30 IS 470 OHMS ON SOME CARDS

CIRCUIT BOARD EC

REF. DESIG.	TELETYPE PART NO	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
MLA1	326846	8	INTEGRATED CIRCUIT 846	
MLB1	326845	2	INTEGRATED CIRCUIT 845	
MLC1			SAME AS MLA1	
MLD1			SAME AS MLA1	
MLE1			SAME AS MLB1	
MLA2			SAME AS MLA1	
MLB2			SAME AS MLA1	
MLC2			SAME AS MLA1	
MLD2	326836	2	INTEGRATED CIRCUIT 836	
MLE2	326862	1	INTEGRATED CIRCUIT 862	
MLC3			SAME AS MLA1	
MLD3			SAME AS MLA1	
MLE3			SAME AS MLD2	
R1-R9	320275	9	RESISTOR,FIXED 10K,1/4W	
R10-22	315958	13	RESISTOR,FIXED 3.6K 1/4W	
R23-24	321213	2	RESISTOR,FIXED 1K,1/4W	
R25-29	315947	7	RESISTOR,FIXED 51 1/4W	
R30	137439	2	RESISTOR,FIXED 820* 1/2W	
R31-34	182514	4	RESISTOR,FIXED 91 1/2W	
R35-38	315954	4	RESISTOR,FIXED 1.5K 1/4W	
R39	315956	1	RESISTOR,FIXED 2.7K 1/4W	
R40	315959	1	RESISTOR,FIXED 4.7K 1/4W	
R41-42			SAME AS R25	
C1-5	312385	7	CAPACITOR, 0.1 MFD,10VDC	
C6	327831	1	CAPACITOR,6.8 MFD,6V DC	
C7	326590	1	CAPACITOR,10 MFD,50V DC	
C8	326591	1	CAPACITOR,3.9 MFD,35VDC	
C9-10			SAME AS C1	
C11-14	171583	4	CAPACITOR,.003MFD	
CR1	321949	1	DIODE, IN4002	
CR2-3	197464	2	DIODE, IN914	
Q1-5	324656	5	TRANSISTOR, 2N3569	
Q6-10	315931	5	TRANSISTOR, 2N3638	
	326536	1	CIRCUIT BOARD	

322079

REVISIONS

ISSUE	DATE	AUTH. NO.
1	5-3-68	19260-R
2	6-7-68	95788
3	8-15-68	96119
4	10-4-68	96309
5	11-15-68	96464

SHEET 1 OF 2 WDP

ALARMS AND AUTOMATIC CONTROLS

APPROVALS

R AND D	E OF M
AJR	

E-NUMBER

PROD NO 322079

DATE 7 2 68

R&D FILE G A1566AA

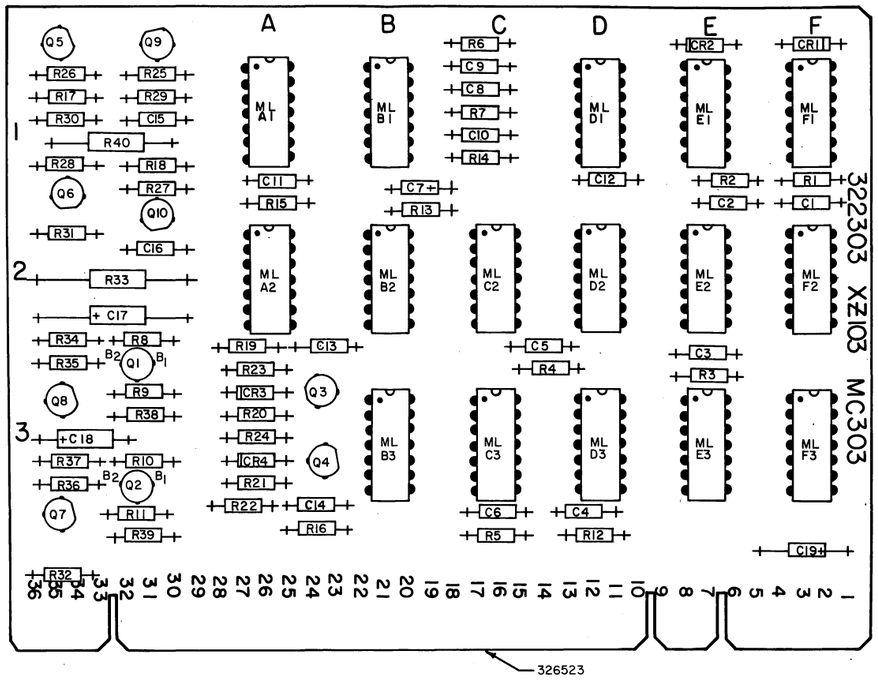
DRAWN JPH	CHKD
ENGD TAY	APPD

TELETYPE CORPORATION

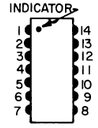
322079

TC 697(11-67)

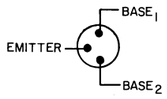
NO.	NOTES
1.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD. ML A I ROW COLUMN INTEGRATED CIRCUIT
2.	SEE SPECIFICATION MR 2.001 FOR CIRCUIT BOARD REQUIREMENTS.
3.	S-NUMBER 61,617S.
4.	ASSOCIATED SCHEMATIC; 8772 WD.
5.	ALL CHARACTERS TO BE SILK SCREENED IN WHITE, RED, OR BLACK ENAMEL.
6.	CHARACTER HEIGHT .120 -12POINTS NEWS GOTHIC.



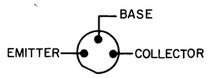
TOP VIEW OF DUAL IN-LINE
POSITION NO.1 INDICATOR



BOTTOM VIEW OF UNIJUNCTION (Q1,Q2).



BOTTOM VIEW OF TRANSISTOR (TYPICAL)



CIRCUIT CARD MC303

REF. DESIG.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
MLA1	326836	4	INTEGRATED CIRCUIT 836	
MLA2	326846	6	INTEGRATED CIRCUIT 846	
MLB1			SAME AS MLA2	
MLB2			SAME AS MLA1	
MLB3	326862	2	INTEGRATED CIRCUIT 862	
MLC2	326830	4	INTEGRATED CIRCUIT 830	
MLC3			SAME AS MLA2	
MLD1			SAME AS MLB3	
MLD2			SAME AS MLA2	
MLD3			SAME AS MLA1	
MLE1			SAME AS MLC2	
MLE2			SAME AS MLC2	
MLE3			SAME AS MLA2	
MLF1			SAME AS MLC2	
MLF2			SAME AS MLA1	
MLF3			SAME AS MLA2	
RI-11	315947	11	RESISTOR, FIXED 51 OHM, 1/4W.	
RI2-15	315948	4	RESISTOR, FIXED 100 OHM, 1/4W.	
RI6-18	315958	3	RESISTOR, FIXED 3.6K, 1/4W.	
RI9-22	315959	4	RESISTOR, FIXED 4.7K, 1/4W.	
R23-28	320275	6	RESISTOR, FIXED 10K, 1/4W.	
R29-30	315954	2	RESISTOR, FIXED 1.5K, 1/4W	
R31-32	315955	2	RESISTOR, FIXED 2.2K, 1/4W.	
R33	171441	1	RESISTOR, FIXED 5600HM, 1W.	
R34	321510	1	RESISTOR, FIXED 51K, 1/4W.	
R35-36	315953	2	RESISTOR, FIXED 1.2K, 1/4W.	
R37	315974	1	RESISTOR, FIXED 300K, 1/4W.	
R38-39	326602	2	RESISTOR, FIXED 360 OHM, 1/4W.	
R40	182514	1	RESISTOR, FIXED 91 OHM, 1/2W.	
CI-6,8-11	312385	10	CAPACITOR, 0.1MFD, 10VDC.	
CI2-16	171583	5	CAPACITOR, 0.003, 75VDC.	
CI7-18	326591	2	CAPACITOR, 3.9 MFD. 35VDC.	
C7,19	327831	2	CAPACITOR, 6.8 MFD. 6VDC.	
CRI-4	197464	4	DIODE IN914.	
QI-2	327812	2	TRANSISTOR, MU4894	
Q3-8	324656	6	TRANSISTOR, 2N3569	
Q9-10	315931	2	TRANSISTOR, 2N3638	
	326523	1	CIRCUIT BOARD	

322303

REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-20-68	19777 R

SHEET 1 OF 2

A.S.R.
SEND CONTROL

APPROVALS

R AND D	E OF M
LDM	

E-NUMBER

PROD NO. 322303

DATE 10-7-68

R&D FILE G-A354AA

DRAWN W.P.B.	CHKD.
ENGD. C.A.Y.	APPD.

TELETYPE
CORPORATION

322303

WIRING DIAGRAM PACKAGE FOR CIRCUIT CARD SET 332563 (RT MODULE)

WDP0128

DRAWING NO.	SHEET NO.	DESCRIPTION	ISSUE NUMBER 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
7856WD	1	OPTION ANALYSIS CHART	2	2																												
8399WD	1	TRUTH TABLES AND LOGIC SYMBOLS	1	1																												
8370WD	ICR	SCHEMATIC RECEIVING DEVICE	1	1																												
8370WD	1	SCHEMATIC RECEIVING DEVICE	1	1																												
8379WD	ICR	SCHEMATIC READER DRIVER	1	1																												
8379WD	1	SCHEMATIC READER DRIVER	1	1																												
8379WD	2	SCHEMATIC READER DRIVER	1	1																												
8379WD	3	SCHEMATIC READER DRIVER	1	1																												
303149	1	CIRCUIT CARD RECEIVING DEVICE	4A	6																												
322054	1	CIRCUIT CARD READER DRIVER	4	4																												
8370WD	CD - ALL	CIRCUIT DESCRIPTION--RECEIVING DEVICE	1	1																												
8379WD	CD - ALL	CIRCUIT DESCRIPTION--READER DRIVER	1	1																												

NOTE : THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF WDP.

NO.	NOTES
1	THE FOLLOWING PROCEDURE SHOULD BE FOLLOWED WHEN INSTALLING CIRCUIT CARD OPTIONS: A. TURN POWER OFF B. LOCATE CARD POSITION GIVEN IN INSTALLATION PROCEDURE. C. CHECK POLARITY OF CARDS (NOTCHES) AGAINST POLARITY OF CARD CONNECTOR. (SMALL TAB IN CONNECTOR) D. INSTALL CARD.
2.	THE FOLLOWING PROCEDURE SHOULD BE FOLLOWED WHEN INSTALLING CABLE OPTIONS: A. TURN POWER OFF. B. IDENTIFY WIRES AND TERMINALS TO BE CONNECTED PER INSTALLATION PROCEDURE. C. INSTALL PUSH-ON TERMINAL CONTACTS DIRECTLY OVER ALLOTTED TERMINALS ON WIRING FIELD TERMINAL BOARD. D. DO NOT SHORT OR BEND TERMINALS ON WIRING FIELD TERMINAL BOARD.
3.	IN REMOVING CIRCUIT CARD STRAP OPTIONS CARE SHOULD BE TAKEN TO AVOID: A. DAMAGE TO ADJACENT COMPONENTS AND CIRCUIT BOARD. B. SHORTING REMAINING PORTION OF STRAP TO ADJACENT CIRCUITS. C. LITTERING CARD WITH CUT STRAPS.
4	IN ADDING CIRCUIT CARD STRAP OPTIONS TO PREVIOUSLY PROGRAMMED CARDS, A SOLDERING IRON NOT LARGER THAN 25 WATTS SHOULD BE USED. CARE SHOULD BE TAKEN TO AVOID DAMAGING ADJACENT COMPONENTS OR CIRCUIT BOARD.
5.	REFERENCES TO 8365WD, PRINTER, AND STUNT BOXES INDICATE THAT OPTION IS PART ELECTRICAL AND MECHANICAL.

SERVICE UNIT OPTION ARRANGEMENTS	DESCRIPTION	APPLICATION	ASSEMBLY AFFECTED	INSTALLATION PROCEDURE
X	CHARACTER COUNTER & CONTROL	ASR	322045	INSTALL PIGGY-BACK ON CARD ASSEMBLY 322045 POSITION XZ 301. 1. REMOVE STRAP "A" WHEN "NU-LINE" IS NOT IMPLEMENTED IN PRINTER.
			322055	INSTALL IN POSITION XZ303. 1. PROGRAM P1-P24 FOR A COUNT OF 66 AS FOLLOWS, STRAP P3-P18, P6-P19, P8-P20, P10-P21, P12-P22, P13-P23, P2-P17 2. FOR OTHER COUNTS REFER TO 8380WD-CD.
X	10/11 UNIT CODE 150 WPM.	RO/KSR ASR	322067 322066	PROGRAM CIRCUIT CARD ASSEMBLY AFFECTED. POSITION XZ 105 AS FOLLOWS: 1. 10 UNIT DO NOT REMOVE STRAP "A".
X	HALF & FULL DUPLEX	KSR/ASR	322062	PROGRAM CIRCUIT CARD ASSEMBLY AFFECTED POSITION XZ 107 AS FOLLOWS: (FIELD MODIFICATION ONLY, CARD TO BE SHIPPED WITH ALL STRAPS. 1. DEDICATED HALF DUPLEX - REMOVE STRAPS "B" 2. DEDICATED FULL DUPLEX - REMOVE STRAPS "A" 3. LINE CONTROL OPERATION - REMOVE STRAPS "A B & C". 4. CHECK MECHANICAL PORTIONS OF STUNT BOX FOR APPROPRIATE CODES.
X	RECEIVER STATUS ALARM	KSR/ASR	322062	1. REMOVE STRAP "C"
X	MOTOR CONTROL (DATAPHONE) EOT AND ALARM DISCONNECT.	RO/KSR/ASR	322068	PROGRAM CIRCUIT CARD ASSEMBLY AFFECTED POSITION XZ 109 AS FOLLOWS: 1. REMOVE STRAPS "D, E, G, H, K, M, Y." DO NOT REMOVE STRAPS "A, B, C, F, L".
X	AUTOMATIC READER AND PUNCH CONTROL.	ASR	322079	1. INSTALL CIRCUIT CARD ASSEMBLY IN POSITION XZ 304. 2. PROGRAM CONTROL PANEL PER 8365 WD. 3. CHECK MECHANICAL PORTIONS OF STUNT BOX FOR APPROPRIATE CODES.
			322054	REMOVE STRAP "A" OF CIRCUIT CARD ASSEMBLY POSITION XZ 108 OF R-T ELECTRICAL SERVICE UNIT.
X	TWO COLOR RIBBON.	RO/KSR/ASR	322070	1. INSTALL CIRCUIT CARD ASSEMBLY AFFECTED IN POSITION XZ 405. 2. CHECK PRINTER AND STUNT BOX FOR APPROPRIATE MECHANISM & CODES.
X	ANSWER BACK	RO/KSR/ASR	327801	1. INSTALL THIS SELF CONTAINED ASSEMBLY IN POSITIONS XZ 310-XZ 315. 2. INSTALL CABLE ASSEMBLY 326575 AS FOLLOWS: WIRE COLOR — TBIII CONNECTION. WHITE-BROWN — A 1 WHITE-RED — A 2 WHITE-ORANGE — A 3 WHITE-YELLOW — A 4 WHITE-GREEN — A 5 WHITE-BLUE — A 6 WHITE-PURPLE — A 7 WHITE-SLATE — A 8 WHITE-BLACK — A 11 GREEN-SLATE — J 3 BLUE-GREEN — H 3 ORANGE-GREEN — F 3 RED-BLUE — C 3 YELLOW — A 13 GREEN — A 14 BLACK — G 3 BLUE — A 10 BROWN — D 3 BROWN — E 3

7856 WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	11-21-68	19778 R
2	3-17-69	96904

WDP

MODEL 37
OPTION
ANALYSIS CHART

APPROVALS

D AND R	E OF M
fDm	

E-NUMBER

PROD. NO. 7856 WD.

DATE 9-4-68

P.D. FILE NO. G-A354AA

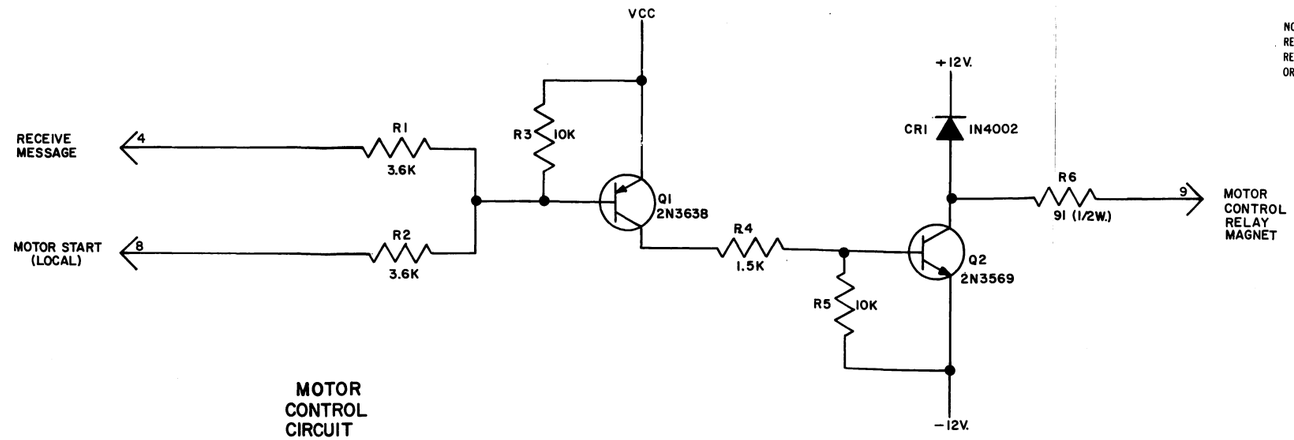
DRAWN W.P.B. CHKD.

ENGD. M.J.R. APPD.

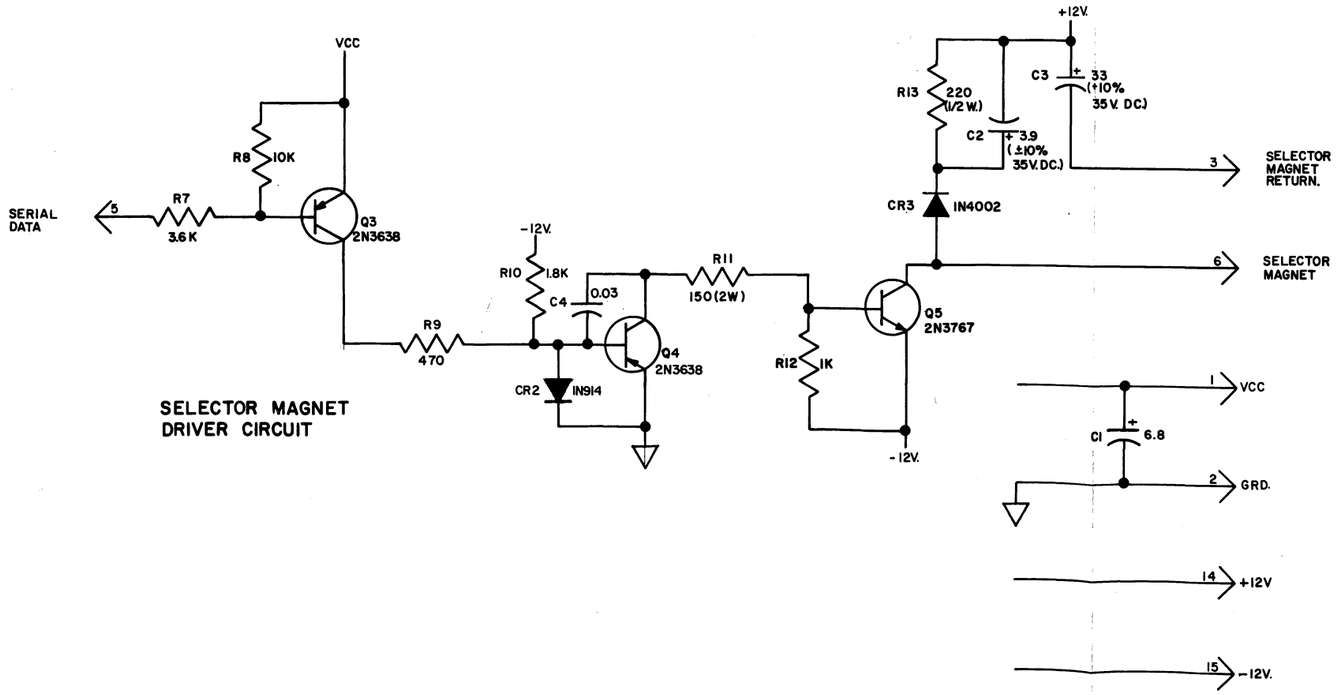
TELETYPE CORPORATION

7856 WD

NO.	NOTES
1.	ALL VOLTAGES DC. UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
5.	INDICATES FEMALE AND INDICATES MALE TERMINAL
6.	REFER TO 303149 FOR ASSEMBLY INFORMATION.
7.	S NUMBER: 61,428 S.
8	REFERENCE CIRCUIT DESCRIPTION: 8370WD-CD.
9.	INDICATES CIRCUIT GROUND.



MOTOR CONTROL CIRCUIT



SELECTOR MAGNET DRIVER CIRCUIT

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8370WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET - 1

SCHEMATIC WIRING DIAGRAM FOR RECEIVING DEVICE

APPROVALS	
D AND R	E OF M
H.P.K	

E-NUMBER	
PROD. NO.	8370 WD.
DATE	2-29-68
P.D. FILE NO.	G-A354AA
DRAWN W.P.B.	CHKD.
ENGD. C.A.Y.	APPD.

TELETYPE CORPORATION

8370WD

TC 456 (2-68)

CIRCUIT DESCRIPTION OF THE RECEIVING DEVICE LOGIC CARD (ASSEMBLY NUMBER 303149)

TABLE OF CONTENTS

201

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF THE RECEIVING DEVICE LOGIC CARD (ASSEMBLY NUMBER 303149)

SECTION I

GENERAL TECHNICAL DATA

1. BASIC FUNCTION

1.1 The 303149 Receiving Device Logic card combines the function of a selector magnet driver and a motor control relay driver.

1.2 Selector Magnet Driver

The selector magnet driver sinks a steady state current of up to 600 ma DC on a MARK input and sinks zero current on a SPACE input. The MARK input is a logic one, and a SPACE input is a logical zero.

1.3 Motor Control

The motor control relay driver is capable of supplying a current of 40 to 60 ma to operate the motor control relay. The relay will be operated on a logic zero input and released on a logic one input.

2. GENERAL TECHNICAL DATA

2.1 Input-Output Data

2.1.1 The Receiving Device Logic card converts the integrated circuit logic levels to current levels appropriate for magnet operation.

A logic one is defined as a voltage level between 5.0 Volts and 6.6 Volts (usually a logic one approximates the integrated circuit supply voltage). A logic one draws no current from the input of the logic element. 202

Signal voltages between circuit ground potential and +0.5 Volts are considered logic zero.

2.2 Input-Output Characteristics

Motor Control

2.2.1 Receive Message/Motor Start Local (Pins 4 and 8)

These two inputs are connected together in a logical or configuration. A logic zero input will energize the associated motor control relay. Input impedance is 3.6K.

2.2.2 Motor Control Relay Magnet (Pin 9)

The associated motor control relay is connected to this output (typical coil resistance 430 ohms). The output impedance is 91 ohms in series with a -12 Volts. The relay driver output is capable of supplying up to 60 ma of current. Relay magnet drop-out is diode suppressed.

Selector Magnet Driver

2.2.3 Send Data (Pin 5)

Under the control of set logic this input is supplied with MARK and SPACE signals corresponding to received data. A logic one signal (MARK) will cause the selector magnet to be energized. A logic zero signal (SPACE) will de-energize the selector magnet. Input and impedance is 3.6K.

2.2.4 Selector Magnet (Pin 6)

The negative end of the selector magnet is connected to this output which will establish a discharge path through a Diode coupled resistor capacitor network. Typical dropout time is approximately 2.50 milliseconds.

2.2.5 Selector Magnet Return (Pin 3)

The positive end of the selector magnet is connected to this output. In series with the selector-coil is a parallel resistor capacitor network which permits maximum current through the coil during SPACE to MARK transitions. Typical MARK hold current is approximately 600 milliamperes. Nominal rise time is 2.25 milliseconds. Typical load supplied is 3.5 ohms 20 millihenries inductance.

2.3 Mechanical Requirements

The motor control amplifier and the selector magnet driver are mounted on a 15-pin circuit board.

2.4 Power Requirements

203

D.C. Supply	Current Required
+5.0V to +5.50V (+5.25V Nom.)	0 to 20 ma
+11.65 to +13.75V (+12.5V Nom.)	0 to 660 ma
-11.13V to -13.88V (-12.5V Nom.)	0 to 660 ma

2.5 Operating Temperature Range

0°C to 70°C (in free air)

2.6 Storage Temperature Range

-40°C to 70°C

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Schematic Drawing - 8370 WD.

1.2 Assembly Drawing - 303149.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 Selector Magnet Driver

2.1.1 The selector magnet driver circuit is a three stage amplifier, designed to operate full on or off without intermediate levels. The input characteristics are matched to the output of currents sinking DTL integrated circuit elements. The output circuit is matched to the characteristics of the 312936 Selector Magnet Assembly.

2.1.2 A logic one signal input, (See Section I-2.1), will turn the output on, picking up the selector magnet armature. The logic one signal turns off Q3, allowing Q4 and Q5 to be turned on. With Q5 turned on, C3 will be charged through the load impedance to give a high initial current. As C3 becomes charged, load current will be limited by the external 50 ohm, 50 watt resistor connected across C3.

2.1.3 With a logic zero signal on the input, (see Section I-2.1), Q3 will be turned on, driving the base of Q4 positive, turning off Q4 and Q5. The positive voltage on the base of Q4 is limited by ground clamp Diode CR2. With Q5 turned off, the load inductance and C3 will discharge through steering Diode CR3, and the discharge network C2, R13. The impedance values of the output circuit are chosen to provide equal selector magnet armature pickup and drop-out times. The characteristics of the(loaded) output circuit will determine the maximum signalling rate. The values chosen will give proper operation with a nominal pulse length of 6 ms or more. 204

2.2 Motor Control Relay Driver

2.2.1 The motor control relay driver is a two-stage amplifier which is designed to operate full ON or OFF without intermediate levels. This circuit is designed to drive an external motor start relay. Inputs to the motor control relay drive circuit are on Pins 4 and 8. The inputs are connected in a logical OR configuration each having an input resistance of 3.6K. With logic zero, (see Section I-2.1), applied to either input, Q1 is switched ON. This switches Q2 ON, energizing the relay. With logic one applied at both inputs Q1 and Q2 are switched OFF. When Q2 is switched OFF, any positive voltage transient developed by the inductive load will be clamped to the positive supply voltage by CR1.

ISSUE CONTROL RECORD

8379WD

NO.	NOTES

SUPPORTING INFORMATION	
CATEGORY	NO.

CONTENTS

SHEET NO.	ISSUE 2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
1																		
2																		
3																		
CD0																		
CD1																		
CD2																		
CD3																		
CD4																		
CD5																		
CD6																		
CD7																		
CD8																		
CD9																		
CD10																		
CD11																		

REVISIONS APPLYING TO THIS CONTROL RECORD

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

ISSUE CONTROL SHEET 1 OF 1

SCHEMATIC
WIRING DIAGRAM
FOR
READER DRIVER

WD NUMBER 8379

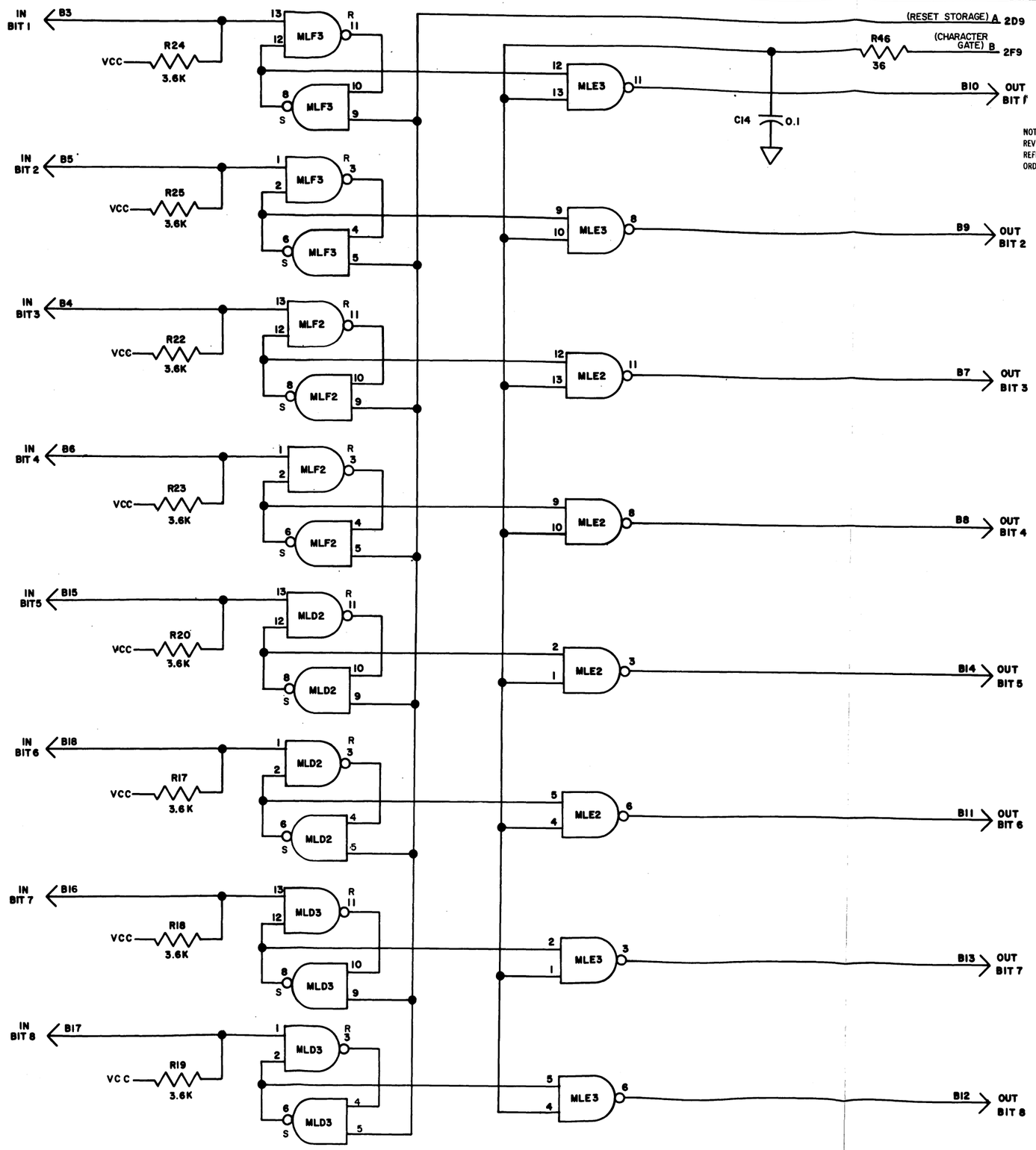
DRAWN	CHKD.
ENGD.	APPD.

TELETYPE CORPORATION

8379 WD

TC 626 (1-66) SEE R&D ROUTINE 5 FOR USE OF THIS FORM

NO.	NOTES
1.	ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
4.	INDICATES FEMALE TERMINAL AND INDICATES MALE TERMINAL
5.	REFER TO 322064 FOR ASSEMBLY INFORMATION.
6.	S NUMBER:
7.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD: ML A 2 — ROW, COLUMN, INTEGRATED CIRCUIT
8.	THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC AND 0V, RESPECTIVELY.
9.	LOGIC NEGATION - A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
10.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER, THE GATE IS USED AS AN INVERTER.
11.	VCC IS PROVIDED TO THE INTEGRATED CIRCUITS ON PIN 14 AND GROUND ON PIN 7, THIS APPLIES TO ALL PACKAGES.
12.	REFER TO 8399WD FOR TRUTH TABLES.
13.	CROSS REFERENCE NOTATION ON SCHEMATIC: 3 B 4 — ROW, COLUMN, SHEET
14.	OPTIONS: A-ENABLES MANUAL CONTROL WHEN 322079 CIRCUIT CARD IS NOT USED. REMOVE STRAP WHEN ABOVE CIRCUIT CARD IS USED.
15.	ABBREVIATIONS USED: MDL- MAGNET DRIVER LATCH. OSL-ONE STEP LATCH. CSL-CHARACTER STORED LATCH. RSL-RECEIVER SELECTABLE LATCH. TOL- TAPE OUT LATCH
16.	REFERENCE CIRCUIT DESCRIPTION 8379WD-CD.
17.	INDICATES CIRCUIT GROUND.



NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8379WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 1

SCHEMATIC WIRING DIAGRAM FOR READER DRIVER.

APPROVALS	
D AND R	E OF M
HBK	

E-NUMBER	
PROD. NO.	8379WD
DATE	4-17-68
P.D. FILE NO.	G-A354AA
DRAWN RJP	CHKD.
ENGD. CAY	APPD.

TELETYPE CORPORATION

8379WD

TC 494 (5-68)

SEE SHEET 1 FOR NOTES

8379WD		
REVISIONS		
ISSUE	DATE	AUTH. NO.
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SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 2

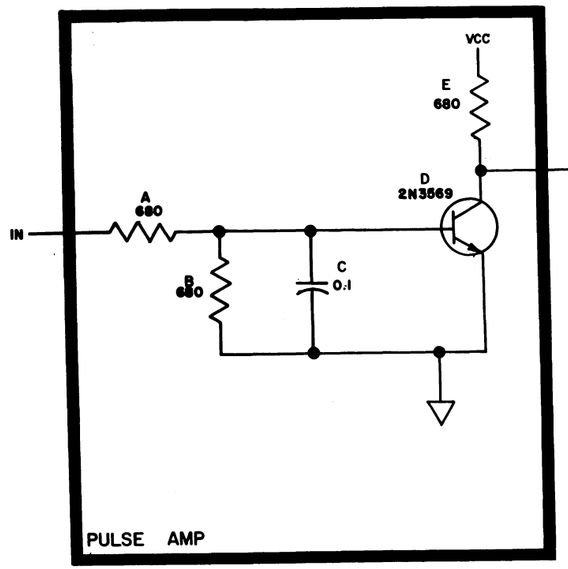
SCHEMATIC WIRING DIAGRAM FOR READER DRIVER.

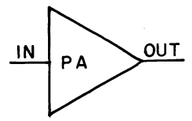
APPROVALS	
D AND R	E OF M
E-NUMBER	
PROD. NO. 8379 WD	
DATE 4-19-68	
P.D. FILE NO. G-A364AA	
DRAWN RJP	CHKD.
ENGD. CAY	APPD.

TELETYPE CORPORATION

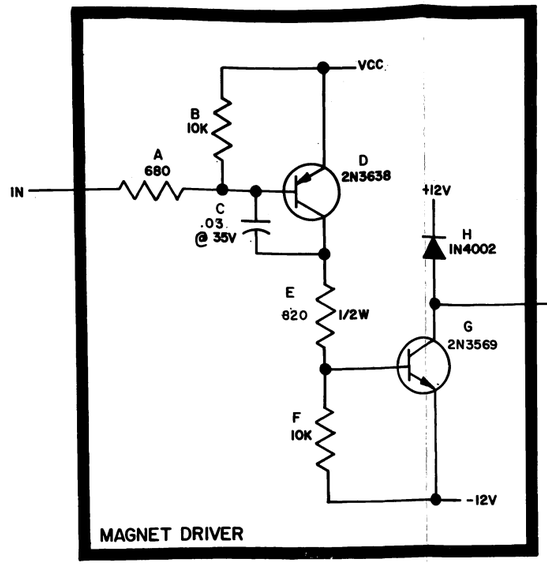
8379WD

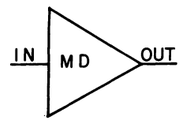
SEE SHEET 1 FOR NOTES



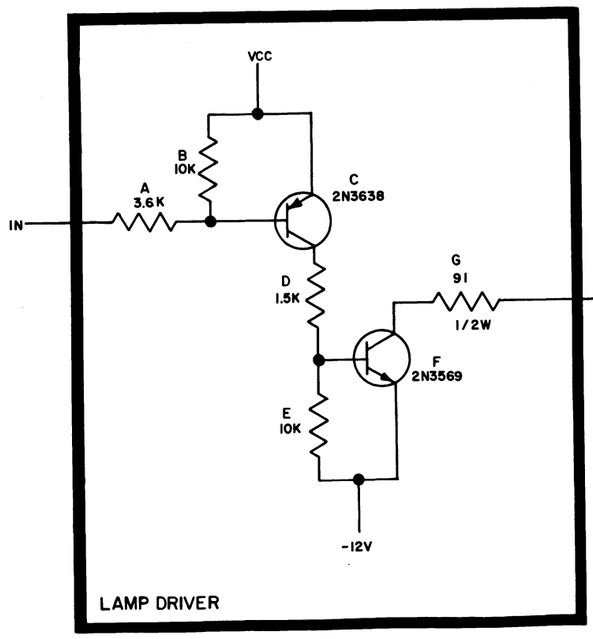


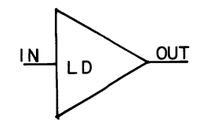
	PA2	PA1
A	R32	R27
B	R31	R30
C	C12	C11
D	Q5	Q4
E	R28	R29



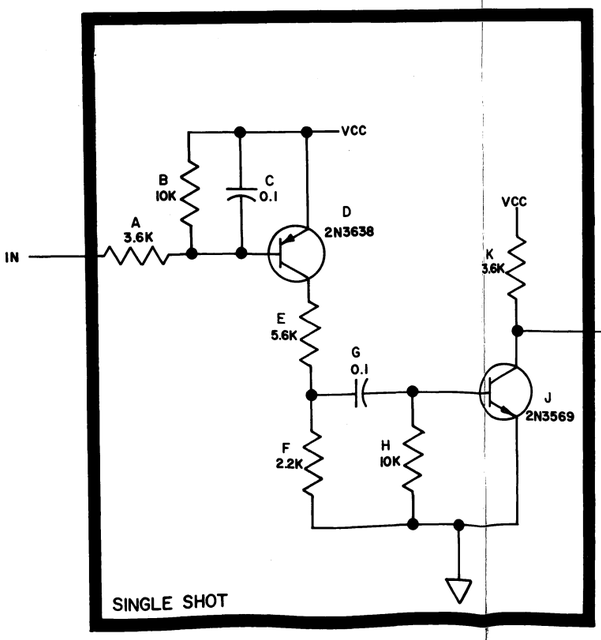


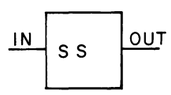
A	R26
B	R1
C	C16
D	Q6
E	R37
F	R2
G	Q1
H	CR1





A	R7
B	R4
C	Q7
D	R33
E	R3
F	Q2
G	R34





A	R21
B	R5
C	C10
D	Q8
E	R35
F	R36
G	C13
H	R6
J	Q3
K	R45

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8379WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 3

SCHEMATIC WIRING DIAGRAM FOR READER DRIVER

APPROVALS	
D AND R	E OF M

E-NUMBER	
PROD. NO.	8379WD
DATE	4-17-68
P.D. FILE NO.	8-A354AA
DRAWN RJP	CHKD.
ENGD. CAY	APPD.

TELETYPE CORPORATION

8379WD

TC 484 (5-68)

CIRCUIT DESCRIPTION OF THE READER DRIVER CARD ASSEMBLY NUMBER 322054

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NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

1

CIRCUIT DESCRIPTION OF THE READER DRIVER CARD ASSEMBLY NUMBER 322054

SECTION I

GENERAL TECHNICAL INFORMATION

1. Basic Function

1.1 The 322054 Reader Driver adapts the CX805 Reader to asynchronous operation. The card includes tape out, tight tape and bat handle logic.

2. Additional Features

2.1 Single step circuit

This circuit causes the reader to send exactly one character per operation of an externally mounted switch.

2.2 Alarm Circuit

A logically controlled paper alarm circuit is included, with lamp driver.

2.3 Automatic Reader Control

Interface leads are provided to allow automatic control of the reader by the 322079 alarms and automatic control card.

3. Lead Designations

3.1 Types of Outputs

3.1.1 DTL Output

ON =LOW = LOGIC ZERO = OPERATED
VO = 0 to + 0.5 VDC
output will sink a specified number of DTL input loads of 1.4 ma each. 233

OFF = HIGH = LOGIC ONE = NOT OPERATED
VO = VCC = 5.25V DC

3.1.2 Lamp Driver Output

ON= OPERATED = lamp lit
VO =-6V DC to -11V DC
Output sinks 60 ma max to -12V DC Supply.
OFF = NOT OPERATED = lamp not lit
VO = +12V DC Supply

3.3.3 Send Ready Pin A 29
This output is a loop back of send message, Pin A 27.

3.3.4 Present Character Pin B 32
This input is made low by set logic when the reader is to place a character on the parallel signal output. Two DTL loads.

3.3.5 Character Available Pin A 31
This output is low while a character from the reader is on the parallel signal output. Will drive seven DTL input loads.

3.3.6 One Step N.O. Contact, Pin B 31
A low on this input causes the reader to send one character. Two DTL loads.

3.3.7 RUN, Pin A 24
A low on this input causes the reader to send "Message Available" to the set logic if the reader is otherwise ready to send. Used only when the reader is to be controlled by the 322079 Alarms and automatic control card or similar logic external to the Reader Driver. One DTL load.

3.3.8 Manual Stop Pin B 28
This output is low when the reader bat handle is at "Stop" or "FREE." See Item 3.3.7 above. Will drive eight DTL loads.

3.3.9 Automatic Stop Pin B 19
A low on this lead stops the reader. When so stopped, the reader buffer storage register may retain a character. See Item 3.3.7 above. Two DTL loads.

234 3.3.10 Clock Pulse Number One, Pin A 23
A positive pulse on this input indicates that the position of the code reading contacts is valid. Input characteristics matched to the TTY Part No. 261M Magnetic Pickup.

3.3.11 Clock Pulse Number Two, Pin A 22
A positive pulse on this input permits the reader driver logic to change the state of the CX805 Operate Magnet. See Item 3.3.10 above.

3.3.12 Reader Bat Handle N.O. Pin B 27
This input is low when the reader bat handle (run-stop switch) is at RUN. Three DTL loads.

3.3.13 CX Coil Pin A 30
This lead sinks 300 ma max. to the -12 volt supply when the CX805 Operate Magnet is to be picked up. Voltage peak on magnet release does not exceed 40V DC, referred to the -12 volt supply.

3.3.14 Tight Tape Pin B 21

A low on this lead causes the reader to stop and lights the "RT Paper Alarm Lamp". The reader buffer storage level may retain a character. Three DTL loads. This lead is controlled by the CX805 tight tape N.O. contact in parallel with any other tape tension sensing N.O. contacts which may be provided.

3.3.15 Tape Out Pin B 23

A low on this lead causes the reader to stop, voids any character which may be held in the reader buffer storage level, and lights the RT Paper Alarm Lamp. The RT Paper Alarm Lamp will not be lit if the reader is stopped by the manual or automatic control circuits. Four DTL loads. This input is driven by the CX805 Tape Out N.O. contact.

3.3.16 Receiver Selectable, Pin B 30

This output is low when the receiving device associated with the reader has no paper alarm condition. Will drive eight DTL loads.

3.3.17 Paper Alarm (Disconnect) Pin B 26

This input to the paper alarm circuit is to be used if an on-line call is to be terminated when the paper supply of the associated receiver is out.

A low input lights the RT paper alarm light and causes Pin B 30, receiver selectable to be high. Three DTL loads.

3.3.18 Paper Alarm (Do Not Answer) B 24

This input lights the RT Paper Alarm light and, when Receive message Pin B 34 is high, causes Pin B30, receiver selectable, to be high. Three DTL loads.

3.3.19 RT Paper Alarm lamp, Pin B 33

This lead will be turned on when a paper alarm condition occurs in either the reader or the associated receiver. See Sections 3.3.14, 3.3.15, 3.3.17 and 3.3.18 above.

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3.3.20 RT Paper Alarm Pin B 29

This output is low when the RT Paper Alarm lamp is lit. Will drive seven DTL loads. See Item 3.3.19 above.

3.3.21 Code Contact Inputs

BIT	1	2	3	4	5	6	7	8
PIN NO.	B3	B5	B4	B6	B15	B18	B16	B17

A low (contact closed) on any of these inputs indicates that the bit is to be a mark.

These inputs are isolated from the reader parallel signal output by a gated buffer storage level. Input and output do not necessarily correspond at a given time.

Each input contact must sink two DTL loads.

3.3.22 Parallel Signal Output

BIT	1	2	3	4	5	6	7	8
Pin No.	B10	B9	B7	B8	B14	B11	B13	B12

A low on any of these outputs indicates that the bit is spacing. These outputs must be high when Character Available, Pin A 31, is high. Each output will drive Light DTL loads.

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NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

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SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly drawing 322054 (MC054) and schematic drawing 8379 WD.

1.2 Logic symbols and truth table 8399 WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 General

The 322054 Reader Driver Card adapts the CX805 Tape Reader to asynchronous operation. Interchange between the reader driver and M37 set logic is described by the following "standard peripheral interface" scheme.

2.2 Peripheral Interface Scheme

Refer to timing diagram number one.

2.2.1 Message Available, Pin B20

Indicates to set logic that the reader has no alarm conditions (tight tape, tape out) and that it is desired to send a message from the reader.

2.2.2 Send Message, Pin A27

Acknowledges Message Available and initiates such subsidiary operations as may be necessary to prepare the reader to transmit a character of the message. No such operations are necessary with the combination of CX805 Reader and 322054 Reader Driver, with or without the 322079 Alarms and Automatic Control Card.

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2.2.3 Send Ready, Pin A29

Acknowledges Send Message, and confirms the performance of subsidiary operations necessary to prepare the reader to send a character of the message. No such operations are necessary with the combination of CX805 and 322054 Reader Driver, with or without the 322079 Alarms and Automatic Control Card; Send Ready is a direct loop-back of Send Message.

2.2.4 Present Character, Pin B32

Present Character acknowledges Send Ready and indicates to the set logic that the distributor (parallel to serial converter) to which the message is to be sent is prepared to accept a character, and that the reader should place a character on its parallel signal output. Present character, once advanced, cannot be withdrawn prior to completion of the distributor character sample without loss of a character.

2.2.5 Character Available, Pin A31

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1

2.2.5 Cont.

Character Available acknowledges present character and indicates to the set logic that the distributor should sample the reader parallel signal output. Character Available remains on until, at the end of the distributor character sample, Present Character is turned off.

3.1 Operation

3.1.1 Message Available, Pin B20

Message Available, Pin B20, is controlled by MLC2 outputs 12 and 8. These two gates are enabled while there is no tight tape (Pin B21) or tape out (Pin B23) signal from the reader. In this condition MLC3 inputs 4 and 5 are high, placing a low on MLC3 inputs 9 and 10, which drives MLC3 output 8 and MLC2 inputs 13 and 11 high.

A low on Run, Pin A24, will start the sending cycle. Run may be controlled by logic external to the reader driver, or, if strap A is installed, by the reader bat handle N.O. Contact. In either case, a low on MLC1 input 10 drives MLC1 output 8 and MLC2 inputs 1 and 2 high. All inputs to MLC2-12 are now high, forcing MLC2-12 low, indicating Message available. MLC1 output 8 high also enables MLC3 output 11. This is done to prevent continuous display of an alarm light on Tape Out, when it is not intended that the reader should run.

MLC2 output 8 holds Message Available, Pin B20, on, in case Run, Pin A24, goes high while a character is stored in the reader buffer storage level. The "Character Stored" Latch (CSL) is set when the buffer storage contains a character. This places a high on MLC2 input 10. If MLC2 output 8 is enabled, (with a high on MLC2 input 11) and Automatic Stop, Pin B19, is not low, Message Available will continue low until the buffer storage is clear (CSL Reset). Automatic Stop, Pin B19, low, disables this feature when the
238 reader is stopped by a detected control character, such as DC3 or EOT, or when the reader is stopped by a line disconnect (NORMALIZATION). The feature is also disabled on Tight Tape or Tape Out, through MLC3 outputs 6 and 8.

3.1.2 Operate Magnet Control

With Run, Pin A24, low and a low output on Message Available, Pin B20, the reader has indicated readiness to send a message. In preparation for sending the message, a character will be read from the tape into the buffer storage level.

To read a character, the CX805 Operate Magnet must be picked up. This magnet is operated by magnet driver MD and controlled by the magnet driver latch (MDL). MDL is set or reset by the matrix formed from MLB1-8 and MLB2-8. NAND Gate MLB2-8 collects the conditions that determine the state of MDL. These conditions are:

1. A "RUN" command:

MLC1 output 8 high (MLB2 input 10 high)

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1

3.1.2 Cont.

2. Not Tape Out:

Tape Out Latch (TOL) Reset (MLB2 input 12 high)

3. No character stored:

Character Stored Latch (CSL) Reset (MLB2 input 9 high)

4. Clock pulse Two present:

Pulse amplifier Two ON, MLB1 inputs 12 and 13 low, MLB1 output 11 high, MLB2 input 13 high, LLB1 input 10 high.

If all of these conditions are as described above, MLB2 output 8 will be low, disabling MLB1-8 with a low on MLB1 input 9, and setting MDL with a low on MLB1 input 4. MDL set turns on MD, picking up the CX OPERATE MAGNET.

If any of these conditions are not met when clock pulse Two occurs, MLB2 output 8 will be high, enabling MLB1-8. MLB1 output 8 will be low during clock pulse Two, resetting MDL, turning off MD and releasing the CX operate magnet.

Clock Pulse Two, CP2, which permits pickup or drop out of the CX operate magnet, is generated by a magnetic pickup on the main shaft of the CX805. This pickup is placed as near the end of the CX read-feed cycle as possible, so that the operate magnet may be fully picked up or released between CP2 and the beginning of the next read-feed cycle. The read-feed cycle time at 150 Baud, 10 bit, is 66.67 ms. Main shaft speed is 900 RPM. The CP2 pick up coil produces a generally sinusoidal wave form when a permanent magnet embedded in the CX805 flywheel passes it. The pickup coil output wave has equal positive and negative half-cycles of about 3 volts amplitude and 1 ms duration (at 900 shaft RPM). The negative half-cycle of the output wave has no effect on the pulse amplifier, and may occur before or after the positive half-cycle. 239

The positive half-cycle turns on the transistor of the pulse amplifier (PA2). PA2, ON, holds MLB1 inputs 12 and 13 low which forces MLB1 output 11 high. This high output is connected to MLB2 input 13 and MLB1 input 10 to enable the magnet control matrix as described above. Clock pulse one, referred to below, is produced in a similar way using PA1, and MLD1-11. The two clock pulses are separated by 1/4 of a main shaft cycle at 900 RPM, or 16.67 ms.

3.1.3 Reading a Character into Storage

MDL set (operate magnet picked up) places a high on inputs 2 and 12 of MLC1, enabling MLC1-11 and MLC1-3. When clock pulse one (CP1) occurs while these gates are enabled, outputs 11 and 3 of MLC1 will go low for the duration of CP1.

3.1.3 Cont.

CP1 occurs during the time that code reading contact closures on the CX805 are valid.

With MDL Set and CP1 on, MLC1 outputs 3 and 11 are low. MLC1-3, low, sets CSL. MLC1-11, low, resets the bit storage levels in the buffer storage register. Bit storage latches with marking (closed) contacts will revert to set as soon as CP1 is over. All others will continue reset (spacing). At the end of CP1, the state of the buffer storage register represents the character being read.

3.1.4 Character Stored Latch (CSL)

CP1, occurring while the operate magnet is picked up (MDL set), places a valid character in the buffer storage register as described above. This event is indicated by a low on output 3 of MLC1, which sets the character stored latch (CSL).

CSL, set, places a high on input 12 of MLA1. When Present Character, Pin B32, is low, MLA1 output 6 and MLA1 input 13 will be high. MLA1 inputs 12 and 13 high causes a low on MLA1 output 11 and Pin A31, Character Available.

Present Character, Pin B32, low, indicates that the send control is ready to accept a character from the reader; Character Available, Pin A31, low, indicates to the s end control that a distributor should sample the parallel data buss for a character from the reader and, through MLA1 output 3, gates the stored character onto the parallel data buss.

When the distributor has read the stored character, Present Character, Pin B32, will go high, causing MLA1 output 6 to go low. MLA1 output 6 low ends Character Available by forcing MLA1 output 11 high, and, through the single shot circuit (SS), resets CSL with a 1/2 ms low pulse. CSL, reset, enables MLB2-8 through the occurrence of CP2, allowing MDL to remain set. MDL, set, permits another character to be read just as described above.

If CSL is not reset before the occurrence of CP2, MLB2-8 will be disabled, through input 12, MLB1-8 will be enabled, and MDL will be reset by CP2, dropping out the operate magnet. With the operate magnet dropped out no further characters will be read until CSL is reset. MLC2-8 will keep Message Available, Pin B20, turned on (low) until CSL, reset, puts a low input on MLC2 input 10. This arrangement prevents leaving a character in storage when the reader is stopped by removal of RUN, Pin A24. Automatic Stop, Pin B19 low, disables MLC2-8. When this lead is operated, the reader may be stopped with a valid character in the buffer storage register.

Another condition under which the reader may be stopped with a valid character in storage occurs if the "control character delay" option is selected on the mode control card (8387 WD - CD, KSR, 8386 WD - CD, ASR). When this option is selected, Present Character, Pin B32, will remain high for 22 bits following the Present Character signal during which a control character is read. CP1, like CP2, occurs in 1 character cycles (66.67 ms between repititions at 150 baud 10 bit, ie. 900 RPM). Thus, when a control character is read from the storage register, the following character in the tape will be read into storage on the next occurrence of CP1, but Present Character will not go low before CP2 occurs in the following cycle and the operate magnet will be released. See timing diagram.

3.1.5 "OFF SPEED" Operation

Reader operation is slightly changed when there is a difference between the reader main shaft speed and the distributor clock rate. Reader main shaft speed is normally 900 RPM (66.67 ms per revolution). The main shaft speed will vary with line frequency.

The distributor clock rate at 150 baud is 15 characters per second (66.67 ms per character). The clock rate is determined by a crystal oscillator on the mode control card.

The reader driver card is designed to tolerate any degree of mismatch between these rates, at character rates up to 300 baud.

The following table is drawn from the preceding section.

Input Conditions	Response
1. CP_2 + RUN + NO TAPE ALARM + NO CHARACTER STORED	PICK UP MAGNET
2. CP_1 + MAGNET PICKED UP	STORE CHARACTER
3. CHARACTER STORED + PRESENT CHARACTER	SEND CHARACTER

Characters are always read into the buffer storage on the CP1 signal. If the stored character is not read out of storage by the time CP2 occurs, 16.67 ms later, the CX operate magnet will drop out. This prevents reading a new character into storage until the stored character is read out.

The distributor clock rate determines the time between occurrences of Present Character. If the clock rate is fast, the distributor will accept a character as soon as it is available.

The "pick up point" is the one-bit interval during which the distributor samples the character presented on the reader parallel data buss. The end of this interval is marked by the low-to-high transition of Present Character (PC) which resets CSL through single shot circuit SS, and ends Character Available through MLA1 input 13.

241

A character stored in the reader buffer storage register on CP1 may be read out at any time thereafter. If the low to high transition of PC occurs before the end of the CP2 immediately following, the operate magnet will stay picked up, allowing a new character to be read into storage.

PC will be returned low by the send control circuit as soon as the distributor completes serial transmission of the character just obtained, in parallel, from the reader. If the distributor clock rate is fast, the time between successive high to low transitions of PC will be short compared to the reader cycle time. The pick up point will now be earlier in each succeeding reader cycle, until characters are being read out as soon as they are available. The pick up point will now be one bit time after CP1, where it will stay. In this condition, the time between the beginning of one serially transmitted character and the next will be determined by the reader main shaft speed while the bit rate of the character is determined by the distributor clock.

3.1.5 Cont.

If the clock rate and main shaft speed are identical, the pick up point will remain stationary somewhere between CP1 and CP2.

If the clock rate is slower than the reader main shaft speed, the pick up point will drift toward CP2. This drift will continue until the low-to-high PC transition, marking the end of the pick up interval, occurs after CP2. The operate magnet will now drop out, to be picked up again when both PC and CP2 are on. The next character in the tape will be read into storage on the CP1 immediately following. With PC already low, the new characters will be read out as soon as it is available. The start-drift-restart cycle will continue as long as the speed difference remains. If the time difference per reader cycle is 0.1 ms, the restart will occur after 100 characters.

900 RPM main shaft speed = 66.67 ms/cycle
CP1 to CP2 time interval = 16.67 ms
16.67 ms less 1 bit time (for pickup) = 10 ms

$$\frac{0.1 \text{ ms drift/cycle}}{10 \text{ ms}} = 1/100$$

This mode of operation permits the CX reader, nominally 150 WPM speed, to send at 100 WPM, and permits a simple "one step" circuit to be added.

3.1.6 One Step Circuit

Operation of the "one step" switch N.O., Pin B31, sets the one step latch (OSL) through MLA3-3, Integrater R38-C1, MLA3-6 and Coupler C3-R9.

OSL, set, institutes a run command, (low on Input 9 of MLC1) which causes the reader to read and store a character as described in 3.1.4 above. 242 Storing the character will set CSL, which resets OSL through MLD1-6 and Coupler C9-R16. This operation causes one character to be stored and read out for each operation of the switch. This convenience feature permits the message tape to be advanced one character at a time, to facilitate tape editing or tape positioning.

3.1.7 Paper Alarm Circuit

Lamp driver LD operates the RT Paper Alarm Lamp, Pin B33, under the control of NAND Gate MLB2-6 and Inverter MLA3-8. Any low on the input of MLB2-6 will turn on the alarm lamp.

MLB2 input 1 is connected to Tape Out, Pin B23, through Inverter MLC3-3 and Gate MLC3-11. A low on MLC3 input 13 will inhibit the alarm indication when the reader is not under a "RUN" command. Tape Out, Pin B23, is controlled by the CX805 Tape Sensing Pin Contact.

MLB2 input 2 is connected to the CX805 Tape Out Contact Pin B21. If the tape handling equipment used provides other contacts to sense Tight Tape, such contacts should be connected between Pin B21 and Circuit Ground, Pin 2, in parallel with the CX805 Contact.

3.1.7 Cont.

MLB2 input 4 is connected to the Paper Alarm, do not answer input Pin B24. This input is normally connected to the tape supply sensing arm of an associated tape punch.

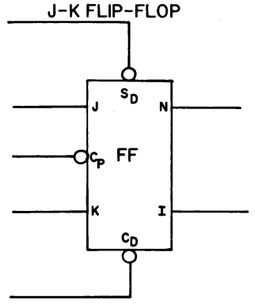
With no alarm present, MLB3-3 sets the Receiver Selectable Latch, RSL. This set signal will be removed when the alarm condition occurs. At the end of an "On Line" message, Receive Message, Pin B34, will go high. Through Integrator R39-C2, MLB3-6 will then reset RSL if an alarm condition on Pin B24 has removed the set signal.

RSL Reset forces MLA3 output 11 high, which runs off the Receiver Selectable Lead, Pin B30.

Paper alarm, disconnect, connected to input 5 of MLB2, removes Receiver Selectable directly through MLA3 input 13. This signal is used where it is desired to terminate an On Line call on the basis of a low receiver paper supply.

NO.	NOTES
1.	GRAPHICAL SYMBOLS AND THE ASSOCIATED TRUTH TABLES ILLUSTRATED ON THIS PAGE ARE TYPICAL SYMBOLS USED IN TELETYPE CORPORATION APPARATUS.
2.	LOGIC NEGATION - A SMALL CIRCLE (O) DRAWN AT THE POINT WHERE A SIGNAL LINE JOINS A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
3.	STATE DESIGNATIONS: I - STATE = +6V O - STATE = 0V
4.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER THE GATE IS USED AS AN INVERTER.
5.	ABBREVIATIONS USED: O - LOW STATE (MORE NEGATIVE) I - HIGH STATE (MORE POSITIVE) X - STATE OF INPUT DOES NOT AFFECT STATE OF CIRCUIT NC - NO CHANGE U - INDETERMINATE STATE N_M - STATE OF N AT TIME M. $\overline{N}_M$ - INVERSION OF STATE OF N AT TIME M.

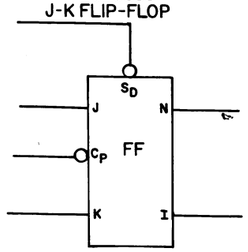
326852 J-K FLIP-FLOP



ASYNCHRONOUS TRUTH TABLE 326852

S_D	C_D	N	I
I	I	NC	NC
O	I	I	O
I	O	O	I
O	O	I	I

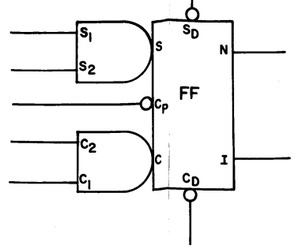
326853 J-K FLIP-FLOP



ASYNCHRONOUS TRUTH TABLE 326853

S_D	N	I
I	NC	NC
O	I	O

326845 CLOCKED FLIP-FLOP



ASYNCHRONOUS TRUTH TABLE 326845

C_D	S_D	N	I
I	I	NC	NC
I	O	I	O
O	I	O	I
O	O	I	I

SYNCHRONOUS TRUTH TABLE 326845

S_1	S_2	C_1	C_2	N
O	X	O	X	NC
O	X	X	O	NC
X	O	O	X	NC
X	O	X	O	NC
O	X	I	I	O
X	O	I	I	O
I	I	O	X	I
I	I	X	O	I
I	I	I	I	U

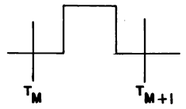
J-K TRUTH TABLES (CONNECT S_2 TO I, C_2 TO N)

T_M		T_{M+1}
S_1	C_1	N
O	O	N_M
I	O	I
O	I	O
I	I	$\overline{N}_M$

J-K TRUTH TABLE BOTH TYPES

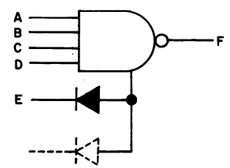
T_M		T_{M+1}
J	K	N
O	O	N_M
I	O	I
O	I	O
I	I	$\overline{N}_M$

CLOCKED PULSE WAVE FORM



ASYNCHRONOUS INPUTS, DIRECT SET (S_D) AND DIRECT CLEAR (C_D), OVERRIDE THE SYNCHRONOUS INPUTS. THEY ARE INDEPENDENT OF ALL OTHER INPUTS.

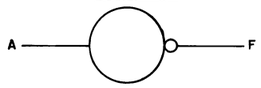
NAND GATE



A	B	C	D	E	F
I	I	I	I	I	O
I	O	O	O	O	I
O	O	O	O	O	I
O	I	I	I	I	I

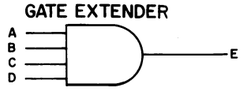
A,B,C,D OR E LOW(O) CAUSES F TO GO HIGH (I)

INVERTER



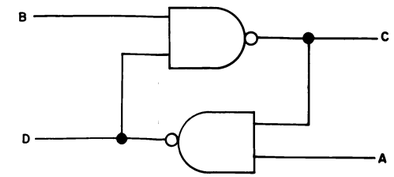
A	F
O	I
I	O

GATE EXTENDER



$E = A \cdot B \cdot C \cdot D$

SET-RESET FLIP-FLOP UTILIZING NAND GATES



A	B	C	D
O	O	I	I
O	I	O	I
I	O	I	O
I	I	NC	NC

8399 WD

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	5-3-68	19208-R

LOGIC SYMBOLS AND TRUTH TABLES

APPROVALS	
D AND R	E OF M
E-NUMBER	
PROD. NO. 8399WD	
DATE 2-12-68	
P.D. FILE NO. G-A354AA	
DRAWN RJP	CHKD.
ENGD. MJR	APPD.

TELETYPE CORPORATION

8399WD

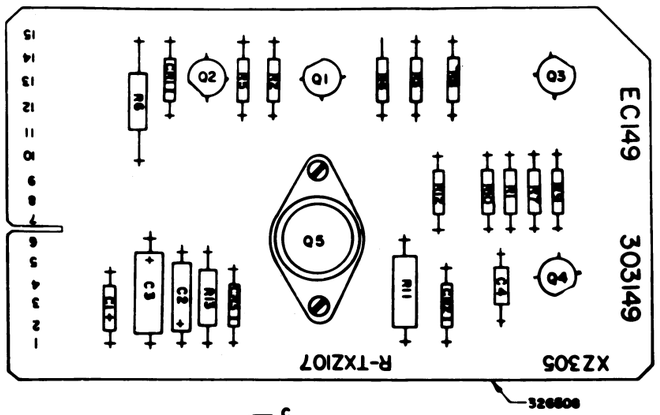
TC 484 (3-68)

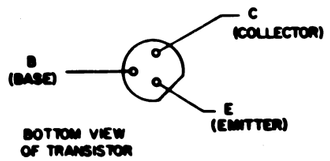
NO. NOTES

1 SEE SPECIFICATION MR2.001 FOR CIRCUIT BOARD REQUIREMENTS.

2 REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY

3 ASSOCIATED SCHEMATICS 8370WD





BOTTOM VIEW OF TRANSISTOR

CIRCUIT CARD EC

REF DESIG.	TELETYPE PART NO	TOTAL QTY	NAME AND DESCRIPTION	LOCATING FUNCTION
R1-2	315958	2	RES. FIXED 3.6K	1/4W
R3	320275	1	" " 10K	1/4W
R4	315954	1	" " 1.5K	1/4W
R5	320275	1	" " 10K	1/4W
R6	182514	1	" " 91	1/2W
R7	315958	1	" " 3.6K	1/4W
R8	320275	1	" " 10K	1/4W
R9	320276	1	" " 470	1/4W
R10	321507	1	" " 1.8K	1/4W
R11	139336	1	" " 150	2W
R12	321213	1	" " 1K	1/4W
R13	118724	1	" " 220	1/2W
C1	327831	1	CAPACITOR DISC 6.8 MFD 6V DC	
C2	326591	1	" TANT. 3.9 MFD 35V DC	
C3	326592	1	" TANT. 33 MFD 35V DC	
C4	326752	1	" .03 MFD 50V DC	
Q2	324656	1	TRANSISTOR 2N3569	
Q1-3-4	315931	1	" 2N3638	
Q5	326594	1	" 2N3767	
CR1	321939	1	DIODE 1N4002	
CR2	197464	1	" 1N914	
CR3	321949	1	" 1N4002	
	326508	1	BOARD, ETCHED CIRC.	
	3598	2	NUT	
	154335	2	SCREW	
	107116	2	LOCKWASHER	

303149

REVISIONS

ISSUE	DATE	AUTH. NO.
6	11-15-68	96464-1

WDP

SHEET 1

RECEIVING DEVICE

APPROVALS

R AND D	E OF M

E-NUMBER

PROD NO 303149

DATE 8-11-67

R&D FILE G-A354AA

DRAWN R.J.P. | CHKD

ENGD. M.J.R. | APPD.

TELETYPE CORPORATION

303149

NO. NOTES

1 INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD:

ML D 2

ROW
COLUMN
INTEGRATED CIRCUIT

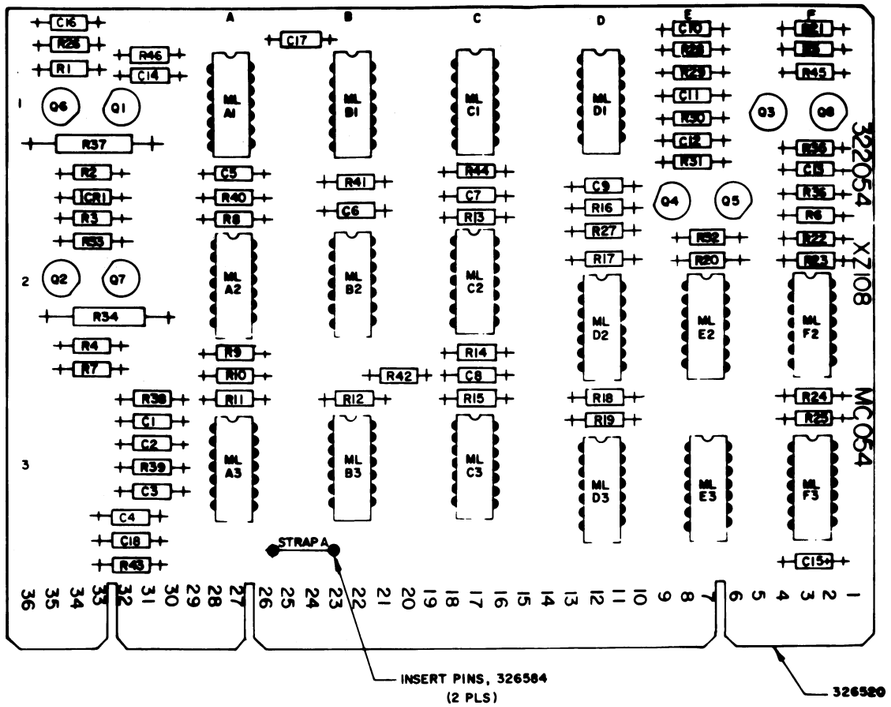
2 CHARACTER HEIGHT .120-12 POINTS NEWS GOTHIC.

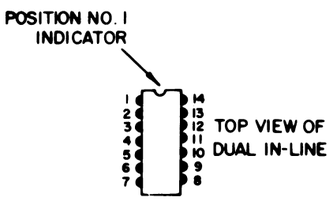
3 REFERENCE SPECIFICATION: FOR TELETYPE CORPORATION EMPLOYEES ONLY.

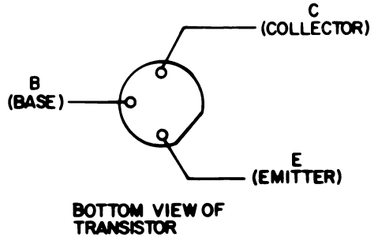
4 ASSOCIATED SCHEMATICS ARE READER DRIVER - 8379WD.

5 REFER TO SPECIFICATION MR2.001 FOR CIRCUIT BOARD REQUIREMENTS. FOR TELETYPE CORPORATION EMPLOYEES ONLY.

6 ALL CHARACTERS ARE TO BE SILK SCREENED IN WHITE, BLACK OR RED ENAMEL.







R 37 IS 470 OHMS ON SOME CARDS

CIRCUIT CARD EC

	REF DESIG.	TELETYPE PART NO	TOTAL QTY	NAME AND DESCRIPTION	LOCATING FUNCTION
	MLA1	326846	1	INTEGR. CIRC. 846	
	MLB1	326846	1	" " "	
	MLC1	326846	1	" " "	
	MLD1	326846	1	" " "	
	MLA2	326846	1	" " "	
	MLB2	326830	1	" " 830	
	MLC2	326862	1	" " 862	
	MLD2	326846	1	" " 846	
	MLE2	"	1	" " "	
	MLF2	"	1	" " "	
	MLA3	"	1	" " "	
	MLB3	"	1	" " "	
	MLC3	"	1	" " "	
	MLD3	"	1	" " "	
	MLE3	"	1	" " "	
	MLF3	"	1	" " "	
	R1-R6	320275	6	RESISTOR, FIXED 10K	(1/4W)
	R7-R25	315958	19	" " 3.6K	(1/4W)
R26-R32		315971	7	" " 680	(1/4W)
	R33	315954	1	" " 1.5K	(1/4W)
	R34	182514	1	" " 91	(1/2W)
	R35	315960	1	" " 5.6K	(1/4W)
	R36	315972	1	" " 22K	(1/4W)
	R37	137439	1	" " 820	(1/2W)
R38-R43		315948	6	" " 100	(1/4W)
	R44	315947	1	" " 51	(1/4W)
	R45	315958	1	" " 3.6K	(1/4W)
C1-C14		312385	14	CAPACITOR 0.1 MFD	10VDC
	C15	327831	1	" 6.8 MFD	6VDC
	Q1-Q5	324656	5	TRANSISTOR 2N3569	
	Q6-Q8	315931	3	2N3638	
	CR1	321949	1	DIODE 1N4002	
		326520	1	CIRCUIT BOARD	
		39603RM	1	STRAP 1.2" 24GA.	
		326584	2	PIN, FORMED	
	R46	326599	1	RESISTOR, FIXED 36	(1/4W)
C16-C17		326752	2	CAPACITOR .03 MFD	
	C18	326752	1	CAPACITOR .03 MFD	

322054

REVISIONS

ISSUE	DATE	AUTH. NO.
5	1-15-68	96464

SHEET 1 OF 2

READER

DRIVER

APPROVALS

R AND D	E OF M

E-NUMBER

PROD NO 322054

DATE 3-22-68

RBD FILE G-A354AA

DRAWN R.J.P.	CHKD
ENGD. C.A.Y.	APPD

TELETYPE CORPORATION

322054

TC 474 (1-66)

BASIC WIRING DIAGRAM PACKAGE FOR THE MODEL 37 REPERFORATOR-TRANSMITTER (RT) MODULE

WDP 0129

DRAWING NO.	SHEET NO.	DESCRIPTION	ISSUE NUMBER 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
8354WD	ICR	Schematic - Model 37 RT (EIA)	1	1	1	2	2	3																								
8354WD	1	Schematic - Model 37 RT (EIA)	1	1	1	1	1	1																								
8354WD	2	Schematic - Model 37 RT (EIA)	1	1	1	2	2	3																								
8355WD	ICR	Actual - YESU803	1	1	1	2	2	3																								
8355WD	1C	Actual - YESU803	1	1	1	1	1	2																								
8355WD	2C	Actual - YESU803	1	1	1	1	1	1																								
8355WD	3C	Actual - YESU803	1	1	1	1	1	1																								
8355WD	4C	Actual - YESU803	1	1	1	2	2	2																								
8355WD	5C	Actual - YESU803	1	1	1	1	1	1																								
8355WD	6C	Actual - YESU803	1	1	1	1	1	1																								
8355WD	7C	Actual - YESU803	1	1	1	1	1	1																								
8355WD	1X	Actual - YESU803	1	1	1	1	1	3																								
8355WD	2X	Actual - YESU803	1	1	1	1	1	3																								
8355WD	1	Actual - YESU803	1	1	1	1	1	3																								
8355WD	2	Actual - YESU803	1	1	1	1	1	3																								
8355WD	3	Actual - YESU803	1	1	1	1	1	3																								
8365WD	ICR	Analysis Chart-Control Panels	1	1	1	1	1	1																								
8365WD	1	Analysis Chart - Control Panels	1	1	2	2	3	3																								
8365WD	6	Analysis Chart - Control Panels	1	1	2	2	2	2																								

TELETYPE CORPORATION

19683 R NOTE : THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF WDP.

SHEET 1 OF 1

ISSUE CONTROL RECORD

8354WD

SHEET NO.	ISSUE																	
	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
1																		
2	X																	

WDP

REVISIONS

ISSUE	DATE	AUTH. NO.
1	[redacted]	19710-R
2	2-5-69	96757

ISSUE CONTROL SHEET 1 OF 1

SCHEMATIC WIRING DIAGRAM FOR THE R-T ELECTRICAL SERVICE UNIT (YESU803)

APPROVALS

D AND R	E OF M
LDm	~

E-NUMBER

PROD. NO. 8354WD

DATE: 4-30-68

P.D. FILE NO. G-A354AA

DRAWN. REG | CHKD. [illegible]

ENGD. MJR | APPD. [illegible]

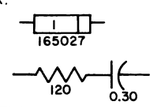
TELETYPE CORPORATION

8354WD

2

TC482 (11-65)

245

NO.	NOTES.
1.	ALL VOLTAGE DC. UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
4.	TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE ONLY, AND ARE NOT MARKED ON COMPONENT.
5.	NETWORK: 
6.	INDICATES FEMALE TERMINAL. INDICATES MALE TERMINAL.
7.	TWISTED PAIR: P
8.	INDICATES TERMINALS ON TB112 WIRING FIELD, UNLESS OTHERWISE SPECIFIED.
9.	INDICATES CIRCUIT GROUND. INDICATES CHASSIS GROUND.
10.	ABBREVIATIONS USED: T.O.-TAPE OUT. AVAIL.-AVAILABLE. T.T.-TIGHT TAPE. MTR.-MOTOR. B.H.-BAT HANDLE. SEL.-SELECTOR. RCV.-RECEIVE. NORM.-NORMALIZE. MESS.-MESSAGE. E.O.T.-END OF TRANSMISSION. GRD.-GROUND. RDR.-READER. AUX.-AUXILIARY. AUTO.-AUTOMATIC. N.C.-NORMALLY CLOSED. CHAR.-CHARACTER. N.O.-NORMALLY OPEN.
11.	S-NUMBER: [illegible]
12.	CIRCUIT CARD PIN NUMBER IS THE SAME AS CONNECTOR SHOWN. RDR DRIVER - CIRCUIT CARD NAME. Z108- [illegible] CARD LOCATION IN ELECTRICAL SERVICE UNIT. SEE CIRCUIT CARD WDP FOR ASSOCIATED SCHEMATIC.
13.	COMMON VOLTAGE INPUTS TO ALL CIRCUIT CARDS. VCC-PIN 1 GRD-PIN 2 +12V.-PIN35 -12V-PIN36
14.	FOR CONTROL STRIP WIRING ON R-T CABINET REFER TO 8365WD, SHEET 1 AND 6.

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8354WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-6-68	19710-R

WDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 1

SCHEMATIC
WIRING DIAGRAM
FOR
MODEL 37-RT.
(YESU 803)

APPROVALS

D AND R	E OF M
LDM	

E-NUMBER

PROD. NO. 8354 WD

DATE 8-14-68

P.D. FILE NO. G-A354AA.

DRAWN W.P.B. CHKD.

ENGD. C.A.Y. APPD.

TELETYPE CORPORATION

8354WD

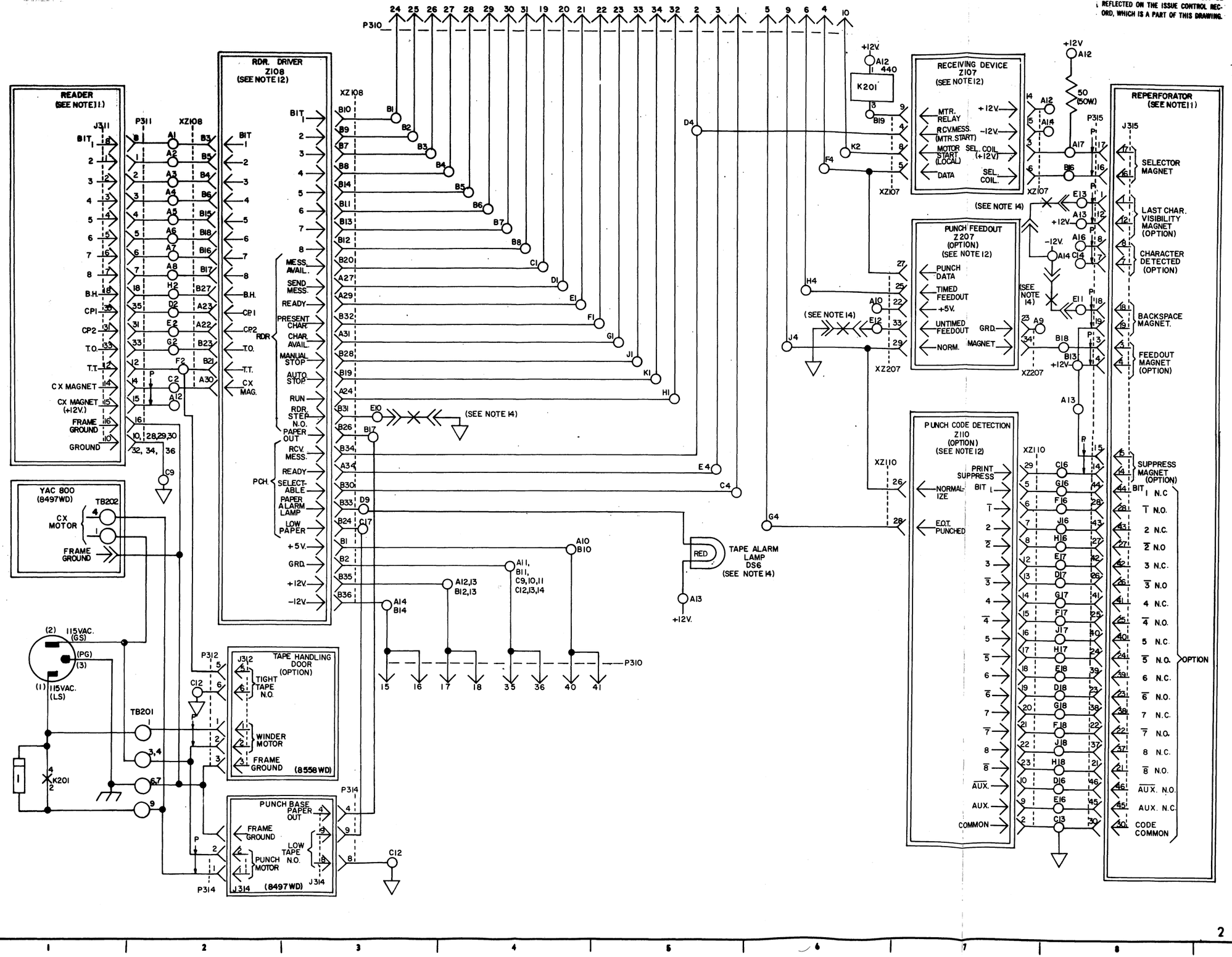
SEE SHEET 1 FOR NOTES.

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8354WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-6-68	19710-R
2	2-4-69	96751



SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 2

SCHEMATIC WIRING DIAGRAM FOR MODEL 37-RT (YESU 803)

APPROVALS	
D AND R	E OF M
LWM	

E-NUMBER	
PROD. NO. 8354WD.	
DATE 5-29-68	
P.D. FILE NO. G-A354AA	
DRAWN W.P.B.	CHKD.
ENGD. C.A.Y.	APPD.

TELETYPE CORPORATION

8354WD

ISSUE CONTROL RECORD

8355WD

SHEET NO.	ISSUE 2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
1C	X																	
2C																		
3C																		
4C	X																	
5C																		
6C																		
7C																		
1X	X	X																
2X	X	X																
1	X	X																
2	X	X																
3	X	X																

WDP

REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-6-68	19710-R
2	2-4-69	19678
3	5-1-69	99130

ISSUE CONTROL SHEET 1 OF 1

ACTUAL WIRING DIAGRAM FOR THE R-T ELECTRICAL SERVICE UNIT YESU803

APPROVALS

D AND R	E OF M
LDM	

E-NUMBER

PROD. NO. 8355WD.

DATE: 4-30-68

P.D. FILE NO. G-A354AA

DRAWN. REG. CHKD. [illegible]

ENGD. MJR APPD. [illegible]

TELETYPE CORPORATION

8355WD

TC482 (11-65)

ACTUAL WIRING DIAGRAM FOR THE R-T ELECTRICAL SERVICE UNIT YESU803 USED ON MODEL 37

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

1. PAGE NUMBERING

This WD consists of three sections: the issue control (and notes), the network listing index pages, and the network listing pages.

Page 3 of 4 means the third page of 4 issue control sheets.

Page 2X of 11X/30 is the 2nd page of 11 index pages in a WD having 30 total pages.

Page 10 of 15/30 is the 10th of 15 network pages in a WD having 30 total pages.

2. ISSUE CONTROL SHEETS

The issue control sheets contain the release information and notes pertaining to the WD.

3. NETWORK LISTING INDEX

The index pages list components and pin designations in alphanumeric, alphabetical and numerical order and indicate the number of the network (net) in which each appears.

4. NETWORK LISTING

All pins with the same network listing number are electrically common. Any pin is connected to the pin listed immediately below (see sample net 0001). Where a pin is connected to two succeeding pins, one of the following pin designations will be indented, thereby indicating
249 that the original is connected to the pin below it and to the indented pin (see sample net 0002). Where a pin is connected to more than two succeeding pins, additional indented columns will be used. The original pin is connected to all the pins at the end of the columns of dots and to the indented pin immediately below, (see sample net 0003). There is no direct connection between a pin and one listed below and in a column to its left.

5. Issue 2 added the following wires:

FROM	TO	FROM	TO
XZ108-A6	TB112-F14	XZ108-A33	TB112-D14
XZ108-A7	TB112-E14	XZ108-B22	TB112-F3
XZ108-A8	XZ107-8	XZ108-B25	TB112-G3

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

NETWORK LISTING (TABULAR WIRING DIAGRAM) ISSUE CONTROL

TITLE
ACTUAL WIRING DIAGRAM FOR THE R-T ELECTRICAL SERVICE UNIT YESU803

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
8355 WD	X 1	MODEL 37	6/30/68	PAGE 2C OF 3C

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SH COMPRISING 1...3 W.D.

SAMPLE NETWORK (ARROWS SHOW CONNECTIONS)

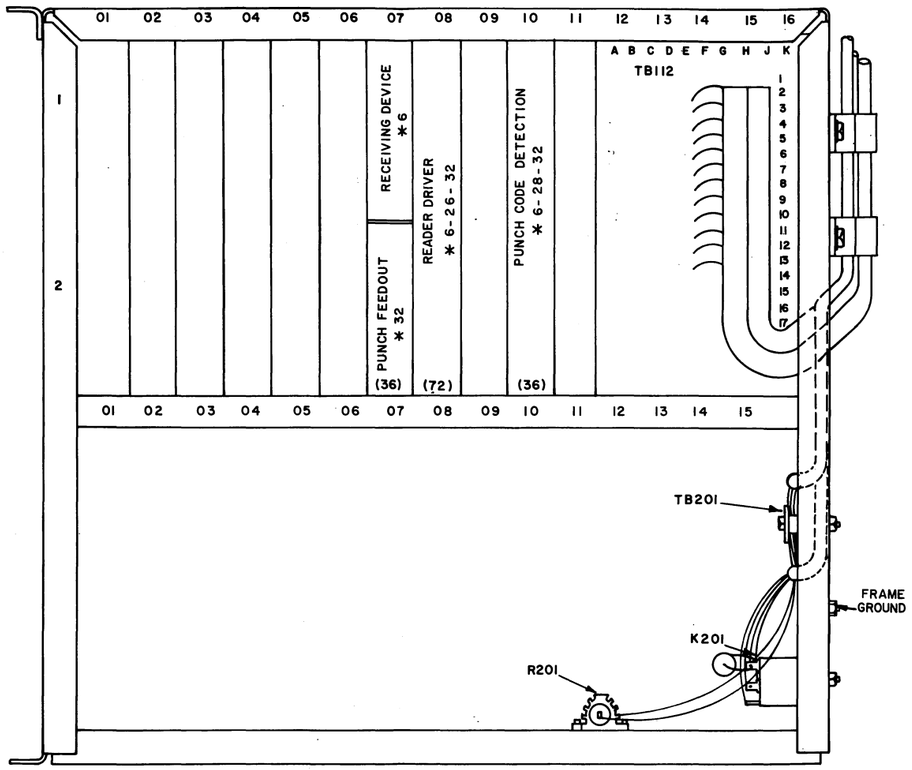
Net	Component	Pin
0001	TB5001	A 1
0001	TB5009	H 9
0001	TB5011	A 1
0002	TB5001	B5
0002	BB5001	C 1
0002	• TB5002	B 6
0002	• PS5002	J 3
0002	• • TB5001	D 2
0002	• • TB5002	C 6
0002	• • TB5002	A10
0002	• TB5001	K 5
0002	TB5011	B 5
0003	TB5011	B 6
0003	TB5012	B 5
0003	• • • • TB5014	A 8
0003	• • • • TB5014	A 2
0003	• • • TB5014	B 5
0003	• • TB5014	B 6
0003	• • TB5014	D 3
0003	• TB5014	E 9
0003	TB5009	E10

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

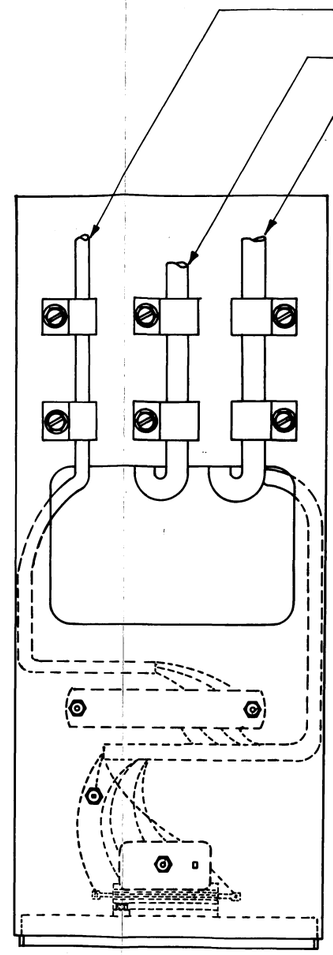
WDP

NO.	NOTES
1.	TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE ONLY AND ARE NOT MARKED ON THE COMPONENTS.
2.	NAMES SHOWN IN CIRCUIT CARD CONNECTOR LOCATIONS INDICATES THE FAMILY OF CARDS TO BE USED IN THOSE POSITIONS.
3.	THE NUMBER IN PARENTHESES SHOWN IN CIRCUIT CARD CONNECTOR LOCATIONS INDICATES THE NUMBER OF CONNECTOR PINS. (36)—148440 CONNECTOR (72)—193263 CONNECTOR
4.	*—INDICATES LOCATION OF POLARIZING TABS, 148459. (THAT IS—SLOT 6 IS BETWEEN PINS 6&7.)
5.	N.O.—NORMALLY OPEN N.C.—NORMALLY CLOSED
6.	CABLE ASSEMBLY 326574 IS PART OF THE YESU 803.
7.	WIRE COLOR CODE: BK-BLACK BL-BLUE BR-BROWN P-PURPLE R-RED S-SLATE O-ORANGE W-WHITE G-GREEN Y-YELLOW

COMPONENT LOCATION



VIEWED FROM CARD SIDE



VIEWED FROM REAR

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8355WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-6-68	19710-R

WDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

PAGE 3C OF 7 C

ACTUAL WIRING DIAGRAM FOR THE R-T ELECTRICAL SERVICE UNIT YESU 803

APPROVALS

D AND R	E OF M
LDM	~

E-NUMBER

PROD. NO. 8355 WD

DATE 4-30-68

P.D. FILE NO. G-A354AA

DRAWN R.E.G. CHKD. [illegible]

ENGD. M.J.R. APPD. [illegible]

TELETYPE CORPORATION

8355WD

REFER TO PAGE 3C FOR NOTES.

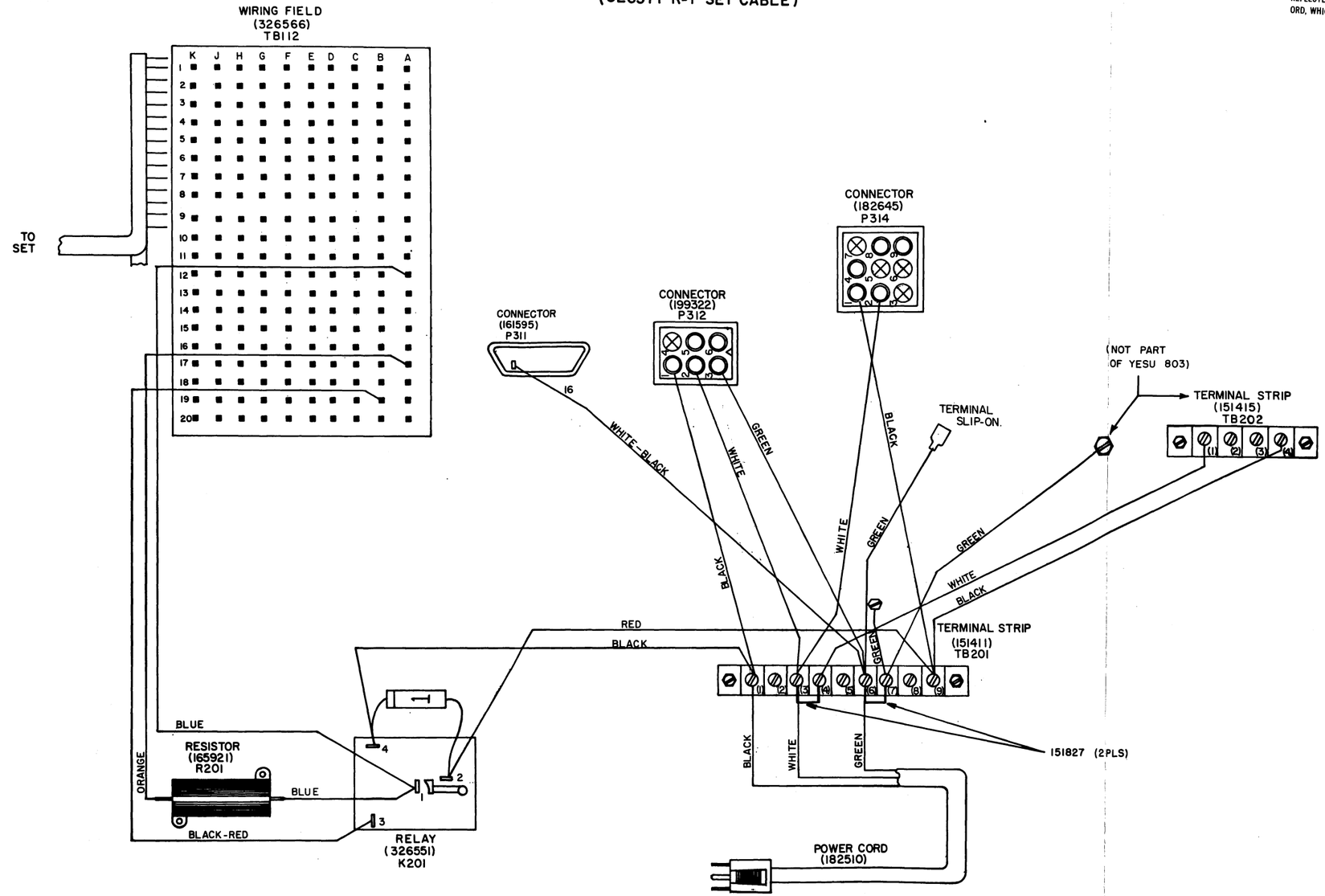
POWER CONNECTIONS
(326571 R-T SET CABLE)

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8355WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-6-68	19710-R
2	2-4-68	96751



WDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

PAGE 4C OF 7C

ACTUAL
WIRING DIAGRAM
FOR
THE R-T
ELECTRICAL SERVICE
UNIT
YESU 803

APPROVALS

D AND R	E OF M
LDm	

E-NUMBER

PROD. NO. 8355WD

DATE 9-6-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. | CHKD.

ENGD. M.J.R. | APPD.

TELETYPE
CORPORATION

8355WD

TC 454 (3-68)

REFER TO PAGE 3C FOR NOTES

TB 112 SIGNAL LOCATION

	A IN	B OUT	C	D	E	F	G	H	J	K
1	1	D 1	MESSAGE AVAILABLE (MA)	SEND MESSAGE (SM)	READY (R)	PRESENT CHARACTER (PC)	CHARACTER AVAILABLE (CA)	RUN	MANUAL STOP	AUTOMATIC STOP
2	2	A 2	CLUTCH MAGNET	CLOCK PULSE NO. 1	CLOCK PULSE NO. 2	TIGHT TAPE	TAPE OUT	BAT HANDLE		LOCAL
3	3	T 3				READER				
4	4	A 4	SELECTABLE	RECEIVE MESSAGE	READY (R)	DATA (D)	EOT	FEEDOUT TIMED	NORMALIZE	
5	5	B 5				PUNCH				
6	6	I 6								
7	7	T 7								
8	8	S 8								
9	FRAME GROUND	FRAME GROUND	GROUND	TA PE ALARM LAMP	TAPE ALARM N.O.	TAPE ALARM N.C.				
10	+ 5 VOLTS.	+ 5 VOLTS.	GROUND	STEP LAMP	STEP N.O.	STEP N.C.				
11	GROUND	GROUND	GROUND	READER CONTROL BACKSPACE LAMP	BACKSPACE N.O.	BACKSPACE N.C.				
12	+ 12 VOLTS.	+ 12 VOLTS.	GROUND	FEEDOUT LAMP	FEEDOUT N.O.	FEEDOUT N.C.				
13	+ 12 VOLTS.	+ 12 VOLTS.	GROUND	LAST CHARACTER VISIBLE LAMP	LAST C HARACTER VISIBLE N. O.	LAST CHARACTER VISIBLE N.C.				
14	− 12 VOLTS.	− 12 VOLTS.	GROUND	LAMP	N.O.	N.C.				
15	HIGH CURRENT GROUND			PUNCH CONTROL						
16	CHARACTER DETECTED N.O.	SELECTOR MAGNET	PRINT SUPPRESS MAGNET	AUXILIARY N.O.	AUXILIARY N.C.	NO. 1 N.O.	NO. 1 N.C.	NO. 2 N.O.	NO. 2 N.C.	
17	SELECTOR MAGNET AND RESISTOR	TAPE OUT	LOW TAPE	NO. 3 N.O.	NO. 3 N.C.	NO. 4 N.O.	NO. 4 N.C.	NO. 5 N.O.	NO. 5 N.C.	
18		FEEDOUT COIL	RIBBON MAGNET	NO. 6. N.O.	NO. 6. N.C.	NO. 7 N.O.	NO. 7. N.C.	NO. 8 N.O.	NO. 8. N.C.	
19		MOTOR CONTROL RELAY		PUNCH		CODE	READING	CONTACTS		
20		PUNCH								

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8355WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-6-68	19710-R

WDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

PAGE 5C OF 7C

ACTUAL
WIRING DIAGRAM
FOR
THE R-T
ELECTRICAL SERVICE
UNIT
YESU 803

APPROVALS

D AND R	E OF M
LDM	

E-NUMBER

PROD. NO. 8355 WD

DATE 4-30-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. CHKD.

ENGD. M.J.R. APPD.

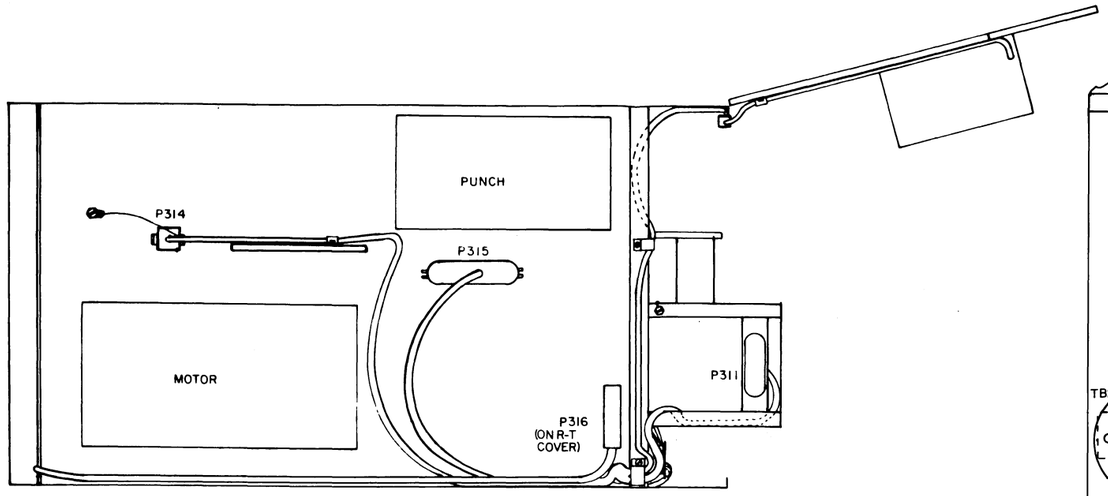
TELETYPE
CORPORATION

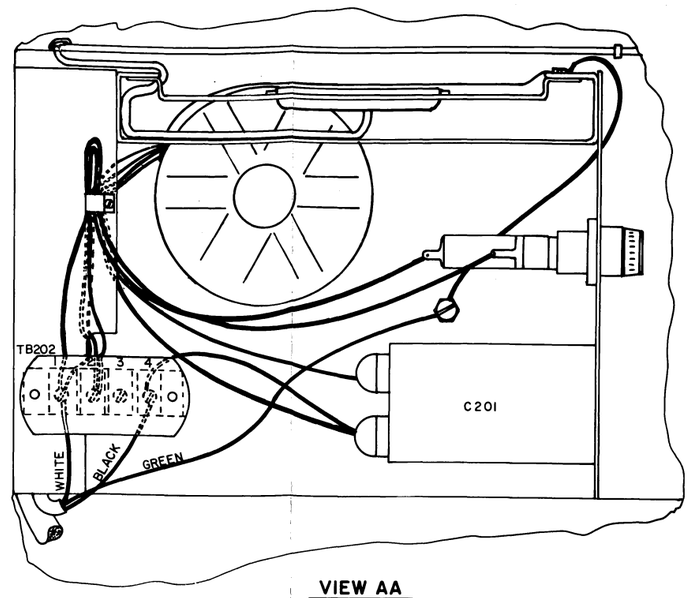
8355WD

1

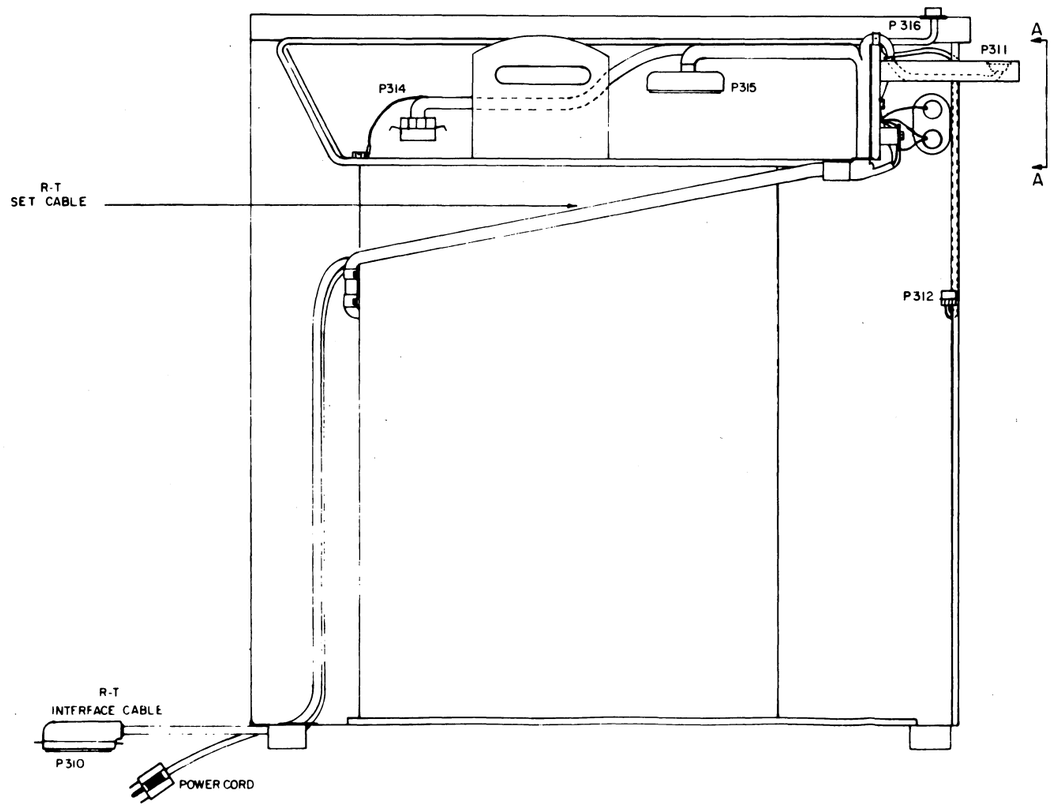
SEE PAGE 3C FOR NOTES

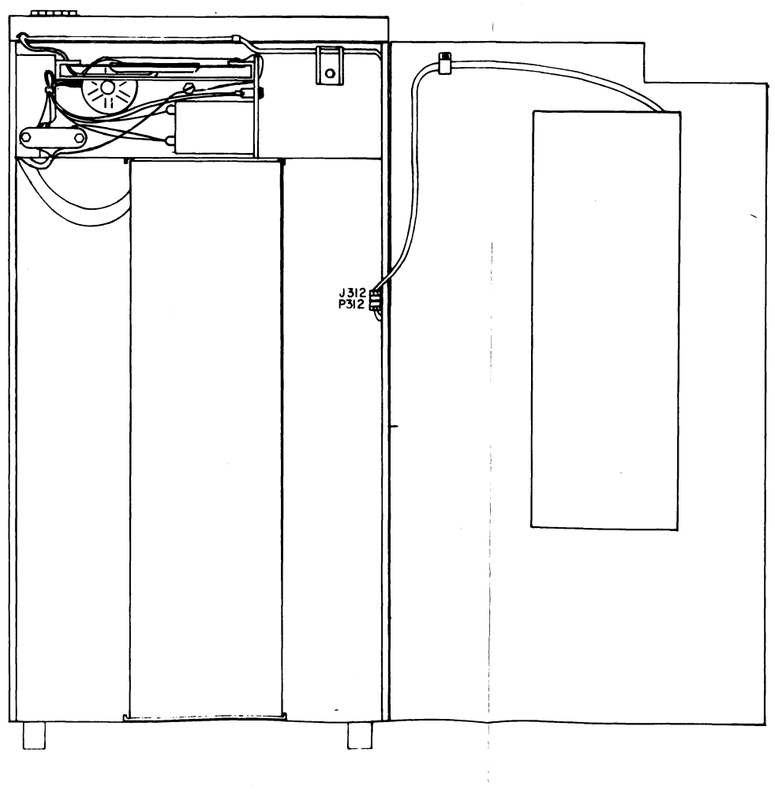
CABLE ROUTING





VIEW AA





8355WD		
REVISIONS		
ISSUE	DATE	AUTH. NO.
1	12-6-68	19710-R

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

WDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

PAGE 6C OF 7 C

ACTUAL
WIRING DIAGRAM
FOR THE R-T
ELECTRICAL SERVICE
UNIT
YESU 803

APPROVALS	
D AND R	E OF M
L.D.M	

E-NUMBER	
PROD. NO. 8355 WD	
DATE 7-31-68	
P.D. FILE NO. G-A354AA	
DRAWN W.P.B	CHKD.
ENGD. M.J.R	APPD.

TELETYPE
CORPORATION

8355WD

SEE PAGE 3C FOR NOTES.

□ - INDICATES SPARE.
ALL WIRE 24 AWG. UNLESS OTHERWISE INDICATED.
△ - INDICATES 18 AWG. WIRE.
○ - INDICATES TWISTED PAIR, NUMBERS ENCIRCLED INDICATE PAIRS.

CABLE TERMINATIONS.

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

R-T INTERFACE CABLE				R-T SET CABLE			
CABLE NO. 326574 (SEE NOTE 6)				CABLE NO. 326571			
TB112	CONN.	TERM.	WIRE COLOR.	TB112	CONN.	TERM.	WIRE COLOR.
1B	P310	24	W-BR	1A	P311	8	BK-S
1C	P310	19	R-BL	2A	P311	1	BR
1D	P310	20	BR-BL	2C ①	P311	14	W-BK-O
1E	P310	21	BK-BL	2D	P311	35	R-Y
1F	P310	22	O-G	2E	P311	31	R-O
1G	P310	23	BL-S	2F	P312	5	R-S
1H	P310	32	BL	2F	P311	12	W-BK-G
1J	P310	33	W	2G	P311	33	BK-Y
1K	P310	34	O	2H	P311	18	BK-G
2B	P310	25	W-R	3A	P311	2	R
2K	P310	10	BK-S	4A	P311	3	O
3B	P310	26	W-O	5A	P311	4	Y
4B	P310	27	W-Y	6A	P311	5	G
4C	P310	1	R-G	7A	P311	6	BL
4D	P310	2	BR-G	8A	P311	7	P
4E	P310	3	BK-G	9C	P311	10	BK
4F	P310	4	O-S	11E ⑥	P315	18	BK-R
4G	P310	5	W-R-O	12A ①	P311	15	BK-O
4H	P310	6	W-R-BR	12A ⑧	□		BL
4J	P310	9	P	12C	P314	8	S
5B	P310	28	W-G	12C	P312	6	BK-BR
6B	P310	29	W-BL	13A ③	P315	15	BR-S
7B	P310	30	W-P	13A ④	P315	12	BR-Y
8B	P310	31	W-S	13B ⑤	P315	4	BL-G
□ 21	P310	11	BR	13B ⑥	P315	19	BK-G
□ 21	P310	12	S	13C	P315	30	BK
□ 21	P310	13	R	13E ④	P315	1	BK-O
□ 21	P310	45	W-R-Y	14C ⑦	P315	7	O-G
□ 21	P310	46	W-BK-G	16A ⑦	P315	8	O-S
□ 21	P310	47	W-BK-O	16B ②	P315	16	BL
□ 21	P310	48	Y-G	16C ③	P315	14	W-O-BR
				16D	P315	46	P
△ 10A	P310	40	BL	16E	P315	45	W-P
△ 10A	P310	41	BL	16F	P315	28	BK-S
△ 11A	P310	35	BK	16G	P315	44	BK-BR
△ 11A	P310	36	BK	16H	P315	27	Y
△ 12A	P310	17	G	16J	P315	43	G
△ 12A	P310	18	G	17A	□		O
△ 14A	P310	15	Y	17A ②	P315	17	R
△ 14A	P310	16	Y	17B	P314	4	W-R-G
				17C	P314	9	BL-S
				17D	P315	26	S
				17E	P315	42	W-BR
				17F	P315	25	W-Y
				17G	P315	41	W-G
				17H	P315	24	W-R
				17J	P315	40	W-BR
				18D	P315	23	Y-G
				18E	P315	39	R-BL
				18F	P315	22	R-G
				18G	P315	38	BR-BL
				18H	P315	21	BR-G
				18J	P315	37	BK-BL
				19B ⑧	□		BK-R
				18B ⑤	P315	3	BL-S

8355WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-6-68	19710-R

WDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

PAGE 7C OF 7C

ACTUAL
WIRING DIAGRAM
FOR
THE R-T
ELECTRICAL SERVICE
UNIT
YESU 803

APPROVALS

D AND R	E OF M
LDM	

E-NUMBER

PROD. NO. 8355 WD.

DATE 8-27-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. CHKD.

ENGD. R.E.L. APPD.

TELETYPE
CORPORATION

8355WD

RM-151696 (9-65)

TELETYPE

NETWORK LISTING (TABULAR WIRING DIAGRAM) - INDEX

WDP

TITLE
ACTUAL WIRING DIAGRAM FOR R-T ELECTRICAL SERVICE UNIT YESU803

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE 1X OF
8355WD	3	MODEL 37	05/01/69	

NOTE: REVISION R- MATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

COMPONENT	PIN	NET
TB112	A 1	0001
TB112	A 2	0002
TB112	A 3	0003
TB112	A 4	0004
TB112	A 5	0005
TB112	A 6	0006
TB112	A 7	0007
TB112	A 8	0008
TB112	A 9	0009
TB112	A10	0010
TB112	A11	0011
TB112	A12	0012
TB112	A13	0012
TB112	A14	0013
TB112	A17	0014
TB112	B 1	0015
TB112	B 2	0016
TB112	B 3	0017
TB112	B 4	0018
TB112	B 5	0019
TB112	B 6	0020
TB112	B 7	0021
TB112	B 8	0022
TB112	B 9	0009
TB112	B10	0010
TB112	B11	0011
TB112	B12	0012
TB112	B13	0012
TB112	B14	0013
TB112	B16	0023
TB112	B17	0024
TB112	B18	0025
TB112	B19	0026
TB112	C 1	0027
TB112	C 2	0028
TB112	C 4	0029
TB112	C 9	0011
TB112	C10	0011
TB112	C11	0011
TB112	C12	0011
TB112	C13	0011
TB112	C14	0011
TB112	C16	0030
TB112	C17	0031
TB112	D 1	0032
TB112	D 2	0033
TB112	D 4	0034
TB112	D 9	0035
TB112	D14	0036
TB112	D16	0037
TB112	D17	0038
TB112	D18	0039
TB112	E 1	0040
TB112	E 2	0041
TB112	E 4	0042
TB112	E10	0043
TB112	E12	0044
TB112	E14	0045
TB112	E16	0046
TB112	E17	0047
TB112	E18	0048
TB112	F 1	0049
TB112	F 2	0050
TB112	F 3	0051
TB112	F 4	0052
TB112	F14	0053
TB112	F16	0054
TB112	F17	0055
TB112	F18	0056
TB112	G 1	0057
TB112	G 2	0058
TB112	G 3	0059
TB112	G 4	0060
TB112	G16	0061
TB112	G17	0062
TB112	G18	0063
TB112	H 1	0064
TB112	H 2	0065
TB112	H 4	0066
TB112	H16	0067
TB112	H17	0068
TB112	H18	0069
TB112	J 1	0070
TB112	J 4	0071
TB112	J16	0072
TB112	J17	0073
TB112	J18	0074
TB112	K 1	0075
TB112	K 2	0076
XZ107	1	0010
XZ107	2	0011
XZ107	3	0014
XZ107	4	0034
XZ107	5	0052
XZ107	6	0023
XZ107	8	0076
XZ107	9	0026
XZ107	14	0012
XZ107	15	0013
XZ108	A 6	0053
XZ108	A 7	0045
XZ108	A 8	0076
XZ108	A22	0041
XZ108	A23	0033
XZ108	A24	0064
XZ108	A27	0032
XZ108	A29	0040
XZ108	A30	0028
XZ108	A31	0057
XZ108	A33	0036
XZ108	A34	0042
XZ108	B 1	0010
XZ108	B 2	0011
XZ108	B 3	0001
XZ108	B 4	0003
XZ108	B 5	0002
XZ108	B 6	0004
XZ108	B 7	0017
XZ108	B 8	0018
XZ108	B 9	0016
XZ108	B10	0015
XZ108	B11	0020
XZ108	B12	0022
XZ108	B13	0021
XZ108	B14	0019
XZ108	B15	0005
XZ108	B16	0007
XZ108	B17	0008
XZ108	B18	0006
XZ108	B19	0075
XZ108	B20	0027
XZ108	B21	0050
XZ108	B22	0051
XZ108	B23	0058
XZ108	B24	0031
XZ108	B25	0059
XZ108	B26	0024
XZ108	B27	0065
XZ108	B28	0070
XZ108	B30	0029
XZ108	B31	0043
XZ108	B32	0049
XZ108	B33	0035
XZ108	B34	0034
XZ108	B35	0012
XZ108	B36	0013
XZ110	1	0010
XZ110	2	0011
XZ110	5	0061
XZ110	6	0054
XZ110	7	0072
XZ110	8	0067
XZ110	9	0046
XZ110	10	0037
XZ110	12	0047
XZ110	13	0038
XZ110	14	0062
XZ110	15	0055
XZ110	16	0073

TELETYPE

NETWORK LISTING (TABULAR WIRING DIAGRAM) - INDEX

TITLE
ACTUAL WIRING DIAGRAM FOR R-T ELECTRICAL SERVICE UNIT YESU803

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
8355WD	3	MODEL 37	05/01/69	PAGE 2X OF

COMPONENT	PIN	NET
XZ110	17	0068
XZ110	18	0048
XZ110	19	0039
XZ110	20	0063
XZ110	21	0056
XZ110	22	0074
XZ110	23	0069
XZ110	26	0071
XZ110	28	0060
XZ110	29	0030
XZ110	35	0012
XZ110	36	0013
XZ207	22	0010
XZ207	23	0011
XZ207	25	0066
XZ207	27	0052
XZ207	29	0071
XZ207	33	0044
XZ207	34	0025
XZ207	35	0012
XZ207	36	0013

OF PINS - 180

END OF LISTING

COMPONENT	PIN	NET

COMPONENT	PIN	NET

TELETYPE

NETWORK LISTING (TABULAR WIRING DIAGRAM)

WDP

TITLE: ACTUAL WIRING DIAGRAM FOR R-T ELECTRICAL SERVICE UNIT YESU803

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
8355WD	3	MODEL 37	05/01/69	1 OF

NET	COMPONENT	PIN
0001	TB112	A 1
0001	XZ108	B 3
0002	TB112	A 2
0002	XZ108	B 5
0003	TB112	A 3
0003	XZ108	B 4
0004	TB112	A 4
0004	XZ108	B 6
0005	TB112	A 5
0005	XZ108	B15
0006	TB112	A 6
0006	XZ108	B18
0007	TB112	A 7
0007	XZ108	B16
0008	TB112	A 8
0008	XZ108	B17
0009	TB112	A 9
0009	TB112	B 9
0010	TB112	B10
0010	TB112	A10
0010	XZ110	1
0010	XZ108	B 1
0010	XZ107	1
0010	XZ207	22
0011	TB112	C 9
0011	TB112	C10
0011	TB112	C11
0011	• TB112	C12
0011	• TB112	C13
0011	• TB112	C14
0011	TB112	B11
0011	TB112	A11
0011	XZ110	2
0011	XZ108	B 2
0011	XZ107	2
0011	XZ207	23
0012	TB112	A12
0012	TB112	B12
0012	TB112	B13
0012	TB112	A13
0012	XZ110	35
0012	XZ108	B35
0012	XZ207	35
0012	XZ107	14
0013	TB112	B14
0013	TB112	A14
0013	XZ110	36
0013	XZ108	B36
0013	XZ207	36
0013	XZ107	15
0014	TB112	A17
0014	XZ107	3
0015	TB112	B 1
0015	XZ108	B10
0016	TB112	B 2
0016	XZ108	B 9
0017	TB112	B 3
0017	XZ108	B 7
0018	TB112	B 4
0018	XZ108	B 8
0019	TB112	B 5
0019	XZ108	B14
0020	TB112	B 6
0020	XZ108	B11
0021	TB112	B 7
0021	XZ108	B13
0022	TB112	B 8
0022	XZ108	B12
0023	TB112	B16
0023	XZ107	6
0024	TB112	B17
0024	XZ108	B26
0025	TB112	B18
0025	XZ207	34
0026	TB112	B19
0026	XZ107	9
0027	TB112	C 1
0027	XZ108	B20

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

TELETYPE

NETWORK LISTING (TABULAR WIRING DIAGRAM)

TITLE
ACTUAL WIRING DIAGRAM FOR R-T ELECTRICAL SERVICE UNIT YESU803

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE	OF
8355WD	3	MODEL 37	05/01/69	2	

NET	COMPONENT	PIN
0028	TB112	C 2
0028	XZ108	A30
0029	TB112	C 4
0029	XZ108	B30
0030	TB112	C16
0030	XZ110	29
0031	TB112	C17
0031	XZ108	B24
0032	TB112	D 1
0032	XZ108	A27
0033	TB112	D 2
0033	XZ108	A23
0034	TB112	D 4
0034	XZ108	B34
0034	XZ107	4
0035	TB112	D 9
0035	XZ108	B33
0036	TB112	D14
0036	XZ108	A33
0037	TB112	D16
0037	XZ110	10
0038	TB112	D17
0038	XZ110	13
0039	TB112	D18
0039	XZ110	19
0040	TB112	E 1
0040	XZ108	A29
0041	TB112	E 2
0041	XZ108	A22
0042	TB112	E 4
0042	XZ108	A34
0043	TB112	E10
0043	XZ108	B31
0044	TB112	E12
0044	XZ207	33
0045	TB112	E14

NET	COMPONENT	PIN
0045	XZ108	A 7
0046	TB112	E16
0046	XZ110	9
0047	TB112	E17
0047	XZ110	12
0048	TB112	E18
0048	XZ110	18
0049	TB112	F 1
0049	XZ108	B32
0050	TB112	F 2
0050	XZ108	B21
0051	TB112	F 3
0051	XZ108	B22
0052	TB112	F 4
0052	XZ107	5
0052	XZ207	27
0053	TB112	F14
0053	XZ108	A 6
0054	TB112	F16
0054	XZ110	6
0055	TB112	F17
0055	XZ110	15
0056	TB112	F18
0056	XZ110	21
0057	TB112	G 1
0057	XZ108	A31
0058	TB112	G 2
0058	XZ108	B23
0059	TB112	G 3
0059	XZ108	B25
0060	TB112	G 4
0060	XZ110	28
0061	TB112	G16
0061	XZ110	5
0062	TB112	G17
0062	XZ110	14

TELETYPE

NETWORK LISTING (TABULAR WIRING DIAGRAM)

TITLE ACTUAL WIRING DIAGRAM FOR R-T ELECTRICAL SERVICE UNIT YESU803

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE	OF
8355WD	3	MODEL 37	05/01/69	3	

NET	COMPONENT	PIN
0063	TB112	G18
0063	XZ110	20
0064	TB112	H 1
0064	XZ108	A24
0065	TB112	H 2
0065	XZ108	B27
0066	TB112	H 4
0066	XZ207	25
0067	TB112	H16
0067	XZ110	8
0068	TB112	H17
0068	XZ110	17
0069	TB112	H18
0069	XZ110	23
0070	TB112	J 1
0070	XZ108	B28
0071	XZ207	29
0071	TB112	J 4
0071	XZ110	26
0072	TB112	J16
0072	XZ110	7
0073	TB112	J17
0073	XZ110	16
0074	TB112	J18
0074	XZ110	22
0075	TB112	K 1
0075	XZ108	B19
0076	TB112	K 2
0076	XZ107	8
0076	XZ108	A 8

NUMBER OF WIRES - 104

END OF LISTING

NET	COMPONENT	PIN

260

NO.	NOTES
	SEE SHEET 1 OF WIRING DIAGRAM FOR NOTES.

SUPPORTING INFORMATION	
CATEGORY	NO.

CONTENTS	SHEET NO.
WIRING FIELD, CABLE ASSEMBLIES, AND CONTROL PANEL LAYOUTS.	1
WIRING FIELD CONNECTIONS FOR YESU 805	2
WIRING FIELD CONNECTIONS FOR YESU 807	3
WIRING FIELD CONNECTIONS FOR YESU 809	4
CONTROL PANEL MARKINGS FOR YESU 805, 807, 809	5
R-T WIRING FIELD CONNECTIONS, (YESU 803) R-T CONTROL PANEL MARKINGS (YESU 803)	6

WDP

ISSUE CONTROL RECORD

SHEET NO.	ISSUE 2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
1	X	X																
2		X																
3	X	X																
4		X																
5	X																	
6	X																	

8365WD

REVISIONS APPLYING TO THIS CONTROL RECORD

ISSUE	DATE	AUTH. NO.
1	9-30-68	19568-R
2	1-15-69	96482
3	2-24-69	96867

ISSUE CONTROL SHEET 1 OF 1

ANALYSIS CHART FOR MODEL 37 CONTROL PANEL ARRANGEMENTS

WD NUMBER 8365 WD

DRAWN W.P.B. CHKD

ENGD. M.J.R. APPD.

TELETYPE CORPORATION

8365WD

NO.	NOTES
1.	COLOR CODE: BK-BLACK R-RED BR-BROWN S-SLATE BL-BLUE P-PURPLE G-GREEN Y-YELLOW O-ORANGE W-WHITE
2.	N.O. - NORMALLY OPEN N.C. - NORMALLY CLOSED L - LAMP
3.	ASSOCIATED CABLE ASSEMBLIES: 326571 & 327807.
4.	IN ARRANGEMENTS THAT USE 3 CABLES. A 327807 CABLE ASSEMBLY MUST BE ORDERED SEPERATELY.
5.	IN ARRANGEMENTS WHERE 2 CABLES ARE SUPPLIED, BUT ONLY ONE SWITCH IS USED, SPARE CABLE TO BE TIED BACK INTO CABINET.
6.	POWER CONNECTIONS FOR 327807 CABLES:

CABLE	WIRE COLOR	WIRING FIELD TERMINAL NO.
A	BK	C12
	G	A12
B	BK	C13
	G	A12
C	BK	C14
	G	A13

7. PROGRAMMING:

1. THE STANDARD ARRANGEMENTS ARE AS FOLLOWS.

TELETYPEWRITER SET	ARRANGEMENT
RO	2
KSR	5
ASR	10

2. TO CHANGE ARRANGEMENTS
   1. DETERMINE FUNCTION REQUIRED
      A. USING SHEETS 2,3,4,5 FIND LOCATION OF FUNCTION ON WIRING FIELD.
      B. ASSIGN POSITION TO FUNCTION SELECTED ON CONTROL PANEL.
      C. FROM SHEETS 2,3,4, DETERMINE COLOR CODE OF WIRES PER SELECTION IN B.
      D. CONNECT WIRES TO TERMINAL BOARD TBIII, IN ACCORDANCE WITH DATA OF A.

8. SEE SHEET 6 FOR R-T CONTROL PANEL ARRANGEMENTS. ARRANGEMENT NO. 1 IS THE STANDARD R-T ARRANGEMENT.
   TO CHANGE R-T ARRANGEMENTS FOLLOW THE PROCEDURE OUTLINED IN NOTE 7 SECTION 2, USING SHEET 6 FOR WIRING INFORMATION.

9. ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.

10. POWER CONNECTIONS FOR 326571 CABLE:

WIRE COLOR	WIRING FIELD TERMINAL NO.
G	B12
G-BR	B14
G-BL	B14
BK	C10

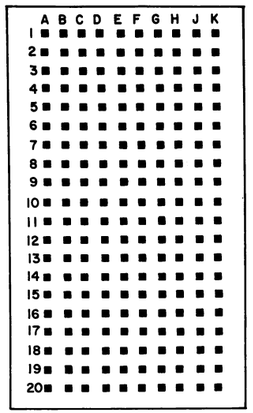
11. * TWO LETTER SUFFIX DENOTES ELECTRICAL SERVICE UNIT VARIATION.

12. ASSOCIATED (327807) CABLE ASSEMBLIES TO BE LABELLED NEAR CONNECTOR AS FOLLOWS:

CABLE LOCATION	PART NO.
A	79267 RM
B	79268 RM
C	79269 RM

13. ADD STRAP 327842 ON TBIII FROM G13 TO D12.

FIGURE 1
326566
WIRING FIELD
(TBIII RO, KSR, ASR)
(TBII2 R-T)



VIEWED FROM CARD SIDE OF SERVICE UNIT.

FIGURE 2
327807
CABLE ASSEMBLY

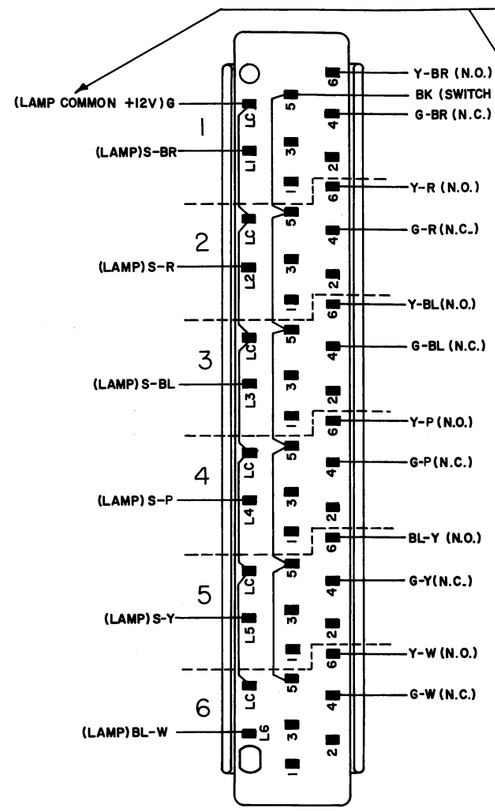


FIGURE 3
326571
CABLE ASSEMBLY
(R-T ONLY)

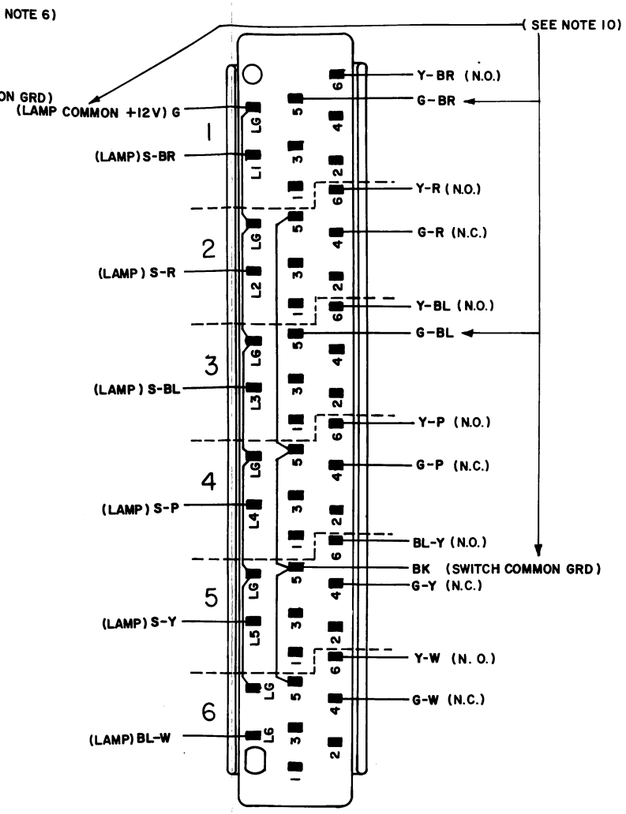


FIGURE 4
(VIEWED FROM FRONT OF UNIT)

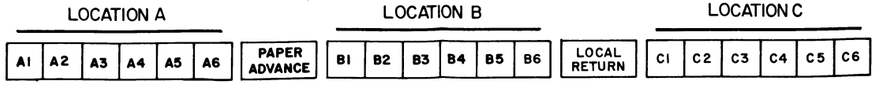
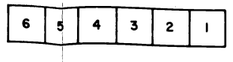


FIGURE 5
(VIEWED FROM TOP OF R-T)



NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8365WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-30-68	19568-R
2	1-15-69	96482
3	2-24-69	96867

WDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 1

ANALYSIS CHART FOR MODEL 37 CONTROL PANEL ARRANGEMENTS

APPROVALS

D AND R	E OF M

E-NUMBER

PROD. NO. 8365WD

DATE 4-18-68

P.D. FILE NO. G-A354AA

DRAWN RJP | CHKD.

ENGD. MJR | APPD.

TELETYPE CORPORATION

8365WD

SEE SHEET I FOR NOTES.

R-T
WIRING FIELD CONNECTIONS (YESU803) (SEE FIGURES 1&3)

POSITION NO. / FUNCTION (SEE NOTE 2) / WIRE COLOR / WIRING ARRANGEMENT / APPROPRIATE MARKINGS NO. (SEE R-T MARKINGS CHART) / REMARKS			6			5				4			3			2			1		
			N.O.	N.C.	L.	N.O.	N.C.	L.		N.O.	N.C.	L.	N.O.		L.	N.O.	N.C.	L.	N.O.		L.
			Y-W	G-W	BL-W	BL-Y	G-Y	S-Y		Y-P	G-P	S-P	Y-BL		S-BL	Y-R	G-R	S-R	Y-BR		S-BR
SEE NOTE 10	1	AA	E9	F9	D9	E10	F10			E14	F14	D14	E13		D13	E12	F12	D12	E11		

R-T
CONTROL PANEL MARKINGS (YESU 803) (SEE FIGURE 5)

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

NOTE 11			POSITION NO.					
MARKINGS NO.	ASSOC. YESU NO.	WIRING ARRG'T	6	5	4	3	2	1
1	803/—	AA	TAPE ALARM	READER STEP				PUNCH BACK SPACE

8365WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-30-68	19568-R
2	1-15-69	96482

WDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 6

ANALYSIS CHART FOR MODEL 37 CONTROL PANEL ARRANGEMENTS

APPROVALS

D AND R	E OF M
HJK	

E-NUMBER

PROD. NO. 8365WD

DATE 4-18-68

P.D. FILE NO. G-A354AA

DRAWN R.E.G. | CHKD.

ENGD. M.J.R. | APPD.

TELETYPE CORPORATION

8365WD

NOTES

1. WIRING LEGEND

2. COLOR CODE

BK	BLACK	W Y	WHITE YELLOW
BR	BROWN	W G	WHITE GREEN
R	RED	W BL	WHITE BLUE
O	ORANGE	W P	WHITE PURPLE
Y	YELLOW	W S	WHITE SLATE
G	GREEN	BK R	BLACK RED
BL	BLUE	BK Y	BLACK YELLOW
P	PURPLE	BK G	BLACK GREEN
S	SLATE	R Y	RED YELLOW
W BK	WHITE BLACK	R G	RED GREEN
W BR	WHITE BROWN	W BK Y	WHITE BLACK YELLOW
W R	WHITE RED	W BK G	WHITE BLACK GREEN
W O	WHITE ORANGE	W R Y	WHITE RED YELLOW

3. CONTACTS SHOWN IN UNOPERATED POSITION.

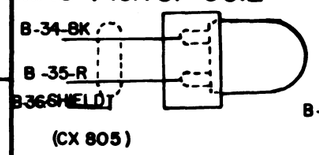
4. NUMBERS ENCLOSED BY PARENTHESES ( ) ARE USED FOR REFERENCE AND ARE NOT NECESSARILY SHOWN ON THE PARTS.

5. STRAP WITH *22 GAGE WIRE AS INDICATED.

6. (*) INDICATES ADDITIONAL WIRES IN 171250 CABLE ASSEMBLY.

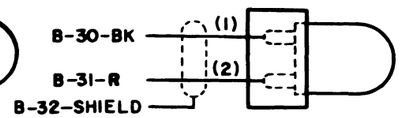
ET-108147
TC255(6-54)

H
MAG-PICK-UP COIL

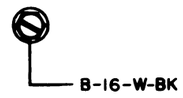


(CX 805)

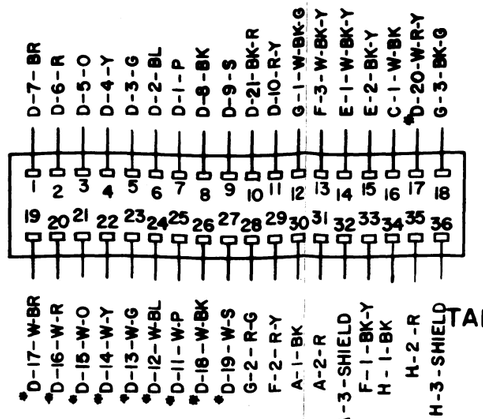
A
MAGNETIC PICK-UP COIL



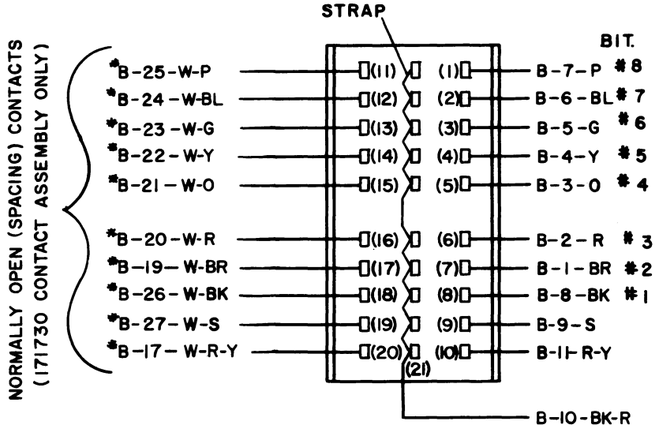
C
GROUND SCREW



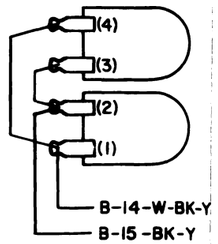
B
CONNECTOR (PLUG)
(VIEWED FROM RECEPTACLE END)



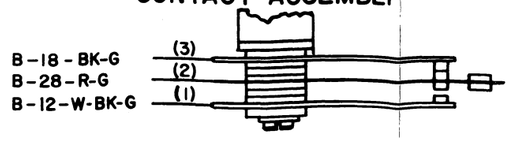
D
CODE READING CONTACT ASSEMBLY
(VIEWED FROM SOLDER TERMINAL END)



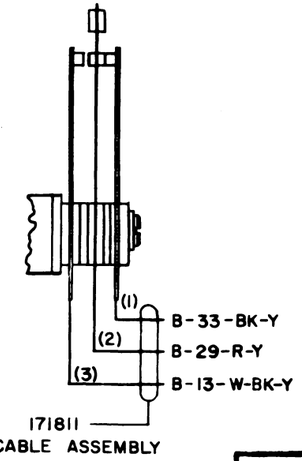
E
OPERATE MAGNET COILS



G
START-STOP (TIGHT-TAPE) CONTACT ASSEMBLY



F
TAPE-OUT CONTACT ASSEMBLY



5072 WD

ISSUE	DATE	AUTH. NO.
2	2-23-60	HS 1000
3	6-6-67	94052

ACTUAL WIRING DIAGRAM CX READER

APPROVALS	
D AND R	E OF M

E-NUMBER

PROD. NO. 5072 WD

DATE: 12-20-59

P.D. FILE NO. 3-47.134 AA

DRAWN. R.B.B. | CHKD.

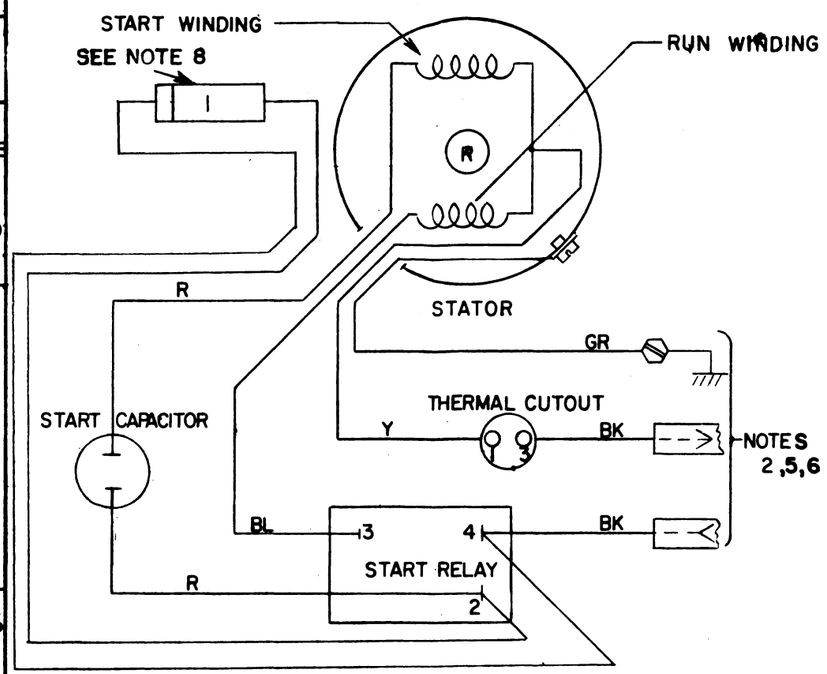
ENGD. J.F.K. | APPD.

TELETYPE CORPORATION

5072 WD

ET-131451

NO.	NOTES
1	SYNCHRONOUS MOTOR OPERATES ON REGULATED 60~±1% A.C. ONLY
2	BLACK LEADS ARE KEYED TO POLARITY BY MEANS OF OPPOSITE CONNECTORS. ALL UNITS MUST CONFORM—ATTACH GREEN LEAD TO CRADLE WHICH IS GROUNDED THRU THE BASE.
3	WIRE COLOR CODE BK – BLACK W – WHITE R – RED GR – GREEN BL – BLUE Y – YELLOW
4	TO BE USED WITH 115 V.A.C.±10% SOURCE ONLY
5	INDICATES MALE CONNR. INDICATES FEMALE CONNR.
6	LEAD FROM THERMAL CUT OUT TO BE CONNECTED TO LIVE SIDE OF AC POWER LINE.
7.	STARTING CAPACITOR VALUE 45-48 MFD.
8.	327828 0.3 120



YMU 2 SYNCHRONOUS MOTOR UNIT

7828 WD

REVISIONS

ISSUE	DATE	AUTH NO.
1	10-7-65	17311-R
2	8-26-66	91768
3	4-14-67	92496
4	7-14-67	94250
5	4-8-68	97429
6	8-23-68	95969

ACTUAL WIRING DIAGRAM OF MODEL 37 MOTOR UNIT YMU 2

APPROVALS

D AND R	E OF M
[illegible]	[illegible]

E NUMBER

PROD NO.

DATE 8/10/65

P.D FILE NO. [illegible]

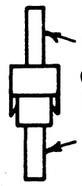
DRAWN PSD CHKD [illegible]

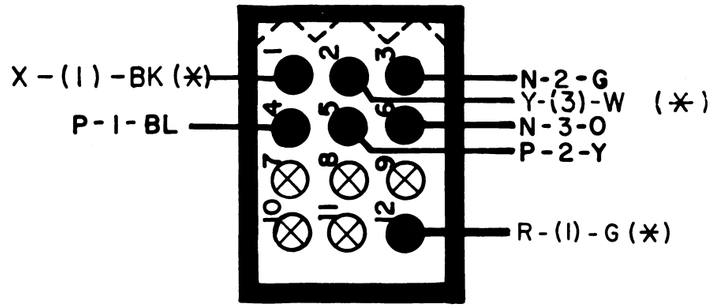
ENGD. BMA APPD [illegible]

TELETYPE CORPORATION

6

7828 WD

NO	NOTES
1.	WIRING LEGEND: N-3-W N — COLOR CODE 3 — DISTANT TERMINATING DESIGNATION. W — DISTANT TERMINATING AREA.
2.	ALL WIRE 24 GA. UNLESS OTHERWISE SPECIFIED.
3.	*DENOTES 18 GA. WIRE
4.	TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE AND ARE NOT MARKED ON COMPONENT.
5.	CONNECTOR VIEWED FROM TERMINAL END.
6.	ASSOCIATED CABLE: 306355 CABLE ASSEMBLY
7.	ASSOCIATED SCHEMATICS: 7880WD (I/O), 8398WD (EIA)
8.	COLOR CODE BK - BLACK W - WHITE BL - BLUE O - ORANGE Y - YELLOW G - GREEN
9	 INDICATES ONE PIN CONNECTOR COMPOSED OF A 306355 PIN IN 306359 HOUSING. 306358 SOCKET IN A 306360 HOUSING.
10	MOTOR CORD ASSEMBLY 306320

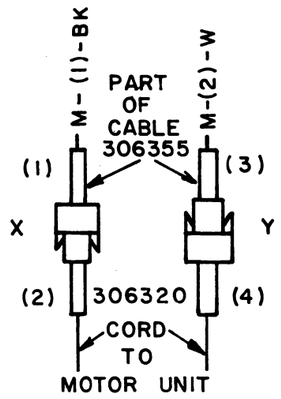


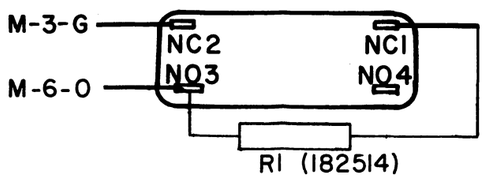
P304

M

181721

BASE CONNECTOR

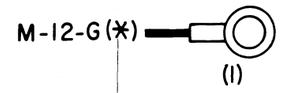




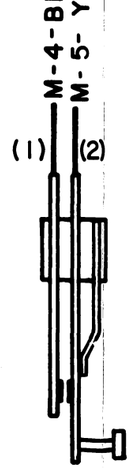
N

E. O. L. SWITCH

R



BASE GROUND CONNECTION



P

KEYBOARD RESET CONTACT

7874 WD

REVISIONS

ISSUE	DATE	AUTH NO
1	10-7-65	17311-R
2	12-13-65	89508
3	1-18-66	89515
4	7-12-66	90675
5	10-24-66	92154
6	5-20-68	95656
7	11-14-68	96411

WDP

ACTUAL WIRING DIAGRAM FOR MODEL 37 BASE (YB 800)

APPROVALS

D AND R	E OF M

E NUMBER

PROD. NO. 7874 WD

DATE: 9-22-65

P.D FILE NO. 1-30.354AA

DRAWN JCH CHKD

ENGD. JCH APPD

TELETYPE CORPORATION

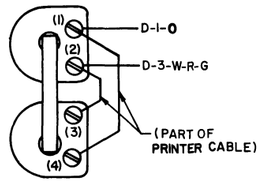
7874 WD

7

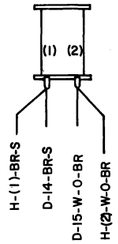
ETIC8147
TC255(11-64)

NO.	NOTES
1.	WIRING LEGEND: K-8-W K — DISTANT TERMINATING AREA. 8 — DISTANT TERMINATING DESIGNATION. W — WIRE COLOR CODE.
2.	TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE ONLY & NOT MARKED ON COMPONENT.
3.	CONNECTOR VIEWED FROM TERMINAL END.
4.	ALL WIRE 24 AWG. UNLESS OTHERWISE SPECIFIED.
5.	COLOR CODE LEGEND: BK - BLACK, BR - BROWN, R - RED, O - ORANGE, Y - YELLOW, G - GREEN, BL - BLUE, P - PURPLE, S - SLATE, W - WHITE
6.	CONNECT WIRES TO AREA F AS SHOWN PER PRINTER REQUIREMENTS

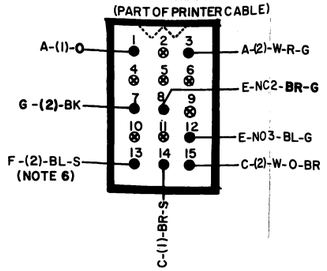
A
SELECTOR MAGNETS



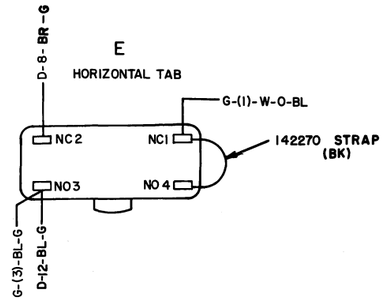
C
RIBBON MAGNET (RIGHT)



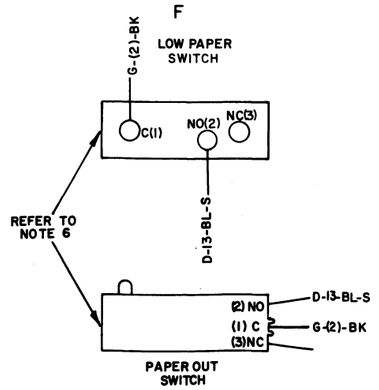
D
CONNECTOR (PART OF PRINTER CABLE)



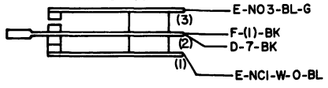
E
HORIZONTAL TAB



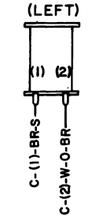
F
LOW PAPER SWITCH



G
VERT. TAB & FORM FEED SWITCH



H
RIBBON MAGNET (LEFT)



8362WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	5-27-68	19260-R
2	7-12-68	97839
3	1-8-69	96481

ACTUAL WIRING DIAGRAM FOR MODEL 37 TYPING UNITS YP806,808, YP811,814.

APPROVALS

D AND R	E OF M
1192	

E-NUMBER

PROD. NO. 8362 WD

DATE 10-24-67

P.D. FILE NO. 43-A25AA

DRAWN W.P.B. CHKD.

ENGD. M.J.R. APPD.

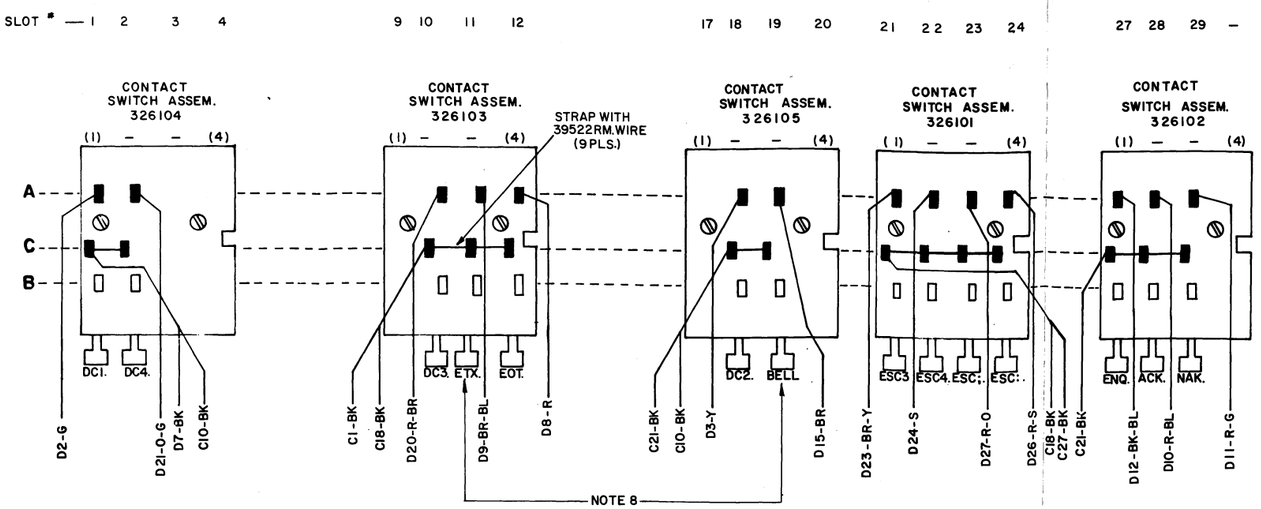
TELETYPE CORPORATION

8362WD

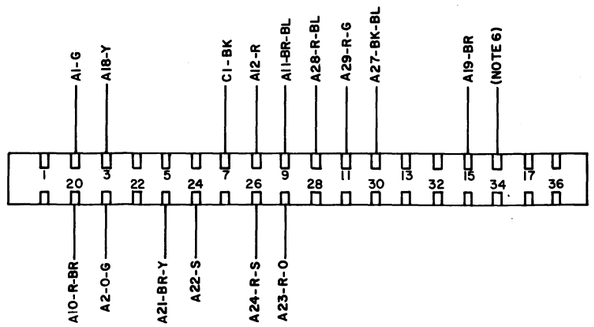
3

TC 484 (5-68)

NO.	NOTES
1.	WIRING LEGEND: C19 – BR WIRE COLOR CODE. DISTANT TERM. DESIGNATION. (STUNT BOX SLOT NUMBER AND CONTACT TERMINAL.) DISTANT TERM. AREA.
2.	ASSOCIATED CABLE: 327817
3.	COLOR CODE: BK-BLACK G-GREEN BR-BROWN BL-BLUE R-RED P-PURPLE O-ORANGE S-SLATE Y-YELLOW W-WHITE
6.	TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE, AND ARE NOT MARK ON COMPONENT.
7.	ALL UNUSED WIRE'S SHOULD BE TIED BACK ON CABLE BODY, CARE SHOULD BE TAKEN TO AVOID SHORTING OF UNTERMINATED WIRES TO PRINTER FRAME.
8.	YAC STUNT BOX ARRANGMENT HAS BELL LOCATED IN SLOT NO.11 WITH ITS ASSOCIATED D15-BR WIRE.



D
(J308)
CONNECTOR
161238



8363 WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	10-24-68	19260 R
2	4-22-69	99032

ACTUAL
WIRING DIAGRAM
FOR
STUNT BOX ARRANGEMENT
YAE - 319776
YAC - 319875
YAJ - 319655

APPROVALS

D. AND R.	E OF M.
L.W.H.	

E-NUMBER

PROD. NO. 8363 WD.

DATE 2-27-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. CHKD.

ENGD. M.J.R. APPD.

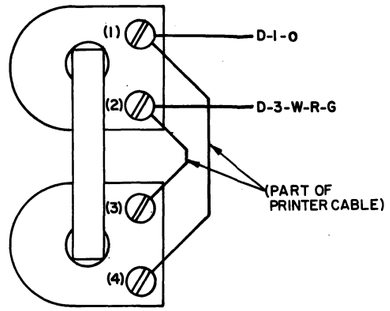
TELETYPE
CORPORATION

8363 WD

NO.	NOTES
1.	WIRING LEGEND: K-S-W K — WIRE COLOR CODE S — DISTANT TERMINATING DESIGNATION W — DISTANT TERMINATING AREA.
2.	TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE ONLY & NOT MARKED ON COMPONENT.
3.	CONNECTOR VIEWED FROM TERMINAL END.
4.	ALL WIRE 24 AWG. UNLESS OTHERWISE SPECIFIED.
5.	ASSOCIATED CABLE: 327814.
6.	COLOR CODE LEGEND: BK-BLACK G-GREEN BR-BROWN BL-BLUE R-RED P-PURPLE O-ORANGE S-SLATE Y-YELLOW W-WHITE
7.	ALL UNUSED WIRES SHOULD BE TIED BACK ON CABLE BODY. CARE SHOULD BE TAKEN TO AVOID SHORTING OF UNTERMINATED WIRES TO THE PRINTER FRAME.
8.	THE LOW PAPER SWITCH IS NOT PART OF THE BASIC PRINTERS. IT BELONGS TO THE LOW PAPER MOD. KIT NO. 319650.

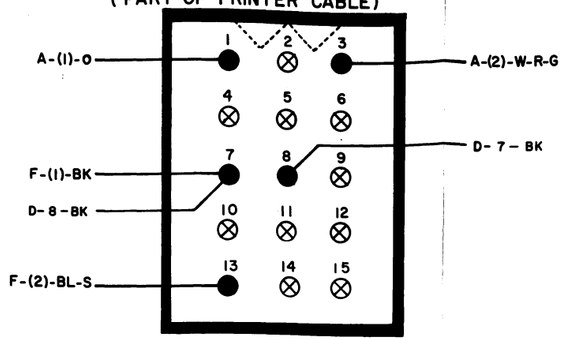
A

SELECTOR MAGNETS



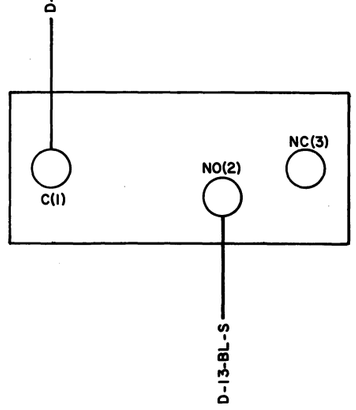
D

CONNECTOR
(PART OF PRINTER CABLE)



F (OPTIONAL)

LOW PAPER SWITCH (SEE NOTE-8)



8364WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	5-27-68	19260-R
2	9-17-68	97842
3	1-2-69	96573

ACTUAL WIRING DIAGRAM FOR MODEL 37 TYPING UNIT YP810, 813

APPROVALS

D AND R	E OF M
[illegible]	[illegible]

E-NUMBER

PROD. NO. 8364 WD

DATE 3-5-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. CHKD. [illegible]

ENGD. M.J.R. APPD. [illegible]

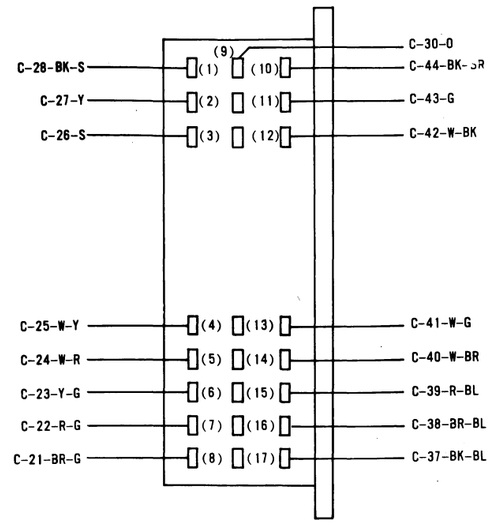
TELETYPE CORPORATION

8364WD

NO.	NOTES
1.	WIRING LEGEND: DISTANT TERMINATING AREA DISTANT TERMINATING DESIGNATION A-1-W-BL WIRE COLOR CODE
2.	COLOR CODE: BK - BLACK BR - BROWN R - RED O - ORANGE Y - YELLOW G - GREEN BL - BLUE P - PURPLE W - WHITE S - SLATE
3.	CONNECTOR VIEWED FROM BOTTOM.
4.	CABLE ASSEMBLIES: 326432 327007 (YRPE802)
5.	AUX. CONTACT VIEWED FROM TOP.

A

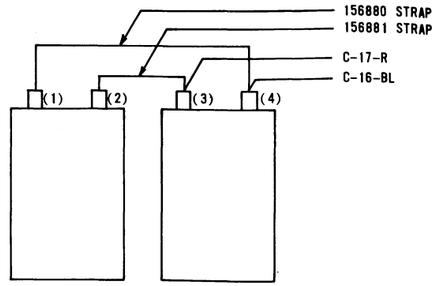
CODE READING CONTACTS
(194065)



PART OF YRPE802 ONLY

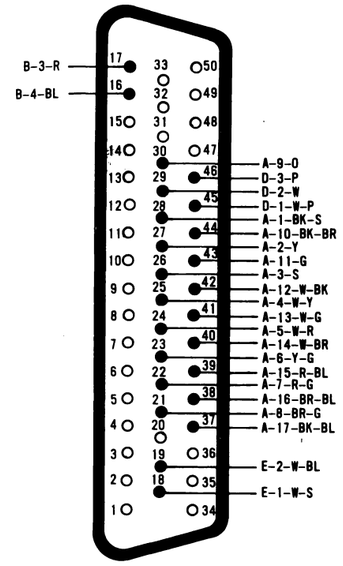
B

SELECTOR MAGNETS



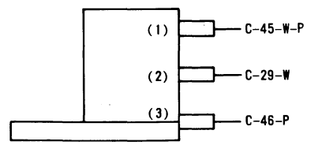
C

50 PIN CONNECTOR
(192013)



D

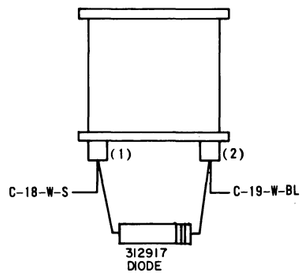
CODE READING
CONTACTS AUXILIARY
CONTACT



PART OF YPPE802 ONLY

E

BACKSPACE MAGNET



8494 WD .

REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-11-67	18983-R
2	9-17-68	96284

ACTUAL
WIRING DIAGRAM
FOR
YRPE800 & YRPE802
REPERFORATORS

APPROVALS

D AND R	E OF M

E-NUMBER

PROD. NO. 8494WD

DATE 7-6-67

P.D. FILE NO. I-A354.220A

DRAWN D.G.S. | CHKD.

ENGD. W.E.C. | APPD.

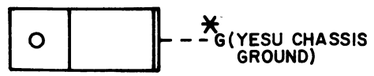
TELETYPE
CORPORATION

8494WD

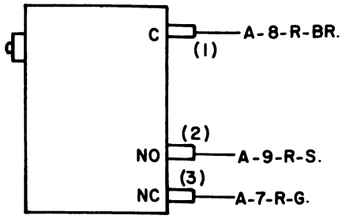
NO.	NOTES
1.	DISTANT TERMINATING AREA. DISTANT TERMINATING DESIGNATION. A-1-Y WIRE COLOR
2.	COLOR CODE: R-RED P-PURPLE BL-BLUE S-SLATE G-GREEN O-ORANGE Y-YELLOW W-WHITE BR-BROWN BK-BLACK
3.	RECEPTACLE VIEWED FROM BOTTOM.
4.	ASSOCIATED CABLES: 327010-REPERFORATOR BASE. 327033-DOOR.
5.	* INDICATES 18 GAGE WIRE

REPERFORATOR BASE

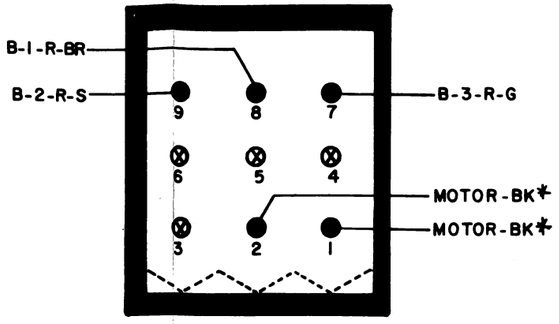
C
CHASSIS GROUND TERMINAL (180904)



B
LOW TAPE SWITCH (198757)

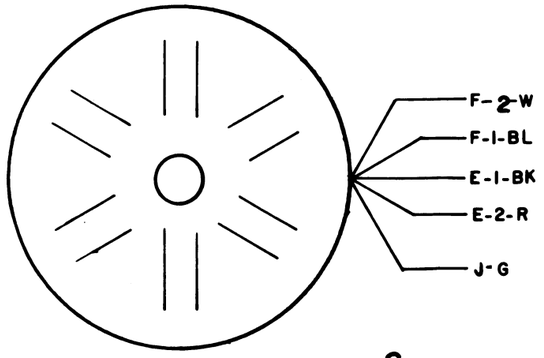


A
(J314)
RECEPTACLE (9 PIN)
(182716)

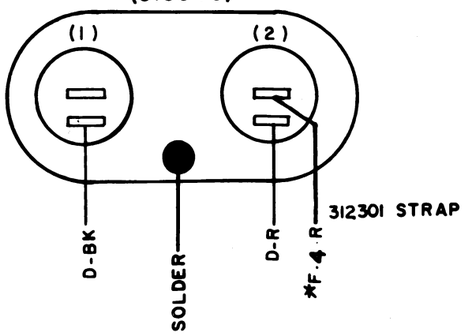


READER MOTOR BASE

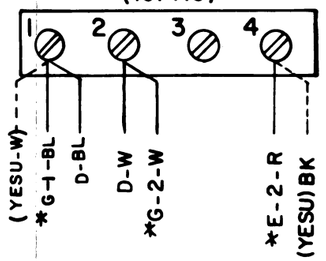
D
MOTOR
(326977)



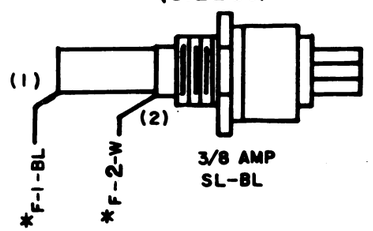
E
(C201)
CAPACITOR
(318843)



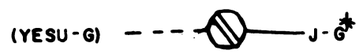
F
(TB202)
TERMINAL BLOCK
(151415)



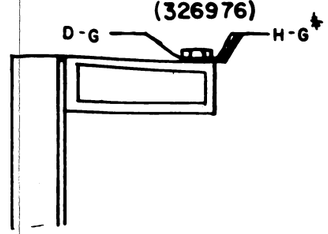
G
CABLE ASSEMBLY
(312299)



H
CABINET GROUND SCREW



J
MOTOR MTG. PLATE
(326976)



3

8497 WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	2-16-68	19157 R
2	10-21-68	96301
3	12-3-68	96543

ACTUAL WIRING DIAGRAM OF THE YAC800 RT CABINET

APPROVALS

D AND R	E OF M

E-NUMBER

PROD. NO. 8497 WD

DATE: 8-2-67

P.D. FILE NO. 1-A354.220A

DRAWN W.P.B	CHKD.
ENGD. W.E.C.	APPD.

TELETYPE CORPORATION

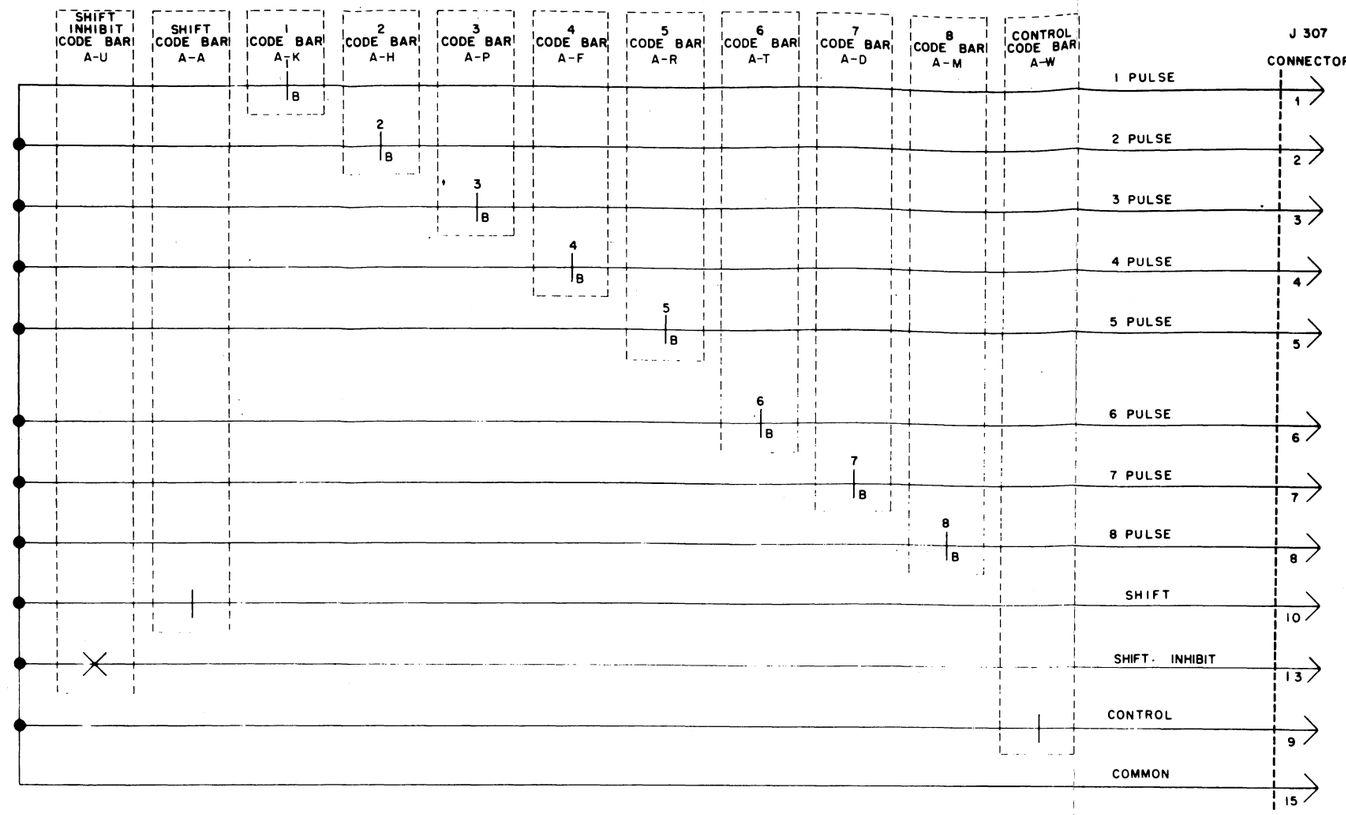
8497 WD

NO.	NOTES
1.	WIRING LEGEND DISTANT TERMINATING AREA DISTANT TERMINATING POINT COLOR CODE A L W-R-S
2.	ALL WIRE24 AWG.
3.	TERMINALS DESIGNATIONS ENCLOSED IN PARENTHESES APE FOR REFERENCE AND ARE NOT MARKED ON COMPONENT.
4.	1 THROUGH 8 CODE BARS ARE SHOWN IN THE MARKING POSITION. SHIFT, CONTROL AND SHIFT INHIBIT CONTACTS ARE SHOWN IN THE UNOPERATED POSITION.
5.	ASSOCIATED CABLE : 324407
6.	→ INDICATES MALE TERMINAL OR CONNECTOR.
7.	ALL COMPONENTS VIEWED FROM WIRE INSERTION SIDE.

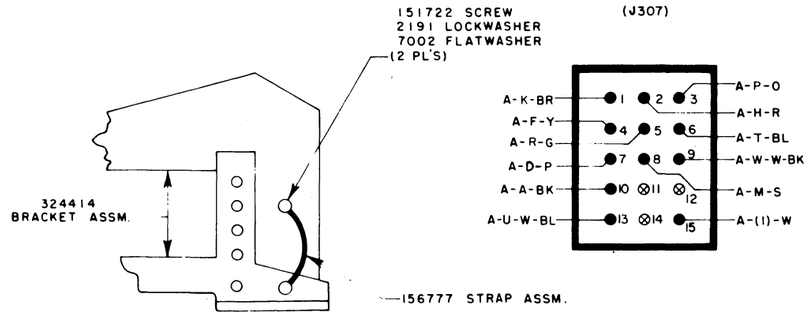
8500 WD

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	1-31-68	19025-R

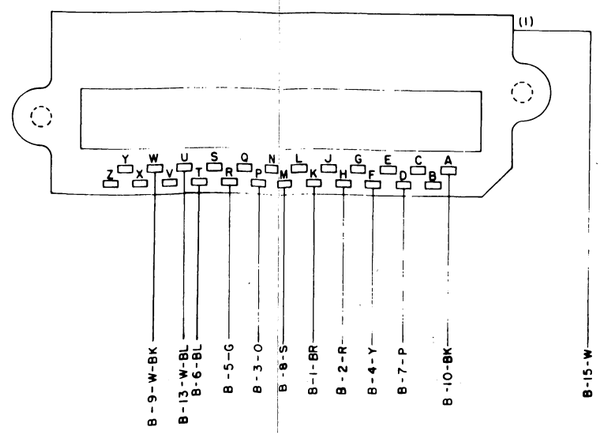
SCHEMATIC



B
CONNECTOR
312912
(J307)



A
RIGHT CONTACT BLOCK
(VIEWED FROM WIRE INSERTION SIDE)



ACTUAL

ACTUAL AND SCHEMATIC
WIRING DIAGRAMS FOR
YK801 AAY
THROUGH ZZY

APPROVALS	
D AND R	E OF M

E-NUMBER	
PROD. NO.	8500 WD
DATE	10 - 6 - 67
P.D. FILE NO.	1-18.354AA
DRAWN JMQ	CHKD.
ENGD. S.M.G.	APPD.

TELETYPE
CORPORATION

8500 WD

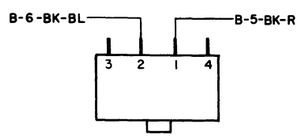
1

8558 WD

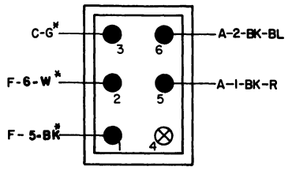
REVISIONS		
ISSUE	DATE	AUTH. NO.
1	2-21-68	19106R
2	8-29-68	96000

NO.	NOTES
1.	WIRING LEGEND F-5-BK (DISTANT TERM. AREA / DISTANT TERM. DESIG. / WIRE COLOR CODE)
2.	WIRE COLOR CODE BK-BLACK BL-BLUE W-WHITE BR-BROWN G-GREEN BK-BL-BLACK-BLUE S-SLATE BK-R-BLACK-RED
3.	ALL TERMINALS VIEWED FROM WIRING SIDE.
4.	ASSOCIATED CABLE ASSEMBLIES
5.	TERMINALS DESIGNATIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE AND ARE NOT MARKED ON COMPONENT
6.	REFER TO 8368 WD FOR SCHEMATIC WIRING DIAGRAM.
7.	* DENOTES 18 GA. WIRE
8.	COMPONENTS "A" THRU "H" USED ON 326955 DOOR W/WINDER COMPONENTS "A" THRU "R" USED ON 326960 DOOR W/WINDER AND UNWINDER.

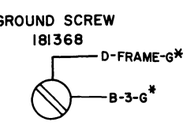
A
TIGHT TAPE SWITCH
174570



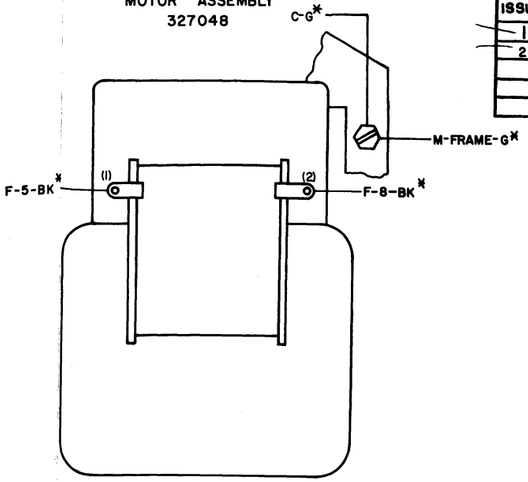
B
J 312
RECEPTACLE-6 PIN
182650



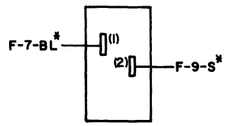
C
GROUND SCREW
181368



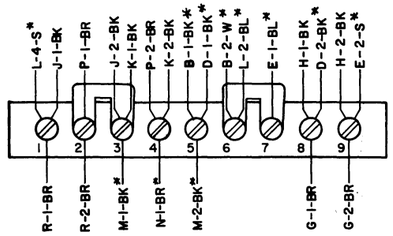
D
WINDER
MOTOR ASSEMBLY
327048



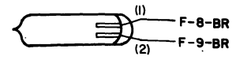
E
WINDER SWITCH
146802



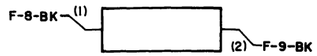
F
TERMINAL BLOCK
199804



G
MERCURY SWITCH
326932

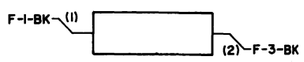


H
SPARK SUPPRESSION
NETWORK
309899



SEE NOTE 8

J
SPARK SUPPRESSION
NETWORK
309899



K
SPARK SUPPRESSION
NETWORK
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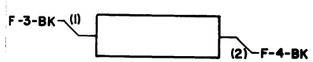

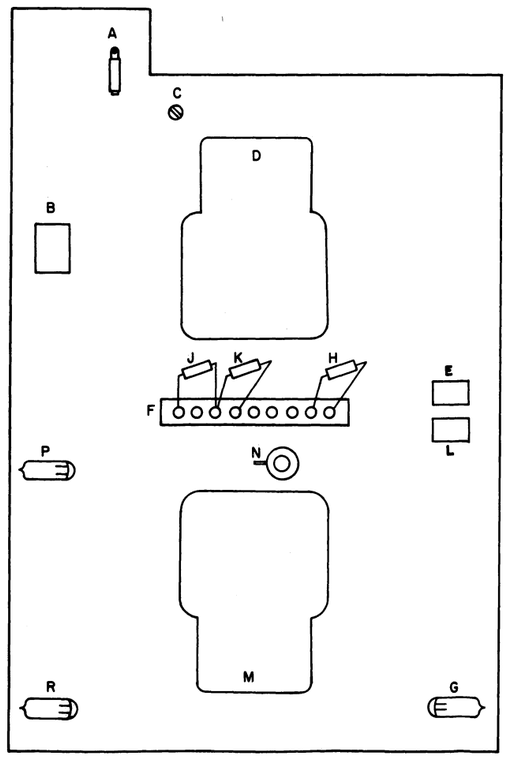

L
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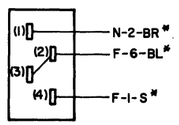
328283



M
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MOTOR ASSEMBLY
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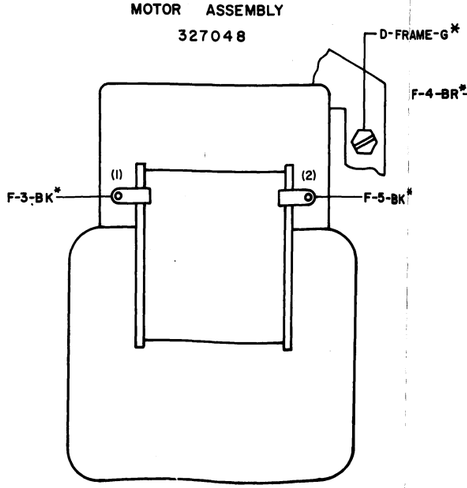

N
RESISTOR
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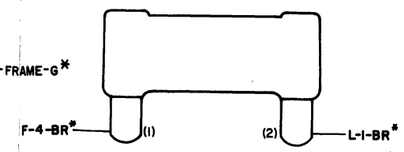

P
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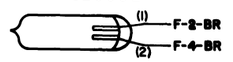

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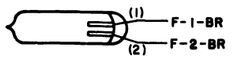

ACTUAL WIRING DIAGRAM OF THE YAC 800 RT CABINET DOORS 326955 AND 326960

APPROVALS	
D AND R	E OF M
HBK	G

E-NUMBER	
PROD. NO. 8558 WD	
DATE 1-12-68	
P.D. FILE NO. 1-A354.220A	
DRAWN W.T.	CHKD.
ENGD. R.B.B.	APPD.

TELETYPE CORPORATION

8558 WD

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TC 484 (3-68)