37 RECEIVE-ONLY (RO) TELETYPEWRITER SET

FOR SWITCHED NETWORK SERVICE

WIRING DIAGRAM AND CIRCUIT DESCRIPTIONS

CONTENTS PAGE

1. GENERAL

1.01 This section is issued to provide actual and schematic wiring diagrams and detailed circuit description information for the 37 Receive-Only (RO) Teletypewriter Set (Figure 1).

1.02 Notes are included on the diagrams and explain the symbols used or point out special conditions that should be observed.

1.03 Most wiring diagrams (WDs) and wiring diagram circuit descriptions (WD-CDs) in this section are a part of one or more wiring diagram packages (WDPs). A complete listing of these WDs and WD-CDs is found on the attached WDP control sheets, and a numerical summary is included in the wiring diagram index.

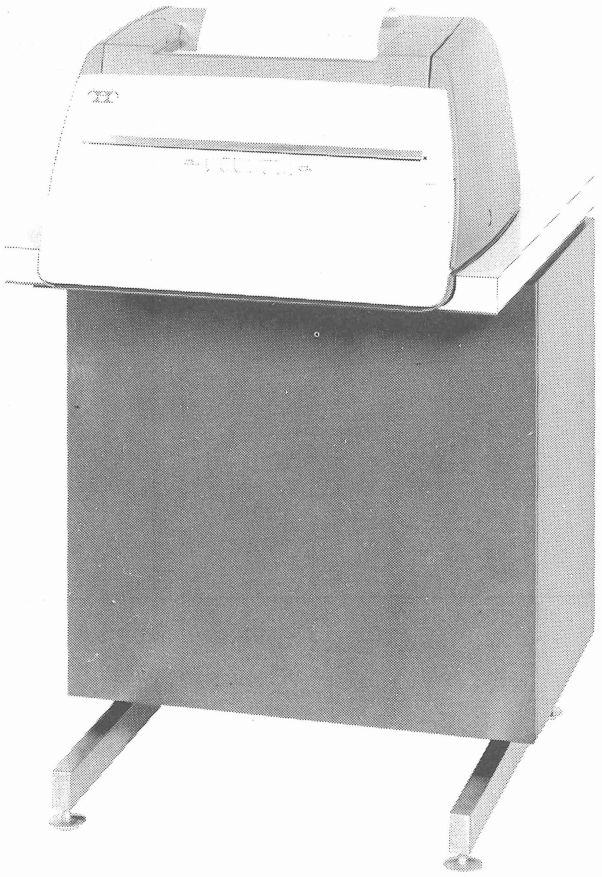


Figure 1 - 37 RO Teletypewriter Set

2. WIRING DIAGRAM INDEX (ATTACHMENTS)

DRAWING NUMBER	TITLE
Wiring Diagram Packages	
WDP0118	Basic Wiring Diagram Package for 37 RO, KSR, and ASR Sets. It includes the following WDs and WD-CD: 8352WD 8353WD 8358WD 8358WD-CD 8359WD 8360WD 8361WD 8365WD 303150

WIRING DIAGRAM INDEX (continued)

DRAWING NUMBER	TITLE
Wiring Diagram Packages	
WDP0125	Wiring Diagram Package for Circuit Card Set TP332546 (RO). It includes the following WDs and WD-CDs: 7856WD, 8370WD, 8370WD-CD, 8371WD, 8371WD-CD, 8377WD, 8377WD-CD, 8383WD, 8383WD-CD, 8387WD, 8387WD-CD, 8388WD, 8388WD-CD, 8389WD, 8389WD-CD, 8399WD, 8773WD, 8773WD-CD, 8774WD, 8774WD-CD, 8845WD, 303149, 322050, 322059, 322062, 322067, 322068, 322070, 322304, 322305

NO.	NOTES
1	THE FOLLOWING PROCEDURE SHOULD BE FOLLOWED WHEN INSTALLING CIRCUIT CARD OPTIONS: A. TURN POWER OFF B. LOCATE CARD POSITION GIVEN IN INSTALLATION PROCEDURE. C. CHECK POLARITY OF CARDS (NOTCHES) AGAINST POLARITY OF CARD CONNECTOR. (SMALL TAB IN CONNECTOR) D. INSTALL CARD.
2.	THE FOLLOWING PROCEDURE SHOULD BE FOLLOWED WHEN INSTALLING CABLE OPTIONS: A. TURN POWER OFF. B. IDENTIFY WIRES AND TERMINALS TO BE CONNECTED PER INSTALLATION PROCEDURE. C. INSTALL PUSH-ON TERMINAL CONTACTS DIRECTLY OVER ALLOTTED TERMINALS ON WIRING FIELD TERMINAL BOARD. D. DO NOT SHORT OR BEND TERMINALS ON WIRING FIELD TERMINAL BOARD.
3	IN REMOVING CIRCUIT CARD STRAP OPTIONS CARE SHOULD BE TAKEN TO AVOID A. DAMAGE TO ADJACENT COMPONENTS AND CIRCUIT BOARD. B. SHORTING REMAINING PORTION OF STRAP TO ADJACENT CIRCUITS. C. LITTERING CARD WITH CUT STRAPS.
4	IN ADDING CIRCUIT CARD STRAP OPTIONS TO PREVIOUSLY PROGRAMMED CARDS, A SOLDERING IRON NOT LARGER THAN 25 WATTS SHOULD BE USED. CARE SHOULD BE TAKEN TO AVOID DAMAGING ADJACENT COMPONENTS OR CIRCUIT BOARD.
5.	REFERENCES TO 8365WD, PRINTER, AND STUNT BOXES INDICATE THAT OPTION IS PART ELECTRICAL AND MECHANICAL.

SERVICE UNIT OPTION ARRANGEMENTS	DESCRIPTION	APPLICATION	ASSEMBLY AFFECTED	INSTALLATION PROCEDURE
X	CHARACTER COUNTER & CONTROL	ASR	322045	INSTALL PIGGY-BACK ON CARD ASSEMBLY 322045 POSITION XZ 301. 1. REMOVE STRAP "A" WHEN "NU-LINE" IS NOT IMPLEMENTED IN PRINTER.
			322055	INSTALL IN POSITION XZ 303. 1. PROGRAM P1-P24 FOR A COUNT OF 66 AS FOLLOWS, STRAP P3-P18, P6-P19, P8-P20, P10-P21, P12-P22, P13-P23, P2-P17 2. FOR OTHER COUNTS REFER TO 8380WD-CD.
X	10/11 UNIT CODE 150 WPM.	RO/KSR ASR	322067 322066	PROGRAM CIRCUIT CARD ASSEMBLY AFFECTED. POSITION XZ 105 AS FOLLOWS: 1. 10 UNIT DO NOT REMOVE STRAP "A".
X	HALF & FULL DUPLEX	KSR/ASR	322062	PROGRAM CIRCUIT CARD ASSEMBLY AFFECTED POSITION XZ 107 AS FOLLOWS: (FIELD MODIFICATION ONLY, CARD TO BE SHIPPED WITH ALL STRAPS. 1. DEDICATED HALF DUPLEX - REMOVE STRAPS "B" 2. DEDICATED FULL DUPLEX - REMOVE STRAPS "A" 3. LINE CONTROL OPERATION - REMOVE STRAPS "A B & C". 4. CHECK MECHANICAL PORTIONS OF STUNT BOX FOR APPROPRIATE CODES.
X	RECEIVER STATUS ALARM	KSR/ASR	322062	1. REMOVE STRAP "C"
X	MOTOR CONTROL (DATAPHONE) EOT AND ALARM DISCONNECT.	RO/KSR/ASR	322068	PROGRAM CIRCUIT CARD ASSEMBLY AFFECTED POSITION XZ 109 AS FOLLOWS: 1. REMOVE STRAPS "D, E, G, H, K, M, Y." DO NOT REMOVE STRAPS "A, B, C, F, L".
X	AUTOMATIC READER AND PUNCH CONTROL.	ASR	322079	1. INSTALL CIRCUIT CARD ASSEMBLY IN POSITION XZ 304. 2. PROGRAM CONTROL PANEL PER 8365 WD. 3. CHECK MECHANICAL PORTIONS OF STUNT BOX FOR APPROPRIATE CODES.
			322054	REMOVE STRAP "A" OF CIRCUIT CARD ASSEMBLY POSITION XZ 108 OF R-T ELECTRICAL SERVICE UNIT.
X	TWO COLOR RIBBON.	RO/KSR/ASR	322070	1. INSTALL CIRCUIT CARD ASSEMBLY AFFECTED IN POSITION XZ 405. 2. CHECK PRINTER AND STUNT BOX FOR APPROPRIATE MECHANISM & CODES.
X	ANSWER BACK	RO/KSR/ASR	327801	1. INSTALL THIS SELF CONTAINED ASSEMBLY IN POSITIONS XZ 310-XZ 315. 2. INSTALL CABLE ASSEMBLY 326575 AS FOLLOWS:
	INSTALLATION KIT. FOR THE YAB 802		336926	

WIRE COLOR	TB111 CONNECTION.
WHITE - BROWN	A 1
WHITE - RED	A 2
WHITE - ORANGE	A 3
WHITE - YELLOW	A 4
WHITE - GREEN	A 5
WHITE - BLUE	A 6
WHITE - PURPLE	A 7
WHITE - SLATE	A 8
WHITE - BLACK	A 11
GREEN - SLATE	J 3
BLUE - GREEN	H 3
ORANGE - GREEN	F 3
RED - BLUE	C 3
YELLOW	A13
GREEN	A14
BLACK	G 3
BLUE	A10
BROWN	D 3
BROWN	E 3

X	CONTROL CHARACTER INHIBIT	KSR/ASR	322059	INSTALL STRAP 327842 BETWEEN PINS 2 AND 7 ON CARD CONNECTOR XZ 102. INSTALL STRAP 327842 BETWEEN PIN B26 ON CARD CONNECTOR XZ102 AND PIN 2 ON CARD CONNECTOR XZ 305.

7856 WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	11-21-68	19778 R
2	3-17-69	96904
3	11-17-69	99693
4	4-14-70	94

DP

MODEL 37
OPTION
ANALYSIS CHART

APPROVALS

D AND R	E OF M

E-NUMBER

PROD. NO. 7856 WD

DATE 9-4-68

P.D. FILE NO. G-A354AA

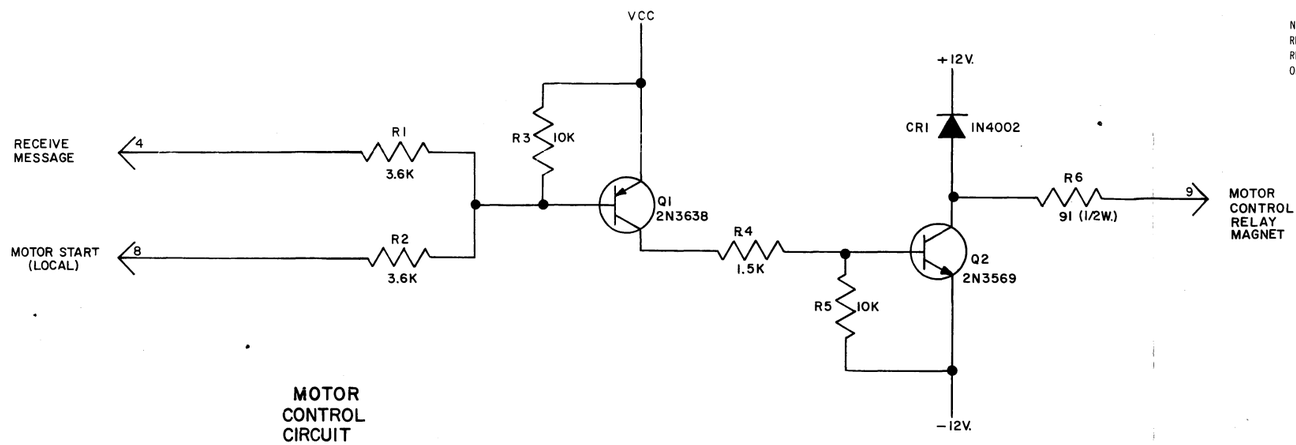
DRAWN W.P.B | CHKD.

ENGD. M.J.R. | APPD.

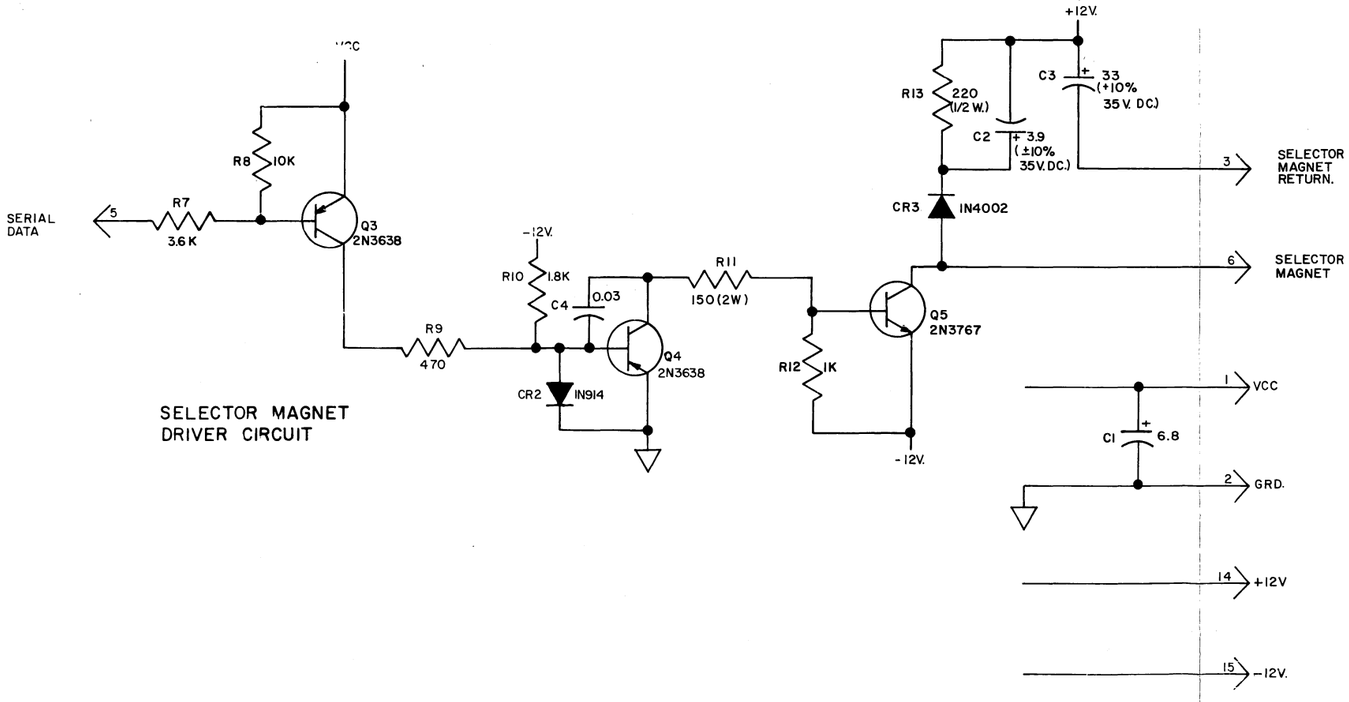
TELETYPE CORPORATION

7856 WD

NO.	NOTES
1.	ALL VOLTAGES DC. UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
5.	INDICATES FEMALE AND INDICATES MALE TERMINAL
6.	REFER TO 303149 FOR ASSEMBLY INFORMATION.
7.	S NUMBER: 61,428 S.
8	REFERENCE CIRCUIT DESCRIPTION: 8370WD-CD.
9.	INDICATES CIRCUIT GROUND.



MOTOR CONTROL CIRCUIT



SELECTOR MAGNET DRIVER CIRCUIT

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8370WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET - 1

SCHEMATIC WIRING DIAGRAM FOR RECEIVING DEVICE

APPROVALS	
D AND R	E OF M
	7

E-NUMBER

PROD. NO. 8370 WD.

DATE 2-29-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. | CHKD.

ENGD. C.A.Y. | APPD.

TELETYPE CORPORATION

8370WD

CIRCUIT DESCRIPTION OF THE RECEIVING DEVICE LOGIC CARD (ASSEMBLY NUMBER 303149)

TABLE OF CONTENTS

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF THE RECEIVING DEVICE LOGIC CARD (ASSEMBLY NUMBER 303149)

SECTION I

GENERAL TECHNICAL DATA

1. BASIC FUNCTION

1.1 The 303149 Receiving Device Logic card combines the function of a selector magnet driver and a motor control relay driver.

1.2 Selector Magnet Driver

The selector magnet driver sinks a steady state current of up to 600 ma DC on a MARK input and sinks zero current on a SPACE input. The MARK input is a logic one, and a SPACE input is a logical zero.

1.3 Motor Control

The motor control relay driver is capable of supplying a current of 40 to 60 ma to operate the motor control relay. The relay will be operated on a logic zero input and released on a logic one input.

2. GENERAL TECHNICAL DATA

2.1 Input-Output Data

2.1.1 The Receiving Device Logic card converts the integrated circuit logic levels to current levels appropriate for magnet operation.

A logic one is defined as a voltage level between 5.0 Volts and 6.6 Volts (usually a logic one approximates the integrated circuit supply voltage). A logic one draws no current from the input of the logic element.

Signal voltages between circuit ground potential and +0.5 Volts are considered logic zero.

2.2 Input-Output Characteristics

Motor Control

2.2.1 Receive Message/Motor Start Local (Pins 4 and 8)

These two inputs are connected together in a logical or configuration. A logic zero input will energize the associated motor control relay. Input impedance is 3.6K.

2.2.2 Motor Control Relay Magnet (Pin 9)

The associated motor control relay is connected to this output (typical coil resistance 430 ohms). The output impedance is 91 ohms in series with a -12 Volts. The relay driver output is capable of supplying up to 60 ma of current. Relay magnet drop-out is diode suppressed.

Selector Magnet Driver

2.2.3 Send Data (Pin 5)

Under the control of set logic this input is supplied with MARK and SPACE signals corresponding to received data. A logic one signal (MARK) will cause the selector magnet to be energized. A logic zero signal (SPACE) will de-energize the selector magnet. Input and impedance is 3.6K.

2.2.4 Selector Magnet (Pin 6)

The negative end of the selector magnet is connected to this output which will establish a discharge path through a Diode coupled resistor capacitor network. Typical dropout time is approximately 2.50 milliseconds.

2.2.5 Selector Magnet Return (Pin 3)

The positive end of the selector magnet is connected to this output. In series with the selector-coil is a parallel resistor capacitor network which permits maximum current through the coil during SPACE to MARK transitions. Typical MARK hold current is approximately 600 milliamperes. Nominal rise time is 2.25 milliseconds. Typical load supplied is 3.5 ohms 20 millihenries inductance.

2.3 Mechanical Requirements

The motor control amplifier and the selector magnet driver are mounted on a 15-pin circuit board.

2.4 Power Requirements

D.C. Supply	Current Required
+5.0V to +5.50V (+5.25V Nom.)	0 to 20 ma
+11.65 to +13.75V (+12.5V Nom.)	0 to 660 ma
-11.13V to -13.88V (-12.5V Nom.)	0 to 660 ma

2.5 Operating Temperature Range

0°C to 70°C (in free air)

2.6 Storage Temperature Range

-40°C to 70°C

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Schematic Drawing - 8370 WD.

1.2 Assembly Drawing - 303149.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 Selector Magnet Driver

2.1.1 The selector magnet driver circuit is a three stage amplifier, designed to operate full on or off without intermediate levels. The input characteristics are matched to the output of currents sinking DTL integrated circuit elements. The output circuit is matched to the characteristics of the 312936 Selector Magnet Assembly.

2.1.2 A logic one signal input, (See Section I-2.1), will turn the output on, picking up the selector magnet armature. The logic one signal turns off Q3, allowing Q4 and Q5 to be turned on. With Q5 turned on, C3 will be charged through the load impedance to give a high initial current. As C3 becomes charged, load current will be limited by the external 50 ohm, 50 watt resistor connected across C3.

2.1.3 With a logic zero signal on the input, (see Section I-2.1), Q3 will be turned on, driving the base of Q4 positive, turning off Q4 and Q5. The positive voltage on the base of Q4 is limited by ground clamp Diode CR2. With Q5 turned off, the load inductance and C3 will discharge through steering Diode CR3, and the discharge network C2, R13. The impedance values of the output circuit are chosen to proved equal selector magnet armature pickup and drop-out times. The characteristics of the (loaded) output circuit will determine the maximum signalling rate. The values chosen will give proper operation with a nominal pulse length of 6 ms or more.

2.2 Motor Control Relay Driver

2.2.1 The motor control relay drive is a two-stage amplifier which is designed to operate full ON or OFF without intermediate levels. This circuit is designed to drive an external motor start relay. Inputs to the motor control relay drive circuit are on Pins 4 and 8. The inputs are connected in a logical OR configuration each having an input resistance of 3.6K. With logic zero, (see Section I-2.1), applied to either input, Q1 is switched ON. This switches Q2 ON, energizing the relay. With logic one applied at both inputs Q1 and Q2 are switched OFF. When Q2 is switched OFF, any positive voltage transient developed by the inductive load will be clamped to the positive supply voltage by CR1.

NO.	NOTES
1.	ALL VOLTAGES DC, UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
4.	INDICATES FEMALE CONNECTOR. INDICATES MALE CONNECTOR. INDICATES CIRCUIT GROUND.
5.	ML B I ROW COLUMN INTEGRATED CIRCUIT
6.	ASSOCIATED ASSEMBLY: 322059.
7.	S-NUMBER: 61658S
8.	REFERENCE CIRCUIT DESCRIPTION 8371WD-CD.
9.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER THE GATE IS USE AS AN INVERTER.
10.	LOGIC NEGATION: A SMALL CIRCLE JOIN TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
11.	THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE +6V. AND 0V, RESPECTIVELY.
12.	VCC. IS PROVIDED TO THE INTEGRATED CIRCUIT PACKAGE ON PIN 14, AND GROUND ON PIN 7. THIS APPLIES TO ALL PACKAGES EXCEPT MLBI.
13.	REFER TO 8399WD FOR TRUTH TABLES.
14.	ABBREVIATIONS: ST - START. SP - STOP. TCL - TIMER CONTROL LATCH. CSL - CHARACTER SAMPLE LATCH. CCL - CONTROL CHARACTER LATCH. OBL - OUTPUT BLIND LATCH. ECL - ESCAPE CHARACTER LATCH. TCS - TIMER CONTROL SET. TC - TAKE CHARACTER. PNC - PRESENT NEXT CHARACTER. FX32 - FREQUENCY X 32 RS(NOT - REGISTER SAMPLE NOT. CP - CLOCK PULSE. SCS - SHIFT CONTROL SAMPLE. CC(NOT) - CONTROL CHARACTER NOT.

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8371 WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	3-10-69	19887 R

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 1

SCHEMATIC
WIRING DIAGRAM
FOR
DISTRIBUTOR

APPROVALS

D AND R	E OF M
LDm	~

E-NUMBER

PROD. NO. 8371 WD.

DATE 4-24-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. | CHKD. RV

ENGD. A.B. | APPD. /

TELETYPE
CORPORATION

8371 WD

1

TC 434 (2-69)

SEE SHEET 1 FOR NOTES.

8371 WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	3-10-69	19887 R

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

TIMER

F X 32

MLA2 FF

MLA2 FF

MLA1 FF

MLA1 FF

MLE1 FF

SCS

MLF1

MLF1

MLD1

MLF1

MLH2

CSL

MLH2

MLH2

MLH2

R S.(NOT)

CC.(NOT)

MLG3

MLH3

CCL

MLH3

MLG3

MLF2

OBL

R2 100

MLF2

MLF2

TC

TCS

PNC

MLG3

MLG2

MLG2

TCL

MLG1

MLG2

C13 0.003

MLG1

MLHI

ECL

MLHI

MLHI

C1 0.003

R1 100

C2 0.003

MLB1

MLB1

MLC1

MLC1

MLD1

MLF2

MLF3

MLF3

10-11 BIT CODE (GRD FOR IO)

GRD

+6V.

C11 68

CP

MLA3 FF SP

MLA3 FF 8

ML B2 FF 7

ML B2 FF 6

MLC2 FF 5

MLC2 FF 4

MLD2 FF 3

MLD2 FF 2

MLE2 FF 1

MLE2 FF ST

MLE1 FF LINE

BLIND

MLB3

MLB3

MLB3

MLB3

MLE3

MLE3

MLE3

MLE3

MLF3

C10 0.1 R10 100

C9 0.1 R9 100

C8 0.1 R8 100

C7 0.1 R7 100

C6 0.1 R6 100

C5 0.1 R5 100

C4 0.1 R4 100

C3 0.1 R3 100

C12 0.003

DATA INPUT 8

DATA INPUT 7

DATA INPUT 6

DATA INPUT 5

DATA INPUT 4

DATA INPUT 3

DATA INPUT 2

DATA INPUT 1

SIGNAL OUTPUT

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D. SHEET 2

SCHEMATIC WIRING DIAGRAM FOR DISTRIBUTOR.

APPROVALS	
D AND R	E OF M
LDm	~

E-NUMBER

PROD. NO. 8371 WD

DATE 4-24-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. CHKD

ENGD. A.B. APPD.

TELETYPE CORPORATION

8371 WD

1

TC 434 (2-63)

CIRCUIT DESCRIPTION OF THE ELECTRONIC TRANSMITTING DISTRIBUTOR (ASSEMBLY NUMBER 322059)

TABLE OF CONTENTS

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF THE ELECTRONIC TRANSMITTING DISTRIBUTOR (ASSEMBLY NUMBER 322059)

SECTION I

GENERAL TECHNICAL DATA

1. BASIC FUNCTION

1.1 The 322059 Circuit Card Assembly is an Electronic Transmitting Distributor with Control Character Detection. The device converts parallel input signals to serial output signals of either 10 or 11 unit code. The parallel input consists of eight information levels (bits). The serial output consists of a start bit, eight information bits, and one or two stop bits. The telegraphic speed is determined by an external oscillator.

1.2 In addition to the basic data transmitting function of the assembly, several other functions are provided. These functions are:

1.2.1 Responds to a character delete signal (blind), and inhibits transmission of a character.

1.2.2 Recognizes ASCII control characters (6th and 7th level spacing), except ESC and electronically delays the transmission of the next character. The delay interval is a fraction more than a character length, depending upon the character unit code.

1.2.3 Recognizes ASCII control character ESC (11011000) and electronically adds a one character delay after the character following the ESC character.

1.2.4 Provides an output signal which indicates that a character is stored in the register and can be decoded.

1.2.5 Provides an output signal which is used to sample conditions prior to the parallel data input sample.

1.2.6 Provides an output signal which indicates that another character may be distributed.

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

The inputs to the assembly are all nand type integrated Diode Transistor Logic (DTL) inputs. Each DTL input is approximately a 1.4 ma load to the device sinking current from it. At no time should any of these inputs be more positive than 8 volts or more negative than -.7 volts.

2.1.1 Take Character (TC) (Pin 10)

The TC input controls the start of the distribution cycle. When the input is in the 0-state, less than 0.5V, it indicates that a character is available for distribution. Once distribution has commenced, this input will have no further effect until the end of the cycle. This input must be low for at least .25 of a bit before it will be recognized as a legitimate start signal. The device driving the input must be capable of sinking one DTL load.

2.1.2 Data Input (Pins 18, 19, 20, 21, 25, 26, 27, 28)

The device driving these inputs must be capable of sinking one DTL load. These inputs will only have effect on the distributor from .5 to .75 of a bit after the TC input first reverts to the low state. At all other times these inputs will not affect the distributor.

2.1.3 Blind Input (Pin 4)

A momentary low on this lead blinds the line to the distribution of the following character. The device driving this input must be capable of sinking four DTL loads. This input should never be allowed to revert to the 0-state except when the PNC output is low. Otherwise, the line would be blinded somewhere in the middle of a character, resulting in an errored character being transmitted. The low on the blind input must be removed before the end of the blinded character to allow the distributor to reset the Output Blind Latch.

2.1.4 Control Character Latch (CC(NOT)Inhibit)(Pin 7)

This input is grounded to disable the control character blind feature (See Paragraph 1.2.2). The device driving this input should be capable of sinking three DTL loads.

2.1.5 Register Condition (TCS)

This input may be grounded in order to clear the register. This may be a requirement in some applications where at times certain characters will not be transmitted. The device driving this input should be capable of sinking three DTL loads.

2.1.6 F X 32 (Pin 35)

This input is from an external oscillator. The frequency of the oscillator must be 32 times the desired bit-rate. The device driving this input must be capable of sinking two DTL loads.

2.1.7 10-11 Unit Option (Pin 11)

This input is grounded when the distributor is operating with a 10 unit character code. It is opened or high for 11 unit operation. The device driving this input must be capable of sinking one load.

2.2 Output Characteristics

The outputs from this assembly are all nand type Diode Transistor Logic (DTL) outputs. The outputs will be rated by the number of DTL loads it can sink. Each DTL load is approximately 1.4 ma.

2.2.1 Present Next Character (PNC) (Pin 9)

This circuit is capable of driving eight DTL loads. When the distributor is idle, this output will be 0-state (approximately .3V).

2.2.1 (Continued)

When this output is low, a character may be presented for distribution. It will revert to the 1-state (approximately Vcc) at the beginning of a distributor cycle. It will remain in the 1-state until the character has been distributed, at which time it will revert again to the 0-state.

2.2.2 Serial Data Output (Pin 12)

A mark signal is represented by a 1-state at this output and a space signal by the 0-state. This output sinks up to eight DTL loads.

2.2.3 Control Character Recognition [CC (NOT)] (Pin 7)

This output is the same as the Control Character Latch Inhibit input. This output will change from the 0-state to the 1-state when a control character is recognized, and will remain in the 1-state for a time duration of 1.1 characters. It is capable of sinking six DTL loads.

2.2.4 Clock Pulse (CP) (Pin 3)

The clock pulse output is a timing output. This output reverts to the one state for approximately .12 of a bit, occuring at the trailing edge of each transmitted bit.

2.2.5 Register Sample [RS (NOT)] (Pin 6)

The Register Sample output is approximately .12 bits in duration occuring between .75 to .87 of a bit following the start of the distributor. When this output reverts from its normally low state to the 1-state, it indicates that a character is in storage, and the parallel data outputs of the register may now be sampled. This output is capable of sinking current from seven additional DTL loads.

2.2.6 Parallel Data Outputs (Pins 14, 17, 29, 31)

When these parallel outputs are in the 1-state it indicates that a mark is stored in the particular position that the given lead is monitoring. These outputs are capable of sinking seven DTL loads.

2.2.7 Parallel Data Outputs (Pins 13, 15, 16, 22, 23, 24, 30, 32)

When these parallel outputs are in the 1-state it indicates that a space is stored in the particular position that the lead is monitoring. Pins 13, 15, 16, 22, 23, and 32 are capable of sinking six DTL loads. Pins 24 and 30 are capable of sinking five DTL loads.

2.2.8 Shift Control Sample (SCS) (Pin 5)

The output of SCS reverts to the 0-state from .25 to .5 of a bit after the start of the distributor. It is a timing signal occuring prior to

2.2.8 (Continued)

the character sample, and may be used to set up characters in external logic prior to the character sample by the distributor.

2.2.9 Stop Output (SP) (Pins 33, 34)

Pin 33 is in the 1-state when a stop bit is set in the SP Flip-Flop. This is a timing signal which may be used by external logic to identify that a character is being distributed. Pin 33 is capable of sinking four DTL loads Pin 34 is capable of sinking five external DTL loads.

2.3 Size

The distributor is a 5-3/4 inch by 4-1/4 inch circuit card which mates with a standard 36 pin circuit card connector.

2.4 Options Available

2.4.1 The distributor may be changed from eleven unit code to ten unit code by grounding Pin 10.

2.4.2 Another option is the electronic insertion of an idle time, one character in duration, following each ASCII control character except control character ESC. This feature may be removed by grounding Pin 7. Grounding Pin 7 also removes the electronic insertion of a character interval for the character following the control character ESC.

2.5 Miscellaneous Requirements

2.5.1 Power Supply Requirement

VDC	I (ma)
+5V to +6.6V	520 ma (max)

2.5.2 Operating Temperature Range

0°C to 70°C (free air)

2.5.3 Storage Temperature Range

-40°C to +70°C

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly drawing 322059 (MC059) and schematic drawing 8371 WD.

1.2 Logic symbols and truth table 8399 WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 General

2.1 Refer to the timing diagram, flow chart and the schematic 8371 WD to aid in understanding the following discussion.

The flow chart should be used as an outline. When two lines enter a symbol, it is implied that either input causes the function in the symbol to be performed. It is not intended that any of the symbols be construed to represent logic functions. The flow chart is intended to relate circuit operation with respect to time.

2.2 Starting Function

Assume that the distributor is idle, i.e., no character is being distributed. In this state the distributor issues a present next character command (PNC in O-state) which indicates to external logic that a character may be presented for distribution. The command to begin the distribution cycle is presented on the take character lead. This command (TC in O-state) releases and controls the timer through MLG3-12.

The TC must remain ON for at least .25 of a bit, after which time the timer is locked on by the timer control latch, TCL, for one distribution cycle. Should TC turn off anytime prior to .25 bit, the timer will be recycled to the O-count. This time period provides integration to reject noise pulses at the TC input.

When the time out reaches .25 of a bit, two gates MLF1-6 and MLF1-12 change to the O-state. MLF1-6 provides the shift-control sample (SCS) signal at Pin 5, while MLF1-12 sets the timer control latch (TCL). An output from TCL locks the timer on, committing the distributor to a complete character cycle. (As a condition, the take character input must remain on for .75 of a bit to assure that a character is correctly entered into the shift register.)

2.3 Preliminary Events

The shift-control signal (SCS) started at .25 of a bit remains on until .5 bit. This signal is used by keyboard logic to perform a controlling function.

At .5 of a bit gate MLD1-6 changes to the O-state. This condition causes the character sample latch to set and opens the character input gates MLB3 and MLE3 to accept data signals. A 1-state on any data input level sets a MARK into the corresponding register flip-flop. The sample period lasts for one quarter bit (until .75 of a bit after TC) at which time MLD1 reverts back to the one-state. If TC is removed prematurely i.e., before .75 bit the

2.3 (Continued)

character sample period will be terminated early or may not occur at all. TC may be removed after .75 bit.

Immediately following the character sample period the register sample (RS) pulse is developed. This is a positive going output which appears on Pin 6. This output, lasting .12 bits, indicates to external logic that a character has been stored in the register and may now be sampled. Internally this signal enables the control character detected gate MLG3-6, whose functions will be further discussed in the control character section.

At approximately .87 of a bit, the clock pulse changes to the 1-state, priming the data flip-flops. At exactly 1-bit time (.13 bits later) the clock pulse reverts to the 0-state. At this time each data bit stored in the distributor is shifted one position. Additional clock pulses shift the data to the LINE flip-flop, which becomes the output signal. This continues for nine additional clock pulses, (10 for an 11-unit code), at which time the register will have been cleared (all flip-flops in the space condition). The distribution cycle is now completed.

2.4 Serializing Function

The serializing function is performed by the shift register. It consists of eleven clocked flip-flops, labeled on the schematic as Stop (SP), Start (ST), Line (LINE) and Data Levels 1 through 8. Information is transferred into the shift register on a parallel basis. When the SD input of any flip-flop reverts to the 0-state, a mark is set in that position of the distributor. Positions SP, ST and LINE are set internally. The elements are cascaded in such a manner that a positive pulse applied to the CP input of the flip-flop will result in each flip-flop assuming the state of the preceding flip-flop when the pulse is removed. Therefore, the shift register performs the function of serializing parallel input signals.

When the distributor is idle, TCL is used to hold the register in the no character stored state, that is, data positions 1 through 8 and ST are held spacing while SB and LINE are held marking. The result is that a character cannot be set in the register until TCL is set, which occurs .25 of a bit after TC. Data bits are read into the register during the character sample period, .5 to .75 of a bit after TC. A 1-state on any data input during the sample period sets a mark into the corresponding data flip-flop. Likewise a 0-state on any data input for the duration of the sample period holds the corresponding data flip-flop in its cleared state (corresponding data flip-flop remains spacing). When the character sample period has passed, the data input leads have no further effect on the distributor.

One bit time after TC, the first clock pulse occurs. Each data bit in the register is shifted one position. After nine additional clock pulses, (10 for 11 unit code) the entire register will have been cleared to the spacing condition, that is, a space stored in each flip-flop. Register condition gate, MLD1-8, then reverts to the 0-state. MLD1-8 resets the timer control latch, TCL, and the output blind latch, OBL, if it had been previously set. TCL clamps the register and sets a MARK in the SB flip-flop which in turn causes the present next character, PNC, command to be issued. A new cycle may now begin.

2.5 Control Character Operation

Another function of the distributor is to insert a marking interval of approximately one character length after the transmission of each control character. This time period is needed by the typing unit to detect, respond, or perform logic associated with certain control characters prior to the transmission of the next character. This feature may be inhibited by grounding the CC (NOT) lead, Pin 7.

When a control character has been entered in the distributor, its presence is recognized by the control character recognition gate, MLG3-6. This gate has inputs to monitor the registers sixth and seventh level for a spacing condition and a lead to monitor the register sample time. After the data has been loaded into the register (.5 to .75 bit after TC), the register sample lead, RS, reverts to the one-state (from .75 to .87 bit after TC). Therefore, for all control characters the control character recognition gate sets the control character latch, CCL.

The control character is then transmitted as any other character. After the control character has cleared the register, the register condition gate MLD1-8 resets the timer control latch, TCL. At this time the output blind latch, OBL, is set via gate MLG3-8, for all control characters except ESCAPE (ESC), which will be discussed later. The output blind latch keeps the signal output at Pin 12 in a MARK state. The control character latch, set previously, inhibits the present next character (PNC), output and provides the input required to cycle the distributor for another character interval. After the register is empty (the stop bit has moved through the register), the TCL and OBL are reset by the register condition gate MLD1-8.

When operating in 10 unit code the detection of a control character causes the distributor to shift into the 11 unit code for the control and delay character. This adds two bit intervals to the control character-delay character length. When in 10 or 11 unit code, an additional interval, approximately .87 bit, is provided by gate MLF2-3. These added time intervals are necessary to insure that all typing unit responses are completed before another character is transmitted.

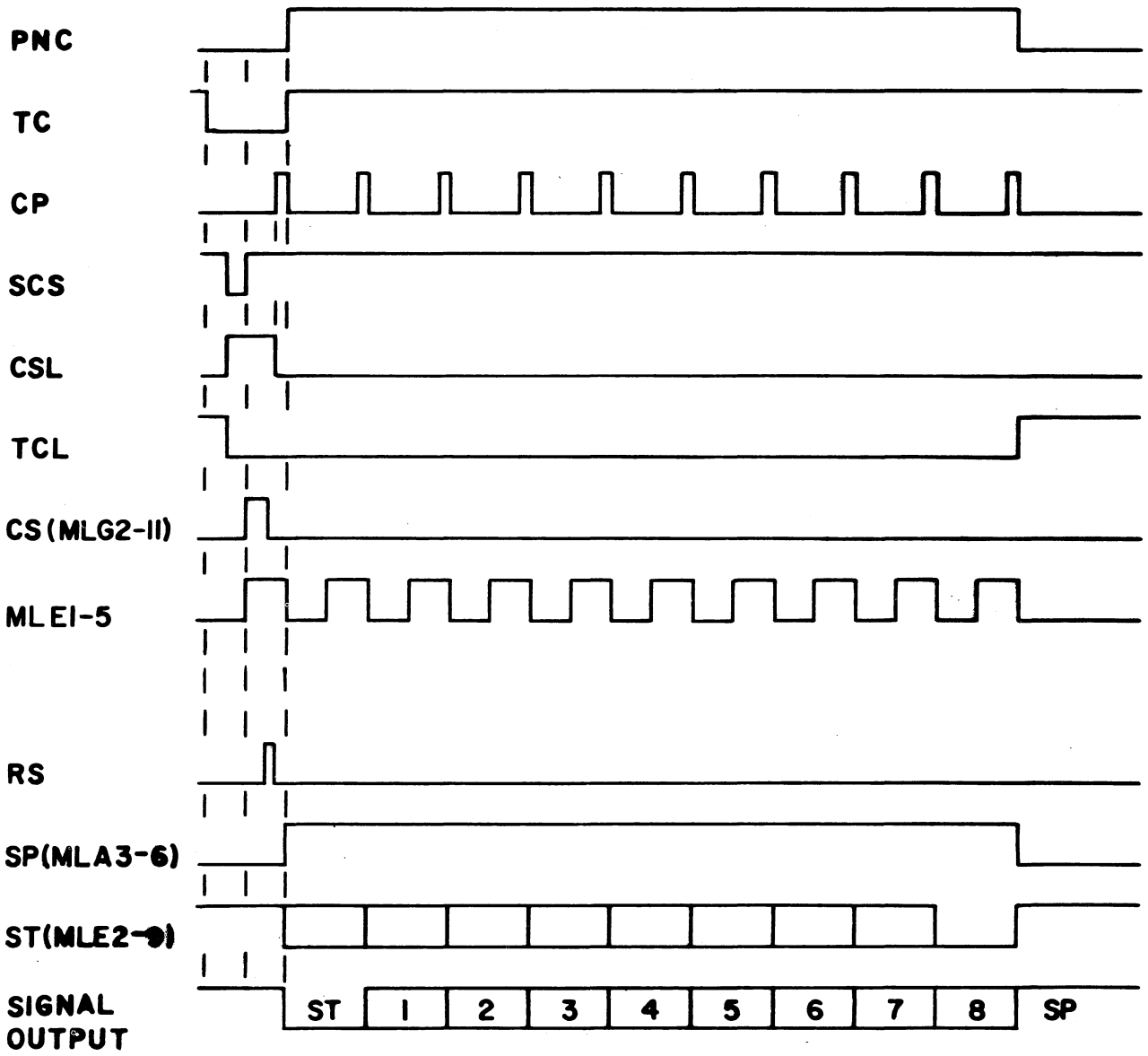
2.6 ESCAPE Character Operation

Another function of the distributor is to insert a marking interval of approximately one character length after the transmission of the character following the control character ESC. No delay is provided after the ESC character. The control character ESCAPE in itself performs no function in the typing unit. The character following ESCAPE is used by the typing unit to perform a function. The delay, therefore, is added after this two character ESCAPE sequence to allow the typing unit to complete its control function before transmission of the next character. This feature may also be inhibited by grounding the CC (NOT) lead, Pin 7.

2.6 (Continued)

An escape character is detected in the escape recognition gate MLC1-6 and MLC1-8 which in turn sets the escape character latch, ECL. ECL inhibits the operation of the output blind latch, OBL, and allows the present next character, PNC, to be issued immediately after the control character ESCAPE has been transmitted. The control character latch CCL, however, remains set. A character other than ESCAPE resets ECL which in turn removes the inhibit from gate MLC3-8. The distributor now operates as if a control character had been detected.

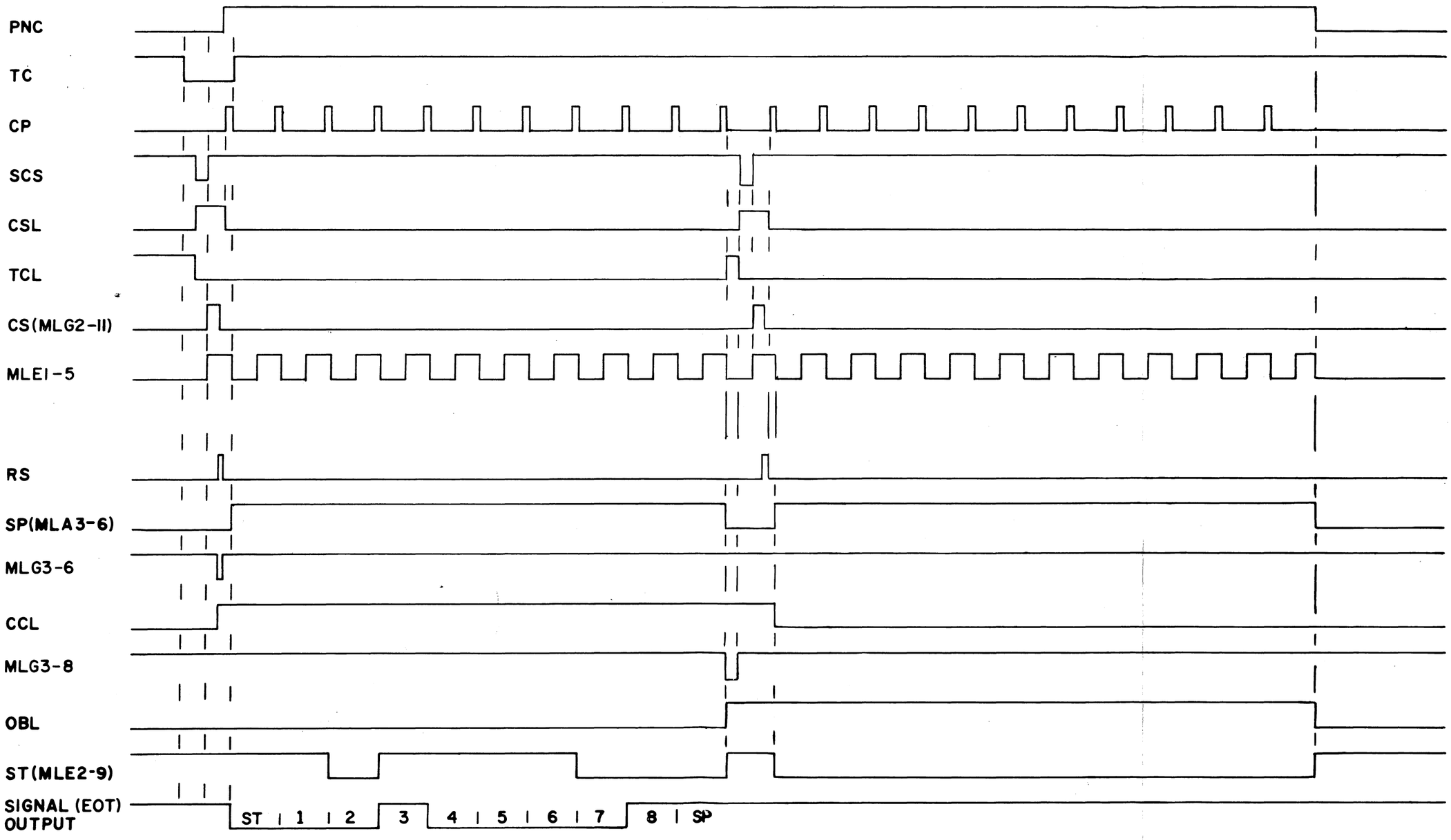
DISTRIBUTOR TIMING DIAGRAM



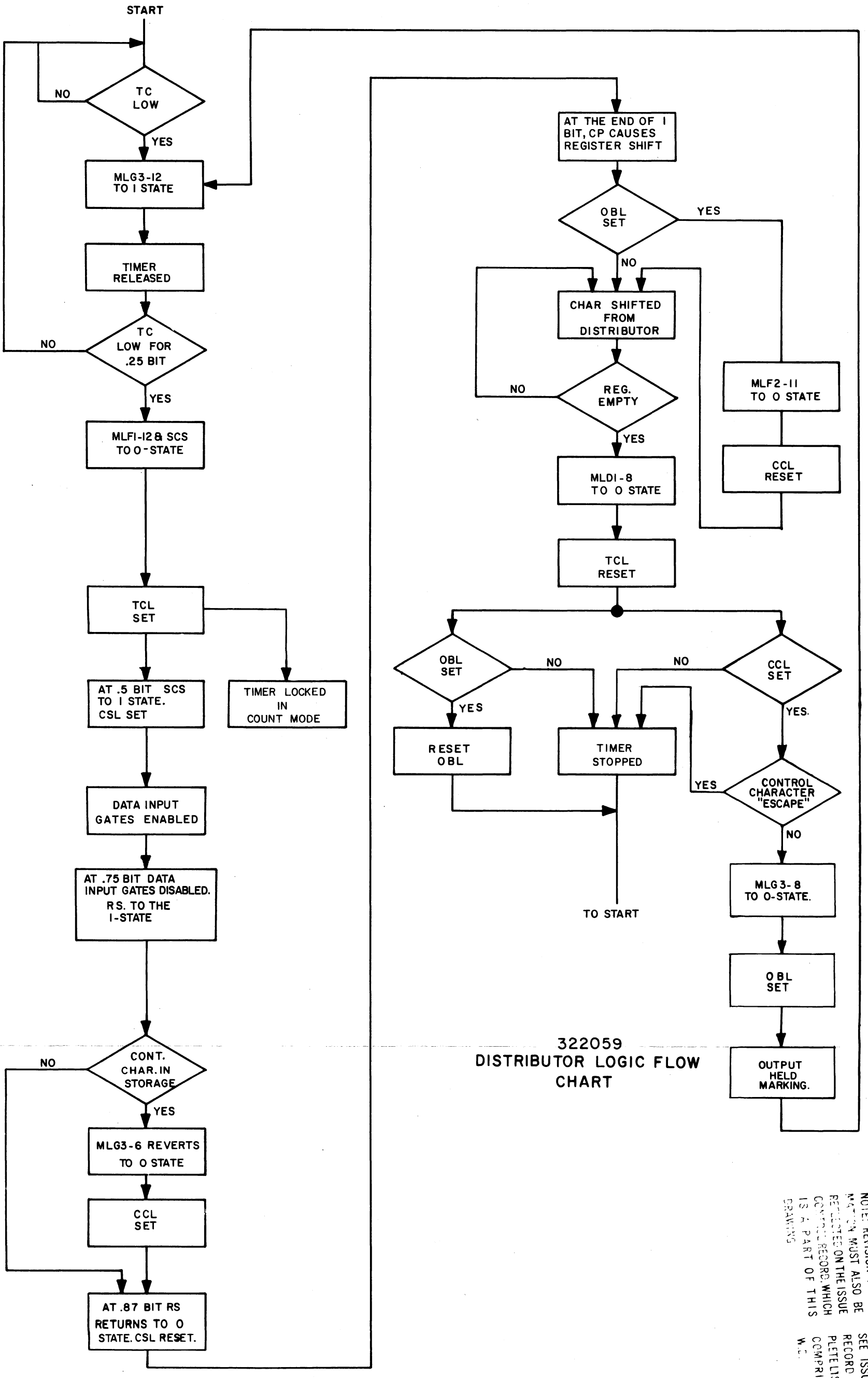
NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

DISTRIBUTOR TIMING DIAGRAM FOR CONTROL CHARACTERS (ESCAPE EXCLUDED)



NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

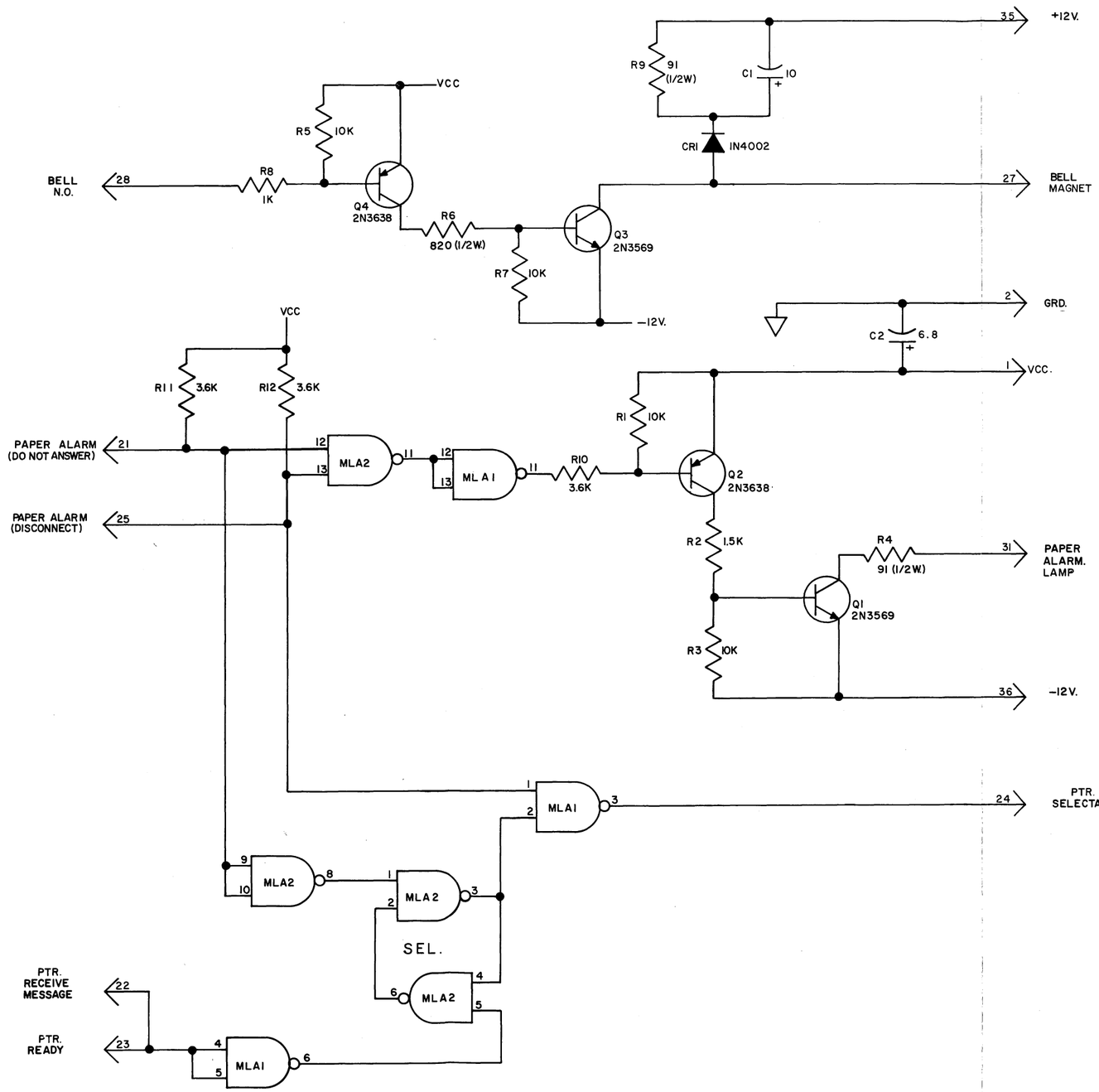


322059
DISTRIBUTOR LOGIC FLOW CHART

NOTE: REVISION INFORMATION MUST ALSO BE RECORDED ON THE ISSUE CONTROL RECORD WHICH IS A PART OF THIS DRAWING

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

NO.	NOTES.
1.	ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTORS 1/4 WATT, AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
4.	INDICATES FEMALE AND INDICATES MALE TERMINAL
5.	REFER TO 322050 FOR ASSEMBLY INFORMATION.
6.	S NUMBER 61,519S.
7.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD: ML D 2 — ROW, COLUMN, INTEGRATED CIRCUIT.
8.	THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC AND OV., RESPECTIVELY.
9.	LOGIC NEGATION - A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
10.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER, THE GATE IS USED AS AN INVERTER.
11.	VCC IS PROVIDED TO THE INTEGRATED CIRCUIT PACKAGE ON PIN 14 AND GROUND ON PIN 7, THIS APPLIES TO ALL PACKAGES.
12.	SEE 8399WD FOR TRUTH TABLES.
13.	REFERENCE CIRCUIT DESCRIPTION 8377WD-CD.
14.	ABBREVIATIONS USED: SEL. - SELECTABLE ENABLE LATCH.
15.	INDICATES CIRCUIT GROUND



NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8377WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R
2	11-15-69	99880

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

WDP

SHEET-1

SCHEMATIC WIRING DIAGRAM FOR ALARMS AND CONTROL

APPROVALS

D AND R	E OF M

E-NUMBER

PROD. NO. 8377WD

DATE 3-1-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B.	CHKD.
ENGD. R.E.L.	APPD.

TELETYPE CORPORATION

8377WD

CIRCUIT DESCRIPTION OF THE ALARMS AND CONTROLS CARD (ASSEMBLY NUMBER 322050)

TABLE OF CONTENTS

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF THE ALARMS AND CONTROLS CARD (ASSEMBLY NUMBER 322050)

SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The 322050 Alarm and Control device logic card performs the function of a bell driver and logically controlled paper alarm.

1.2 The bell driver sinks a nominal current of 230 ma on a logic zero input and sinks zero current on a logic one input. The bell serves as an attention getting device.

1.3 The logically controlled paper alarm sinks a current of 30 ma (nominal) to operate the "PAPER ALARM" panel indicator lamp. The lamp will be turned ON on a logic zero input and turned OFF on a logic one input. The paper alarm signifies a "DO NOT ANSWER" or "DISCONNECT" condition.

1.4 Additional Features

1.4.1 The terminal remains "SELECTABLE", when a "DO NOT ANSWER" condition occurs and becomes "NON-SELECTABLE" after message transmission is completed.

1.4.2 A "DISCONNECT" condition renders the set "NON-SELECTABLE" by means of a direct disconnect line.

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

A logic one is defined as a voltage level between +5.0 volts and +6.6 volts (Usually a logic one approximately equals the integrated circuit supply voltage.) or an open circuit. In either case, a logic one draws no current from the input of the logic element.

Signal voltages between circuit ground potential and +0.5 volts are considered logic zero. Logic currents that flow into the signal source are a function of the element driven, source impedance, supply voltage, and the value of pull up resistor used, if any. Refer to manufacturers specifications for loading information.

2.1.1 Bell In (Pin 28)

This input is high during normal set operation and high and low during an alarm condition (pulse width approximately 30 milliseconds).

2.1.2 Paper Alarm (DO NOT ANSWER) (Pin 21)

This input is high during normal set operation and low during a "DO NOT ANSWER" alarm condition. The driving source must be capable of sinking 3 DTL loads. (1 DTL load = 1.4 ma)

2.1.3 Paper Alarm (DISCONNECT) (Pin 25)

This input is high during normal set operation and low during a "DISCONNECT" alarm condition . The driving source must be capable of sinking 3 DTL loads.

2.1.4 PTR Receive Message-PTR Ready (Pins 22, 23)

This input is low while the printer motor is in operation and high at all other times. The driving source must be capable of sinking 1 DTL load.

2.1.5 Paper Alarm Lamp (Pin 31)

The Paper Alarm Lamp is turned on by a zero output from the inverter MIA1 Pin 11, and indicates to the operator that the printer is in a paper alarm condition.

2.1.6 Printer Selectable (Pin 24)

This output is normally low, but will be high when the printer is not selectable (paper alarm). The paper alarm (DO NOT ANSWER) does not immediately affect Printer Selectable, whereas the Paper Alarm (DISCONNECT) immediately causes Printer Selectable to go high (non-selectable). This output is capable of driving 8 DTL loads.

2.1.7 Bell Driver

A logic zero applied to the input of the bell driver (Pin 28), turns the output transistor on and rings the bell. A logic one turns the output transistor off and no current flows through the bell winding.

2.2 Mechanical Characteristics

The integrated circuit logic and driver amplifiers are mounted on a printed circuit card which is inserted in a conventional 36-pin edge card connector.

2.3 Power Requirements

Vcc (DC)	Current Maximum
+5.0V to +6.6V (+5.25V Nom.)	85 ma
+11.65 to +13.75V (+12.5V Nom.)	275 ma
-11.88V to -13.13V (-12.5V Nom.)	275 ma

2.4 Temperature Range

The ambient temperature range for operation is from 0°C to 70°C in free air. Non-operating storage temperature is from -40°C to 70°C.

WDP

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly and Schematic drawing 322050, (MC050) and 8377 WD, respectively.

1.2 Logic Symbols and Truth Tables Per 8399 WD.

1.3 Integrated circuit information per manufacturers specifications.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 Bell Driver

2.1.1 The bell driver circuit is a two stage amplifier, designed to operate full ON or OFF without intermediate levels.

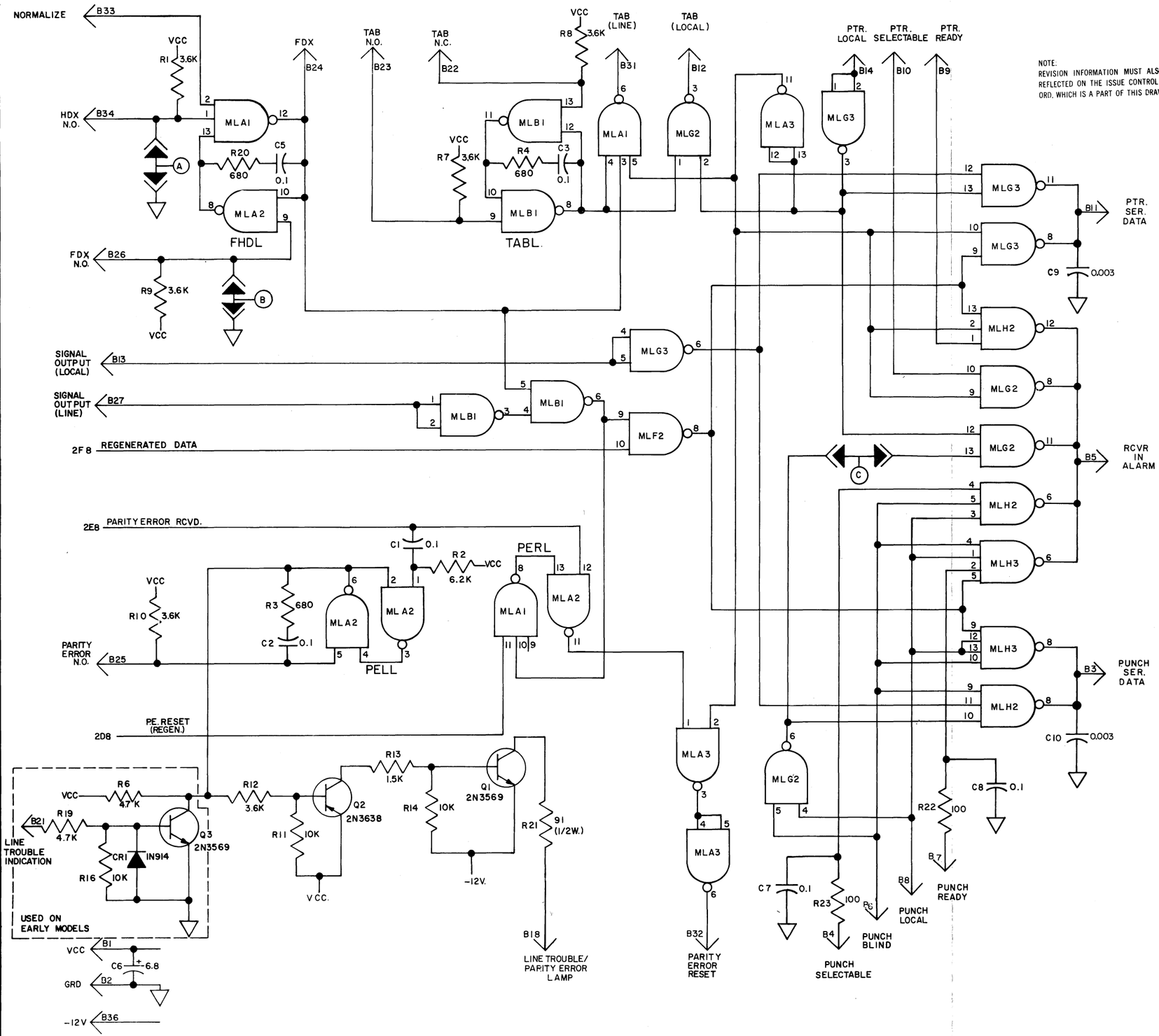
A logic zero applied to the input of C4 results in a positive going pulse at the base of Q3. As a result, Q3 is turned ON and approximately 24 volts DC is applied to the bell winding. The bell (collector current of Q3) current rises exponentially to a nominal value of 230 ma. The rise time of the current waveform is determined by the inductance and series resistance of the bell winding.

A logic one applied to the input of C4 causes Q4 collector current to decrease to zero. As a result, a negative going pulse appears at the base of Q3. Q3 is now in the "OFF" state. The bell winding discharges its energy through CR_1 and the discharge network R_9, C_1. The pickup and dropout times are not adjustable and for a given bell are a function of the charge path, discharge network, and winding inductance which determine the electrical time constant.

2.2 Paper Alarm

2.2.1 The "Paper Alarm (DISCONNECT)" is used where immediate alarm action is required and is a logic zero during the alarm condition. The alarm signal goes through two stages of inversion and turns ON the paper alarm lamp. The alarm signal also appears on MLA1 Pin 1 and immediately switches the output high, causing "Printer Selectable" Pin 24 to go to the non-selectable state (high). The "Paper Alarm (DO NOT ANSWER)" is used to disable the "Printer Selectable" (Pin 24) whenever Receive Message (Pin 22) is high. Thus, if the alarm occurs during a message (Printer Receive Message in zero state), the alarm lamp will turn on, but the Printer Selectable will remain low until Printer Receive Message goes high at the end of the message. This sequence is controlled by the Selectable Enable Latch (SEL) which is gated by Printer Receive Message MLA1 Pin 6 and will transfer the Paper Alarm indication (zero), from MLA2 Pins 9 and 10 to MLA1 Pin 2, whenever Printer Receive Message goes high. Thus Printer Selectable goes high.

NO.	NOTES.
1.	ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTOR 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
4.	INDICATES OPTION. INDICATES FEMALE AND INDICATES MALE TERMINAL,
5.	REFER TO 322062 FOR ASSEMBLY INFORMATION.
6.	S NUMBER: 61,434S.
7.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD. ML D 2 — ROW, COLUMN, INTEGRATED CIRCUIT
8.	CROSS REFERENCE NOTATION ON SCHEMATIC: 3 B 4 — ROW, COLUMN, SHEET
9.	THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC AND OV., RESPECTIVELY.
10.	VCC IS PROVIDED TO THE INTEGRATED PACKAGE ON PIN 14 AND GROUND ON PIN 7, THIS APPLIES TO ALL PACKAGES.
11.	REFER TO 8399WD. FOR LOGIC LEGEND AND TRUTH TABLES.
12.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER, THE GATE IS USED AS AN INVERTER.
13.	ABBREVIATIONS USED: FHDL - FULL & HALF DUPLEX LATCH. TABL - TABULATION LATCH. PELL - PARITY ERROR LAMP LATCH. PERL - PARITY ERROR RECEIVED LATCH. TCL - TIME CONTROL LATCH.
14	OPTIONS: A - DEDICATED HALF DUPLEX OPERATION STRAP A IN - STRAP B OUT. B - DEDICATED FULL DUPLEX OPERATION STRAP B IN - STRAP A OUT. C - ALTERNATE LINE RECEIVER. STRAP C MUST BE IN.
15.	REFERENCE CIRCUIT DESCRIPTION - 8383 WD-CD.
16.	INDICATES CIRCUIT GROUND.



8383WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R
2	2-24-69	96867-1
3	11-15-69	99881

kDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 1

SCHEMATIC WIRING DIAGRAM FOR RECEIVE CONTROL (WITH REGENERATOR)

APPROVALS	
D AND R	E OF M

E-NUMBER

PROD. NO. 8383 WD.

DATE 3-11-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. | CHKD.

ENGD. A.B. | APPD.

TELETYPE CORPORATION

8383WD

TC 434 (2-69)

SEE SHEET 1
FOR NOTES.

TIMER

BIT COUNTER

F X 32

B16

B17

MLF3 FF

MLF3 FF

MLC3 FF

MLC3 FF

MLD2 FF

MLD3

MLHI FF

MLHI FF

MLGI FF

MLGI FF

MLF1

MLF1

MLF1

MLE2

MLE3

MLE2

MLD3

MLE3

TCL

MLC1

MLC1

MLE1

MLE2

CR6

CR5

R15 100

C4 0.003

MLE3

CR3

CR4

MLE1

MLF1

B28 CHARACTER IN PROCESS

P.E. RESET

MLE3

1E2

MLF2

10 BIT CODE

B29

MLA3

LINE RCV DATA

B19

MLC1

MLC1

DATA

MLD1 FF

MLD2 FF

PARITY.

4.7K R5 VCC

B20 4.7K R18

RCV DATA (BB)

10K R17

CR2

Q4 2N3569

MLF2

B30 PARITY ERROR RCVD.

1D2

MLF2

REGENERATED DATA

B15

1C2

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 2

KCP

SCHEMATIC
WIRING DIAGRAM
FOR
RECEIVE CONTROL
(WITH REGENERATOR)

APPROVALS

D AND R	E OF M
WK	

E-NUMBER

PROD. NO. 8383 W.D.

DATE 3-6-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B.	CHKD.
ENGD. A.B.	APPD.

TELETYPE
CORPORATION

8383WD

8383WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

TC 450-0-(4)

CIRCUIT DESCRIPTION OF THE RECEIVE CONTROL CARD (W/REGENERATOR) (ASSEMBLY NUMBER 322062)

TABLE OF CONTENTS

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF THE RECEIVE CONTROL CARD (ASSEMBLY NUMBER 322062)

SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The 322062 Circuit Card Assembly controls and directs telegraph signals to the appropriate receiving device. The circuit receives serial input signals and provides serial output signals. An EIA input amplifier receives incoming on-line signals. Signals generated locally are received directly from sending distributors.

1.2 Several other functions are provided. These functions are:

1.2.1 Signal regeneration which changes input line data signals distorted 40% or less to output signals with less than 3% distortion. The regenerator assures a minimum character length of 9.8 units at 150 baud (150 wpm) and 10.6 units of 110 baud (100 wpm).

1.2.2 Detects improper received signal parity and provides power to an external parity error detection indicator lamp.

1.2.3 Half or full duplex selection - controls operation in either the half or full duplex mode.

1.2.4 Line or local tabulation - locks all sending devices during tabbing functions.

1.2.5 An output to indicate a receiving device in alarm - indicates an alarm condition for receivers.

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

The inputs to the circuit assembly are either EIA (RS-232-B) or nand type integrated diode transistor logic (DTL) inputs. EIA inputs are defined in Electronic Industries Association Standard RS-232-B. Each DTL input is approximately a 1.4 ma load to the device sinking current from it. At no time should any of these inputs be more positive than 8 volts or more negative than -.7 volts.

2.1.1 Received Data (Pin 20)

This input receives an EIA data signal from the signal line. This input is marking when the voltage is between 0V to -25V and is spacing when the voltage is between +3V to +25V. A spacing signal greater than .5 bit in length forces the regenerator to cycle and monitor the line for the duration of one character.

2.1.2 10-11 Bit Code (Pin 29)

This input is grounded when the regenerator is operating with signals containing 10 bits per character (one stop bit). It is open or high for characters containing 11 bits (two stop bits). The device driving this input must be capable of sinking three DTL loads.

2.1.3 FX32 (Pin 16)

This input is from an external oscillator. The frequency of the oscillator must be 32 times the desired bit rate. The device driving this input must be capable of sinking two DTL loads.

2.1.4 HDX N.O. (Pin 34)

This input is normally in the 1-state. When in the full duplex mode (FDX), a low (0-state) on this input will change the logic to half duplex mode. This contact must be capable of sinking two DTL loads.

2.1.5 FDX N.O. (Pin 26)

This input is normally in the 1-state. When in the half-duplex mode (HDX) a low on this input will change the logic to the full duplex mode. This contact must be capable of sinking two DTL loads.

2.1.6 Normalize (Pin 33)

This input is normally in the 1-state. At certain times it is desirous to condition selected set logic to a predetermined state. A low input on this lead will condition the full-half duplex latch (FHDL) to the half duplex state. This input represents one DTL load.

2.1.7 Signal Output (Local) (Pin 13)

This input is connected to the local distributor's data signal output and represents one DTL load. The signal moves through gated logic to the proper receiving device.

2.1.8 Signal Output (Line) (Pin 27)

This input is connected to the line distributor's data signal output and represents one DTL load. The signal moves through gated logic to the proper receiving device.

2.1.9 Parity Error N.O. (Pin 25)

This input is normally in the 1-state. A low on this input will reset the parity error lamp latch (PELL) which turns off the parity error received lamp driver. The device driving this input must be capable of sinking two DTL loads.

2.1.10 Line Trouble Indication (Pin 21)

This is an EIA input from an external control device or from a data set. It identifies an abnormal line condition. An ON condition causes the Parity Error or Line Trouble lamp to light.

2.1.11 Tab N.C. (Pin 22)

This is a contact input from the typing unit indicating to a local sending device that a tabbing condition is in process. The contact must be capable of sinking two DTL loads.

2.1.12 Tab N.O. (Pin 23)

Same as Section 2.1.11.

2.1.13 Printer Local (Pin 14)

This input primarily directs the proper data signals (line or local) to the typing unit and primes certain "receiver in alarm" gates. It also inhibits the line tab and parity error outputs (ribbon shift) when the printer is in the local mode. This input represents one DTL load.

2.1.14 Printer Selectable (Pin 10)

This lead monitors the typing unit's paper supply. With a full paper supply the lead is normally in the 0-state. It should revert to the 1-state when a paper out condition exists or upon termination of a call if a low paper condition exists. This lead represents one DTL load.

2.1.15 Printer Ready (Pin 9)

This input is normally low when the printer motor is operating. It reverts to the 1-state when the motors are OFF. This information is used to prime "alarm" logic. This lead represents one DTL load.

2.1.16 Punch Ready (Pin 7)

This input is normally low when the punch motor is operating. When the punch motor is OFF, it reverts to the 1-state. It is used to prime "alarm" logic. The input represents one DTL load.

2.1.17 Punch Local (Pin 8)

This input directs the proper data signals (line or local) to the punch and primes certain "receiver in alarm" gates. When this lead is in the 0-state, the punch receives local data. In the 1-state and no blind condition, the punch receives line data. This lead represents one DTL load.

2.1.18 Punch Blind (Pin 6)

When this input is in the 0-state, the punch is blinded to data signals. This input represents five DTL loads.

2.1.19 Punch Selectable (Pin 4)

This lead monitors the punch tape supply. With a full tape supply the lead is normally in the O-state. It should revert to the 1-state when a paper out condition exists or upon termination of a call if a low tape condition exists. This lead represents one DTL load.

2.2 Output Characteristics

The outputs from this assembly are either nand type diode transistor logic (DTL) or transistor driver outputs. Each output will be rated by the number of DTL loads it can sink. Each DTL load is approximately 1.4 ma.

2.2.1 Line Received Data (Pin 19)

This output follows the EIA received signal input lead. This lead is in the O-state when the EIA input is spacing and is in the 1-state when the EIA input is marking. It is used in other system logic to indicate the presence of a long spacing signal. This output will sink 20 DTL type loads.

2.2.2 Regenerated Data (Pin 15)

This output provides a data signal derived from the received signal input lead which is practicably distortion free. This lead is in the 1-state for a MARK and in the O-state for a SPACE. This output will sink seven loads.

2.2.3 Parity Error Received (Pin 30)

This output, normally in the 1-state, reverts to the O-state whenever a character is detected with incorrect vertical parity. This indication is presented at the end of the errored character. This lead will sink six loads.

2.2.4 Full Duplex (FDX) (Pin 24)

For half duplex operation this output is in the 1-state. When a full duplex command is received,this output reverts to the O-state. It is capable of sinking four loads.

2.2.5 Tab (Line) (Pin 31)

This output is normally in the 1-state. When a tabbing function occurs with the unit in the local and half duplex mode, the lead reverts to the O-state until the tabbing function is completed. This indication is used in other system logic to intercept the line distributor's "PRESENT NEXT CHARACTER" (PNC) output. It will sink eight DTL loads.

2.2.6 Tab (Local) (Pin 12)

This output is normally in the 1-state. When a tabbing function occurs with the typing unit in the local mode, the lead reverts to the O-state until the tabbing function is completed. This indication is used in other system logic to intercept the local distributor's "PRESENT NEXT CHARACTER" output. It will sink eight DTL loads.

2.2.7 Printer Serial Data (Pin 11)

This lead presents serial data derived from the incoming signal line from the line/local distributor to the printer selector magnet driver. It is in the 1-state for a marking bit and in the 0-state for a spacing bit. This output will sink seven DTL loads.

2.2.8 Punch Serial Data (Pin 3)

This lead presents serial data derived from the incoming signal line or from the line/local distributor to the punch selector magnet driver. A marking bit is in the 1-state and a spacing bit is in the 0-state. This output will sink seven DTL loads.

2.2.9 Receiver in Alarm (Pin 5)

This output indicates to external logic that a receiving device is in an alarm condition or that no receiving device is available. This lead is normally in the 1-state but changes to the 0-state when an alarm condition is present. This output will sink four DTL loads.

2.2.10 Parity Error Not(Pin 32)

This output normally in the 0-state reverts to the 1-state upon the reception of a parity errored character and remains in the 1-state until a character with the correct parity is received. This signal is used in external logic to change the color of the printed character. Eight loads may be attached to this lead.

2.2.11 Line Trouble/Parity Error Lamp (Pin 18)

This output drives a lamp located on the control strip to indicate a parity error. A parity error will cause this lead to change to the "ON" state providing power to this lamp. It remains in this state until manually reset.

2.2.12 Character in Process (Pin 28)

When this lead is in the 1-state, the regenerator is idling. This lead reverts to the 0-state during the time in which a character is processed through the regenerator. This output will sink one DTL load.

2.3 Size

The receive control card measures 5-3/4 x 4-1/4 inches. It is designed to mate with a standard 36 pin circuit card connector.

2.4 Options

2.4.1 10-11 Unit Code

The receive control may be changed from an eleven unit code to ten unit code by grounding Pin 29.

2.4.2 Half Duplex (Strap A)

The assembly may be permanently strapped for half-duplex by having strap A in place.

2.4.3 Full Duplex (Strap B)

The assembly may be permanently strapped for full duplex by having strap B in place and removing strap A.

2.4.4 Auxiliary Receiver (Strap C)

Strap C remains in place when an auxiliary receiving device, such as a reperforator, is part of the system. It is used to indicate, along with other receiving devices, a capability to receive incoming line data. If no receiving device is in the line mode, an alarm condition is generated.

2.5 Miscellaneous Requirements

2.5.1 Power Supply Requirements

V_{DC}	I ma (max)
5V to 6.6V	390 ma

2.5.2 Operating Temperature Range

0°C to 70°C (free air)

2.5.3 Storage Temperature Range

-40°C to +70°

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 See assembly drawing 322062 (MC062) and schematic drawing 8383 WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 General

The Receive Control card assembly is described in two parts, signal regeneration (regenerator) and data control (receive control). Refer to the timing diagrams, flow chart, and schematic 8383 WD to aid in understanding the following description. The flow chart is intended to be used as a guide to help in understanding the operation of the regenerator. It should be studied in conjunction with the circuit schematic and timing diagram. The rectangular symbols denote functions that are to be performed, and the triangular shaped symbols denote a decision point. It is not intended that any of the symbols be construed to represent logic functions. The flow chart is primarily intended to relate circuit operation with respect to time.

2.2 Regenerator

The mode of operation described first is for characters of 10 unit code. This requires a ground or 0-state on Pin 29.

Assume that the regenerator is in an idle condition. The timer is not operating because the output of the Start Gate, MLD3-6, is in the 0-state. This gate is in the 0-state when the receive signal input is MARKING continuously and the Timer Control Latch, TCL, has been reset. TCL resets at the end of each character.

When a SPACING signal (Start bit) appears at the receive signal input, Pin 20, the output of MLC1-11 switches to the 0-state. This forces the Start Gate to the 1-state, releasing the timer.

After 1/2 bit time duration, a clock pulse appears at MLD3-8. This sets a one count in the bit counter, which in turn sets TCL via MLF1-3 and MLF1-6. The output of the TCL clamps the Start Gate "ON" for a full character interval. Control of the timer is now removed from the signal line.

If the SPACING signal is not present for a full 1/2 bit interval, however, the TCL will not have been set. Consequently, as the Receive Signal Input returns to a MARK, the Start Gate reverts to a 0-state, clearing the timer to the idle state. A character, therefore, will not be regenerated.

When the SPACING signal is longer than 1/2 bit, the timer is locked on and delivers clock pulses at bit frequency. These pulses are used to

cycle the bit counter, the data flip-flop, and the parity flip-flop. The function of each of these circuits is as follows:

2.2.1 Bit Counter

The function of the bit counter, composed of four binary elements and two gates arranged to operate as a decade counter, is that of timing out a character interval. When a count of ten is reached, the output of MLF1-3 switches to the 0-state. (Refer to the diagram and timing chart of Figure 1 for information on intermediate states of the bit counter.)

2.2.2 Data Flip-Flop

Clock pulses generated by the timer process data through the Data Flip-Flop, MLD1. Incoming line data (which may be distorted) appears at the synchronous set and clears inputs of MLD1. This data is sampled and read into the data flip-flop by the clock pulses. The inverted output of the data flip-flop, distortion free, is applied to the Regenerated Data Gate, MLF2-11.

2.2.3 Parity Flip-Flop

The function of the parity flip-flop is to search for even parity on the 8 data bits of a character. The parity flip-flop changes states each time a MARK signal from the data flip-flop is read into it by the timer clock. The inverted output of the parity flip-flop is applied directly to the Parity Error Received Gate, MLF2-6, where it is sampled at the end of each character by the bit counter. The output of the gate remains in the 1-statefor correct parity or, conversely, switches to the 0-state if a parity error has been detected.

2.2.4 Timer Control Latch Reset

After the 10th count is reached, the timer continues counting for an interval designed to guarantee regeneration of a minimum length stop bit. When operating in the 10 unit character code, this time period is approximately 0.3 of a bit. At this time Stop Bit Regenerator Gate, MLE1-6, has three of its four inputs primed (extender inputs CR5 and CR6 primed by 10 unit code and TCL respectively) to reset the timer control latch. The remaining input is controlled by the Synchronism Gate, MLE3-8, which senses for either the presence of correct parity or the presence of a marking bit in the data flip-flop. If either is present the regenerator is considered to be in synchronism with the signal line and gate MLE3-8 is in the 1-state. Now all inputs of the stop bit regenerator gate are in the 1-state, resetting TCL and the timer. The regenerator now waits for a new character.

If the regenerator is not in apparent synchronism with the signal line, i.e., parity incorrect and no marking bit in the data flip-flop, Synchronism Gate, MLE3-8, will not permit the stop bit regenerator gate to reset TCL and the timer. The regenerator continues to run 0.3 of a bit

beyond the next clock pulse or pulses until the conditions for synchronism are achieved. Only then will TCL and the timer be reset. The regenerator logic is now conditioned for the start of a new character. It waits for the next 1/2 bit SPACING "start" signal to begin a new cycle.

For units operating with characters consisting of 11 bits, i.e., with two stop bits, Stop Bit Regenerator Gate, MLE1-6, is electrically replaced by Stop Bit Regenerator Gate MLE1-8. This is accomplished by removing the ground on Pin 29. MLE1-6 is inhibited through its CR5 input while MLE1-8 is primed through its CR3 input. The Stop Bit Regenerator Gate, MLE1-8, operates in a very similar manner to MLE1-6. Its function, however, is to time out 1.1 bit elements instead of .3 elements after the 10th count. Three inputs are used for this purpose, two from the timer and one from a latch made up of MLE3-11 and MLE2-8.

The MLE2-12 gate has inputs from the timer such that when .75 bits are sensed, the MLE3-11, MLE2-8 latch is set. Approximately .35 bits later the two inputs to MLE1 from the timer are high. If apparent synchronization is present (MLE3-8 high) the Stop Bit Regenerator Gate switches to the 0-state, resetting TCL. When TCL is reset, the MLE3-11, MLE2-8 latch is reset, and MLE1-8 is inhibited via diode CR4.

2.2.5 Parity Count Inhibit Gate

The function of the Parity Count Inhibit Gate, MLF2-3, is to prevent sampling for parity of the incoming signal during a stop bit. When the first clock pulse occurs, the stop bit of the previous character is stored by the data flip-flop. Consequently, the first clock pulse should not sample the data flip-flop for parity. Also, when operating in the 11 unit character mode, the last clock pulse of a character occurs during the stop pulse and, therefore, should not be permitted to sample the data flip-flop. During both these time periods the output of MLF2-3 is low and the parity flip-flop is inhibited.

2.3 Receive Control

The second major function of the receive control circuit card is: to direct data received from a multiplicity of sources to the proper receiving device, to control the receiving alarm indicators, and to perform miscellaneous control functions associated with the receivers.

2.3.1 Receive Data Logic

Data is received from three sources. These are: regenerated data from the regenerator, data generated by the on-line sending distributor, and data generated by the local sending distributor. Assume a half duplex operating mode. Data received from the local sending distributor passes through MLG3-6 and primes output serial data gates associated with the printer and punch. Data associated with the line distributor passes through MLB1-3, MLB1-6 (primed in the half duplex mode) and MLF2-8. The MLF2-8 output also

primes serial data gates associated with the printer and punch. Receive data from the regenerator passes through MLF2-8 and also primes serial data gates associated with the punch and printer.

The input at Pin 14 is low when the printer is in the local mode, and high when it is in the on-line mode. Consequently, MLG3-11 is primed only when the printer is in the on-line mode. Thus, local data appears at Pin 11, the printer serial data output, when a printer local command appears at Pin 14, and on-line data appears at Pin 11 when an on-line command appears at Pin 14.

When the punch is in the local mode a low appears at Pin 8, and when the punch is on-line a high appears at that input. This input primes gate MLG2-6 which has as its second input the punch blind signal received at Pin 6. The punch blind signal is low when the punch is to be blinded and high when it is to be enabled. Thus, when the punch is local and enabled, only local data will appear at Pin 3, the punch serial data output. When the punch is enabled, on-line (Pin 8 high) and only on-line data will appear at Pin 3. When the input received at Pin 6 is low, signifying that the punch is to be blinded, the output at Pin 3 will remain continuously MARKING.

2.3.2 Receive Alarms

The output at Pin 5, receiver in alarm, is high when all receivers are functioning normally and low for an alarm condition. An alarm condition exists when one of the receiving devices is unable to function, i.e., out of paper, or, when no receiver is in the on-line condition during receipt of a message. The following are alarm conditions:

Condition 1: The printer is on-line, the printer motors are not yet up to speed(printer not ready, Pin 9 high), and a spacing bit is received on line. MLH2-12 is switched.

Condition 2: The printer is on-line and a paper alarm is present. MLG2-8 is switched.

Condition 3: No receiving device is in the on-line mode. MLG2-11 is switched.

Condition 4: The punch is on-line and a tape alarm is present. MLH2-6 is switched.

Condition 5: The punch is on-line, the punch motors are not yet up to speed (punch not ready, Pin 7 high), and a spacing bit is received on line. MLH1-6 is switched.

All alarm gate outputs are connected together and appear at Pin 5. For applications where a printer must be on-line for a call to be received, strap C is removed. With strap C removed, MLC2-11 will switch to an alarm condition whenever the printer is off-line.

2.3.3 Tabbing Control

The purpose of the tabbing control logic is to prevent transmission from a local reader or keyboard until response to a tabbing function is completed by the local printer. The tabbing latch, TABL, is set by a contact on the typing unit during tabbing and is reset by a contact when the tabbing is complete. The output of this latch at MLB1-8 primes the MLA1-6 and the MLG2-3 gates. The MLG2-3 gate has two inputs. The second input is primed while the printer is in the local mode. The MLA1-6 gate has three inputs. The second input is high while the printer is on-line, and a third input to the MLA1-6 gate is high when the unit is in the half duplex mode. Thus a line tab indication at Pin 31 (0-state) will be present only when the typing unit is on-line, tabbing is in process, andthe terminal is in the half duplex mode. A tab condition will be present at Pin 12 (0-state) only when the printer is in the local mode and tabulation is in process.

2.3.4 Full Duplex

A full duplex latch, FHDL, is operated directly from the typing unit. When a full duplex command is sensed, Pin 26 is shunted to ground (0-state) setting the latch. The latch is reset bhen a half duplex command at Pin 34 is sensed, or when the system is normalized by a logical zero at Pin 33. The output of the latch, MLA1-12, at Pin 24, is a logical zero for full duplex and a logical one for half duplex. The output of FHDL also primes gates MLB1-6 and MLA1-6. When in the full duplex mode, locally generated line data will not pass through MLB1-6 and, therefore, will not be copied by the local printer. When in the full duplex mode, and while a tabulation is taking place, the line tab output will remain high. Transmission by a local reader or keyboard will continue, therefore, since the system is in full duplex mode.

The system may be wired permanently full duplex or permanently half duplex. For permanent full duplex, strap B should be connected and strap A removed. For permanent half duplex operation, strap A should be connected and strap B removed. For on-line control, both straps are removed.

2.3.5 Parity Error Display Logic

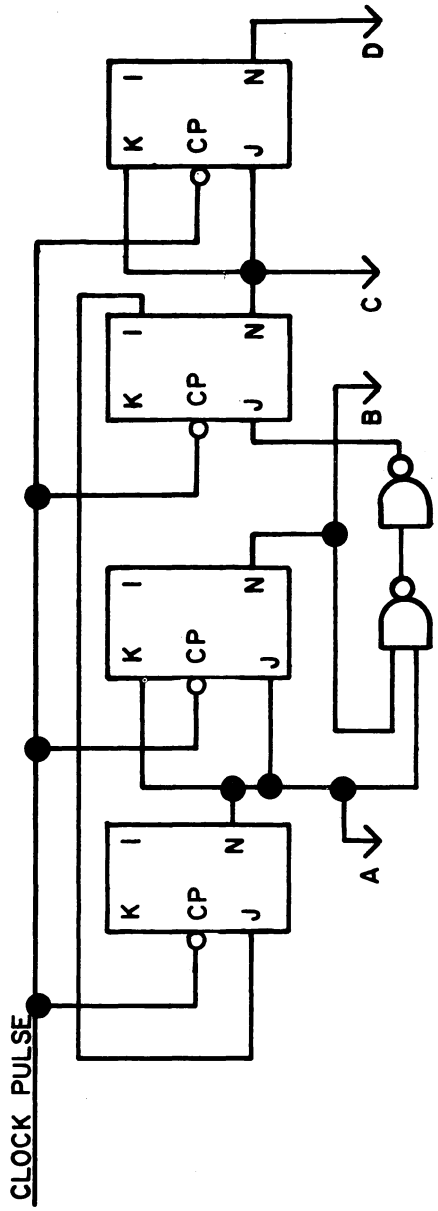
Parity errors may be displayed in either or both of two ways. These are a lamp located on tye control panel, or, by a ribbon shift to print the errored character in red. When a parity error is detected by the parity error circuitry of the regenerator, the parity error lamp latch, PELL, and the parity error ribbon latch, PERL, are both set. The output of the PELL latch drives a lamp amplifier composed of transistors Q2 and Q1, having an output at Pin 18. The output is turned ON, a logical lamp zero for a parity error. The output may also be turned ON by an EIA input (1-state) at Pin 21, the line trouble indication input. The "Parity Error or Line Trouble" output may optionally display either parity error or line trouble (Carrier Fail) or both. The PELL latch, and the associated parity error or line trouble lamp is turned OFF by a logical zero applied

at Pin 25. The logical zero is derived from a reset switch contact closure on the control panel.

As an option, the parity error causes the printing of the errored character in red via the PERL latch. The output of this latch is applied through MLA3-3 and MLA3-6 to Pin 32. A logical one at Pin 32 operates the ribbon magnet through an amplifier on the ribbon magnet amplifier card. At the end of a character, the PERL latch is reset by the regenerator or by receipt of a SPACING signal identifying the beginning of the next character. A second input to the MLA3-3 gate prevents operation of the parity error ribbon circuitry when the printer is in the local mode.

BIT COUNTER DIAGRAM AND TIMING CHART

	0	1	2	3	4	5	6	7	8	9
A	L	H	L	H	L	L	H	L	H	L
B	L	L	H	H	L	L	L	H	H	L
C	L	L	L	L	H	L	L	H	L	H
D	L	L	L	L	L	H	L	L	H	H



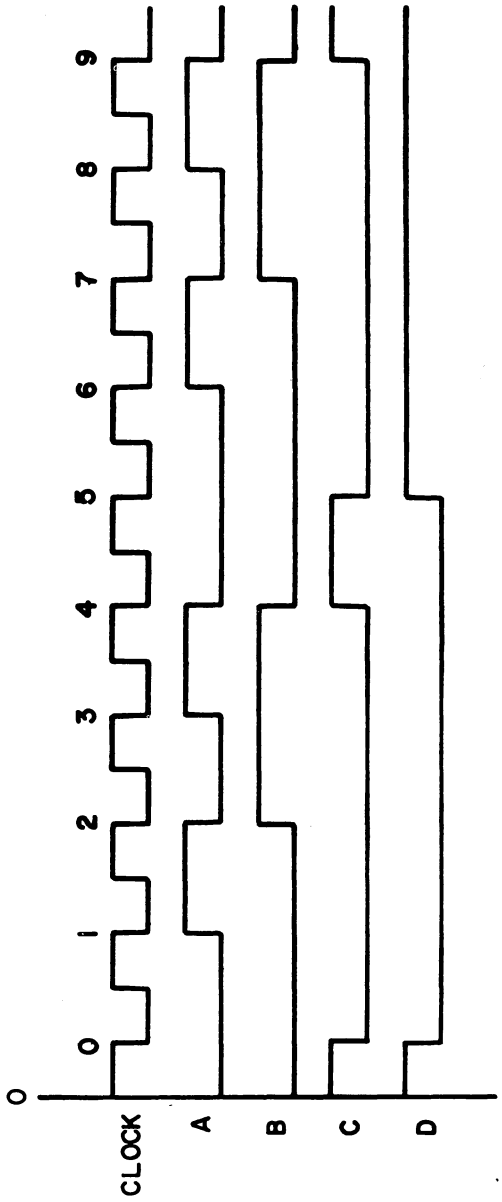


FIGURE 1

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

TIMING DIAGRAM
RECEIVING SIGNAL REGENERATOR
P/O 322062 RECEIVE CONTROL ASSEMBLY

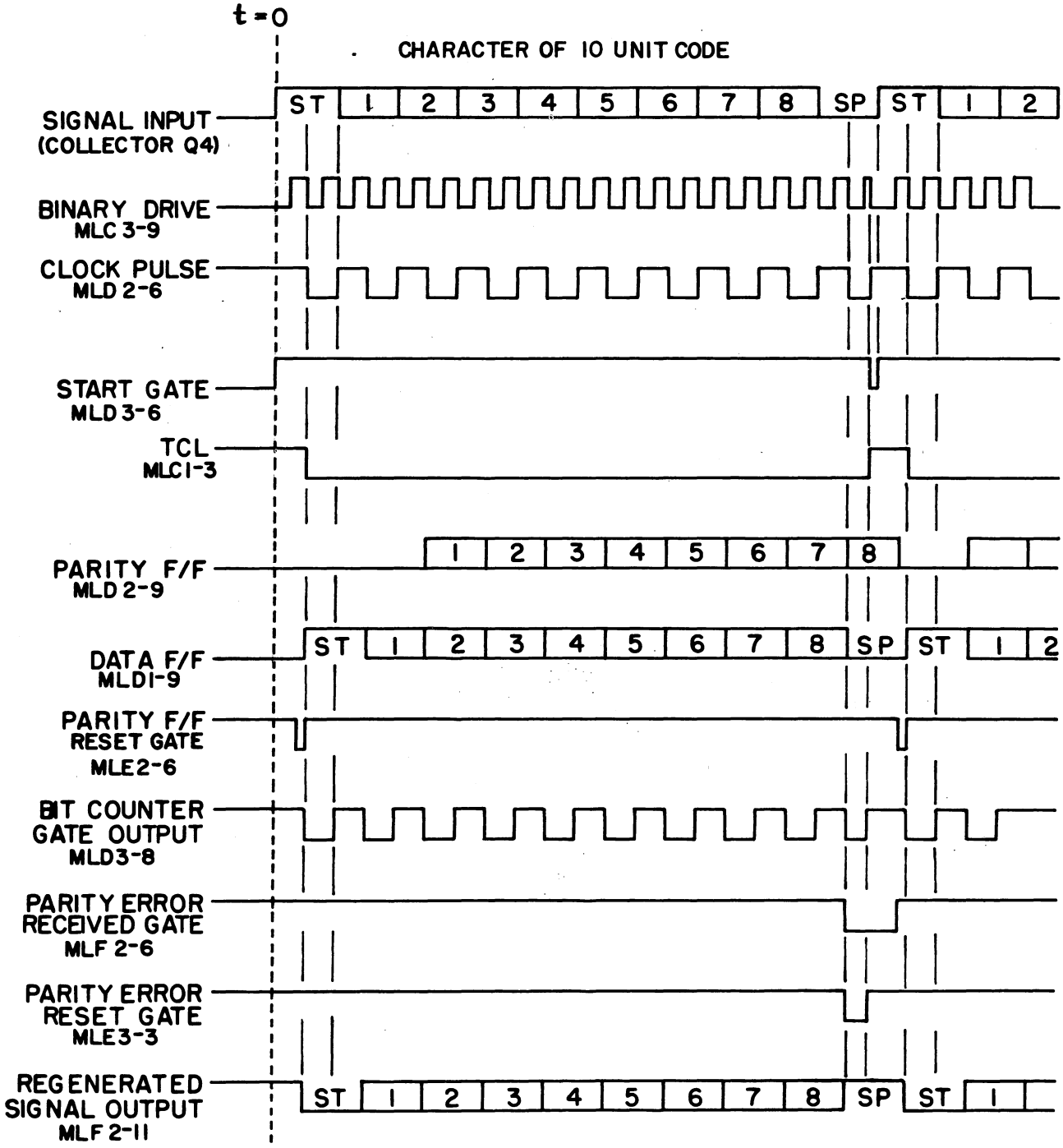


FIGURE 2

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

TIMING DIAGRAM
RECEIVING SIGNAL REGENERATOR
P/O 322062 RECEIVE CONTROL ASSEMBLY

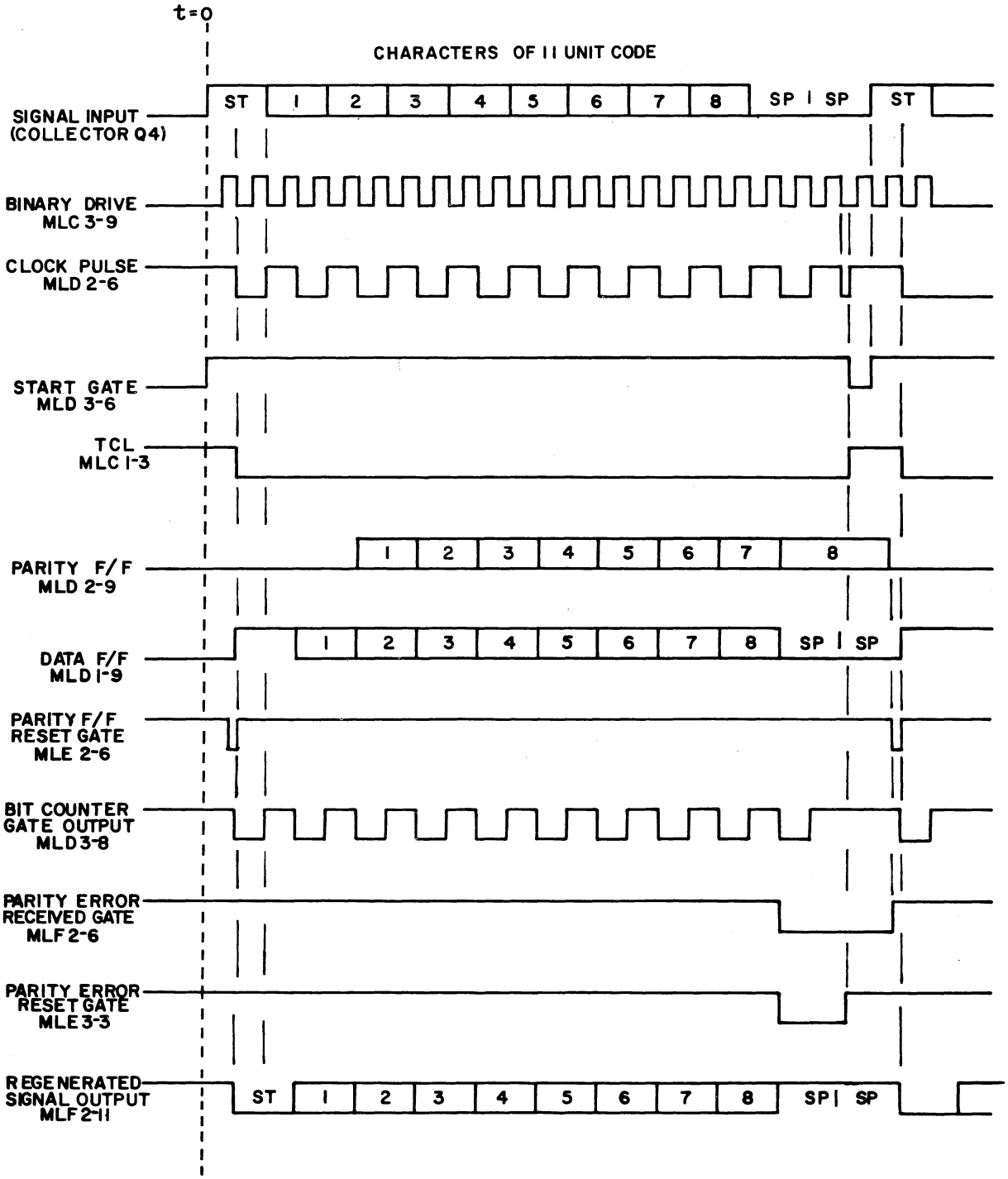


FIGURE 3

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

TIMING DIAGRAM
RECEIVING SIGNAL REGENERATOR
P/O 322062 RECEIVE CONTROL
ASSEMBLY.

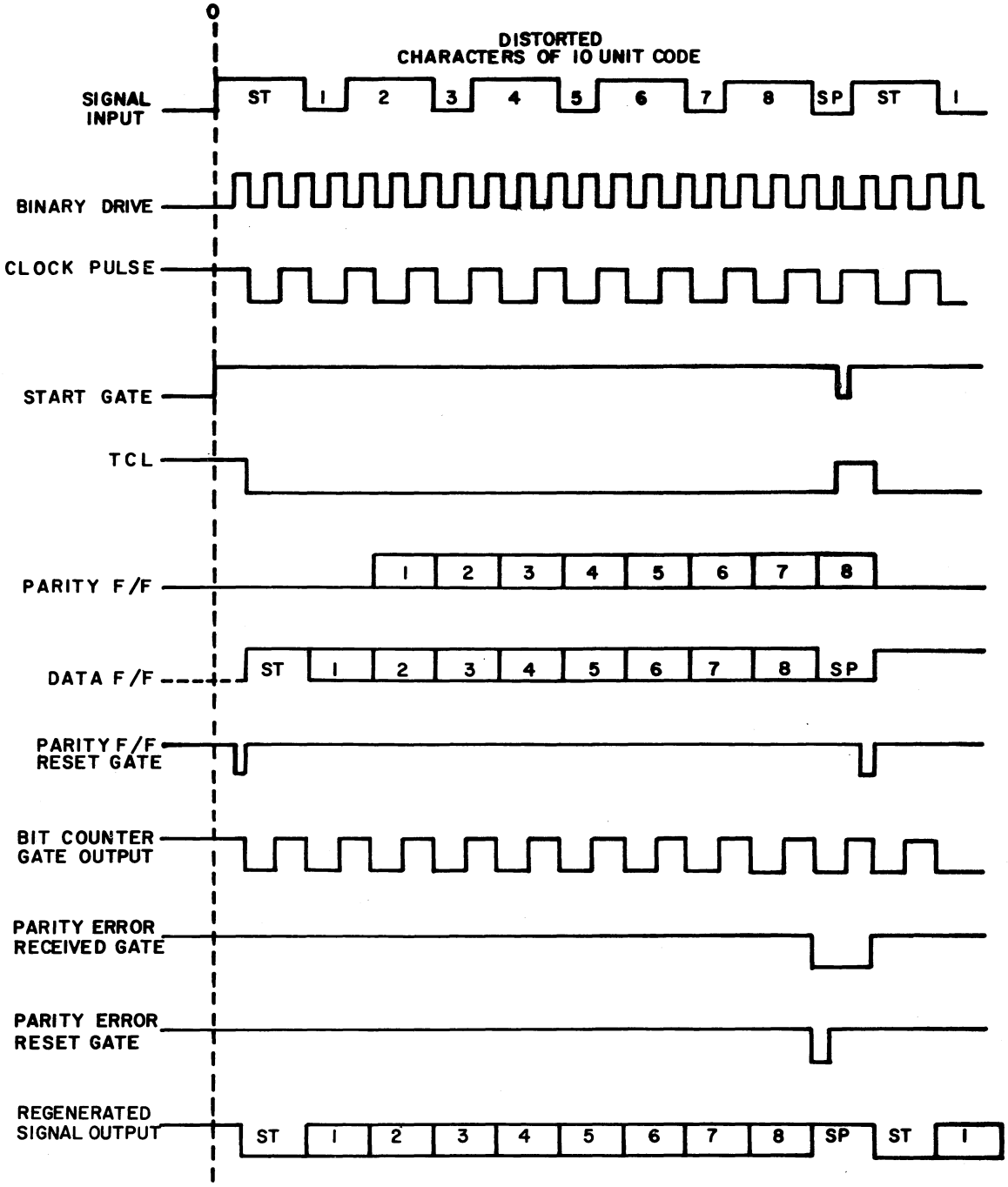
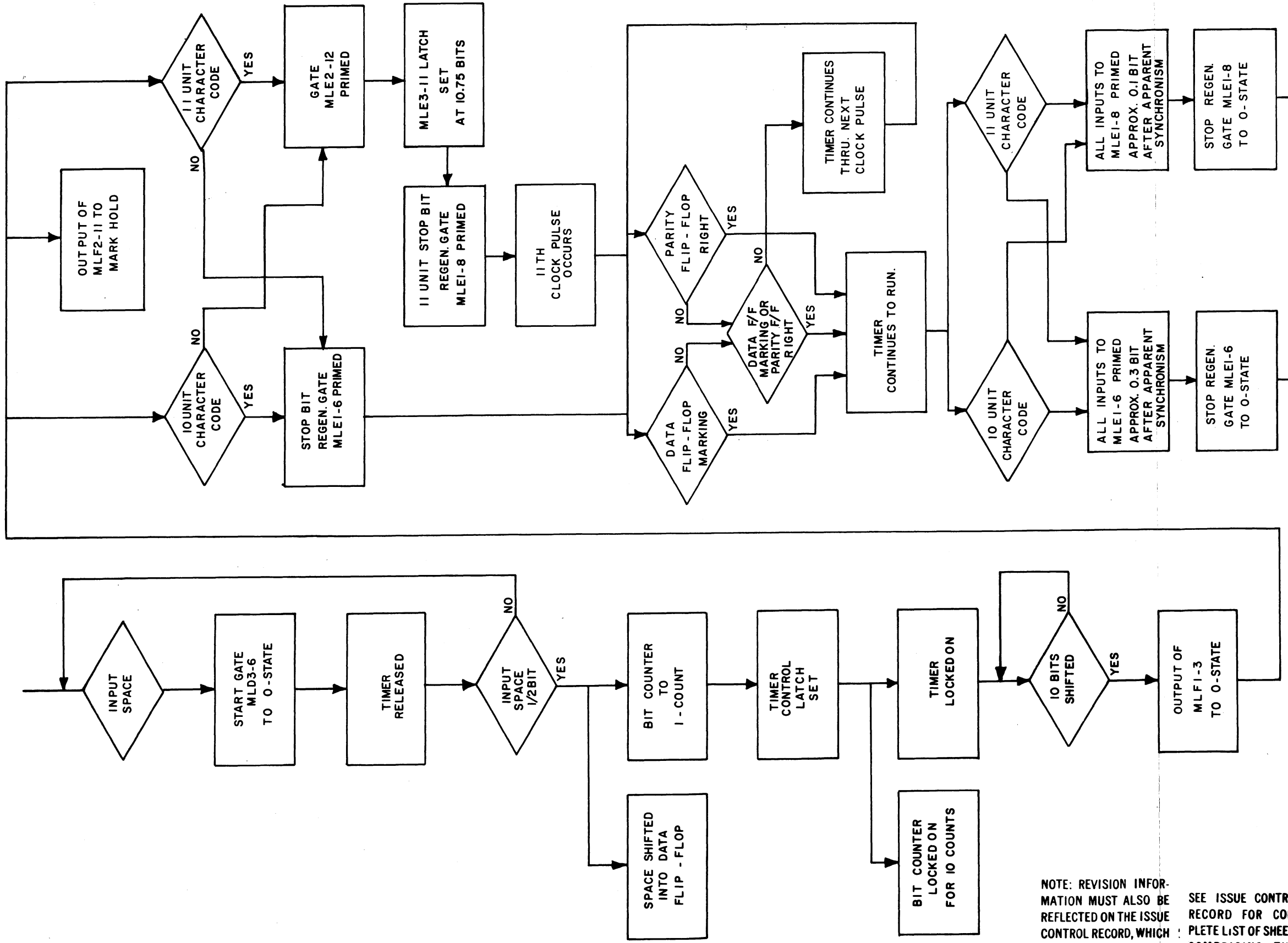


FIGURE 4

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

FLOW CHART
RECEIVING SIGNAL REGENERATOR
P/O 322062 RECEIVE CONTROL ASSEMBLY

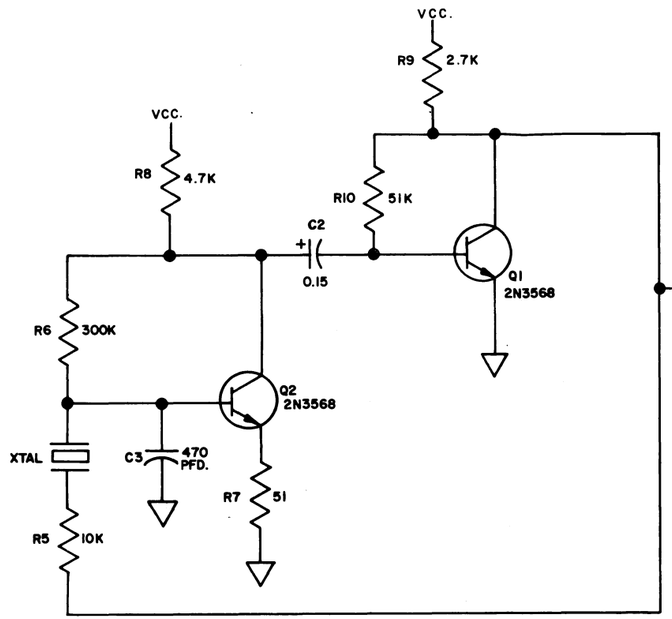


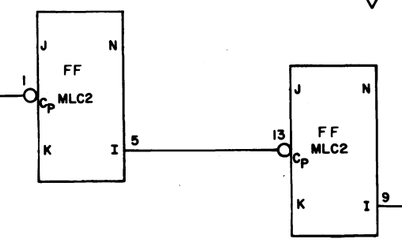
NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

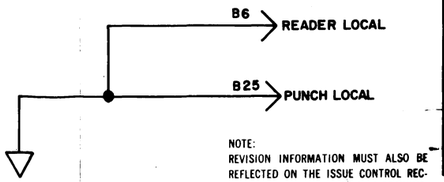
SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

FIGURE 5

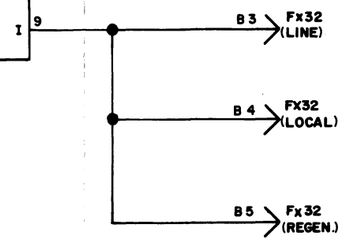
NO.	NOTES
1.	ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
4.	INDICATES FEMALE TERMINAL AND INDICATES MALE TERMINAL
5.	REFER TO 322067 FOR ASSEMBLY INFORMATION.
6.	S NUMBER: 61,516 S.
7.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD: ML D 2 — ROW, COLUMN, INTEGRATED CIRCUIT
8.	THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC AND 0V, RESPECTIVELY.
9.	LOGIC NEGATION- A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
10.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER, THE GATE IS USED AS AN INVERTER.
11.	VCC. IS PROVIDED TO THE INTEGRATED CIRCUIT PACKAGE ON PIN 14 AND GROUND ON PIN 7, THIS APPLIES TO ALL PACKAGES.
12.	REFER TO 8399WD FOR TRUTH TABLES.
13.	OPTIONS: A - 10-11 BIT CODE. ADD STRAP FOR 10 BIT CODE.
14.	REFERENCE CIRCUIT DESCRIPTION: 8387 WD-CD.
15.	ABBREVIATIONS USED: LLFF - LINE LOCAL FLIP-FLOP
16	R15 AND C6 NOT INCLUDED ON SOME CARDS
17.	ORIGINALLY KSR MODE CONTROL.

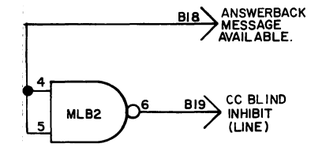


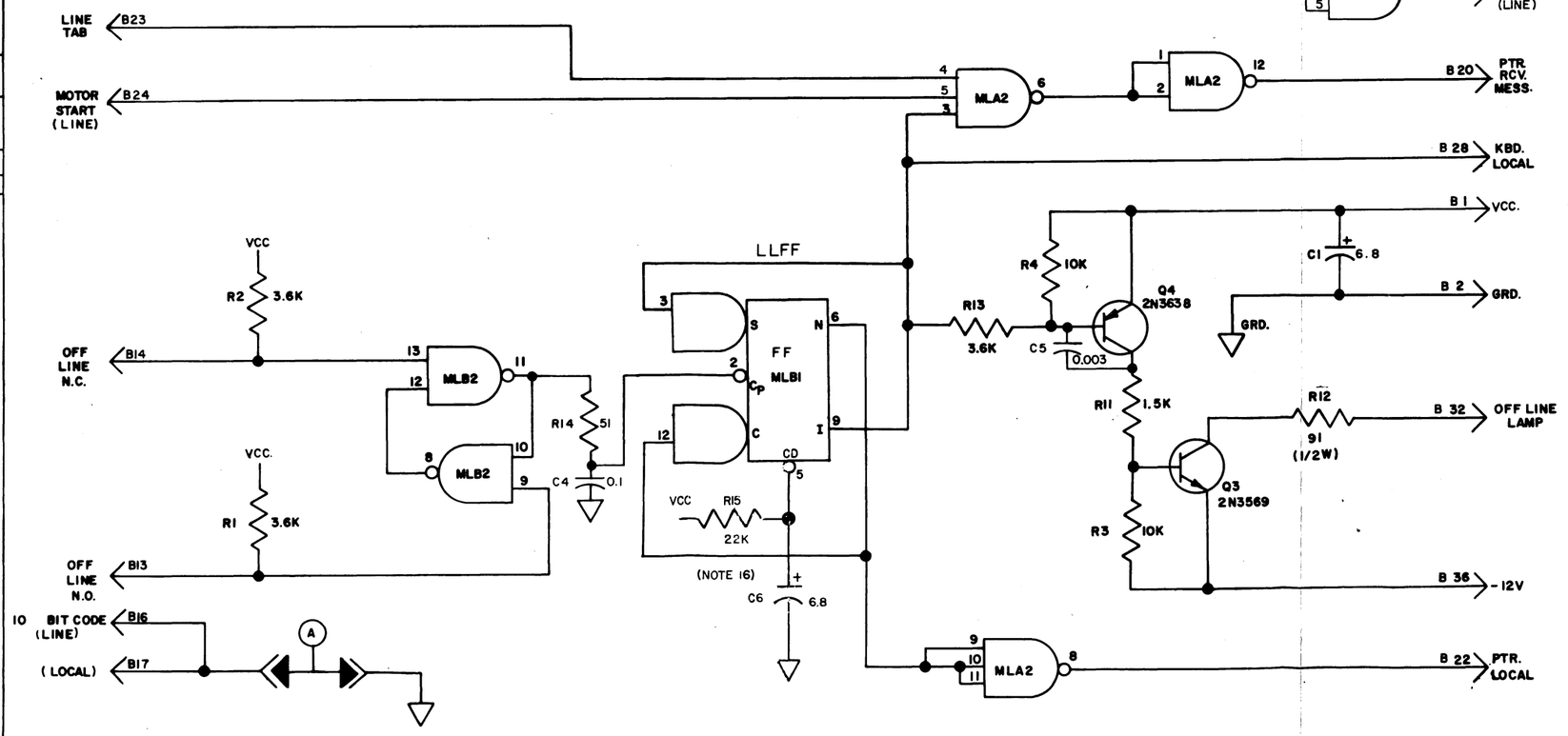




NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.







WDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 1 - NOTE 17

R.O. AND KSR MODE CONTROL

8387 WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R
2	10-22-68	96395
3	6-20-69	99181
4	2-5-70	99993

APPROVALS

D AND R	E OF M
HSK	

E-NUMBER

PROD. NO. 8387 WD

DATE 9-9-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. CHKD.

ENGD. REL APPD.

TELETYPE CORPORATION

8387 WD

TC 084 (5-68)

CIRCUIT DESCRIPTION OF THE R.O. AND KSR MODE CONTROL CARD (ASSEMBLY NUMBER 322067)

TABLE OF CONTENTS

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF THE R.O. AND KSR MODE CONTROL CARD (ASSEMBLY NUMBER 322067)

SECTION I

1. BASIC FUNCTION

1.1 The 322067 Circuit Card Assembly is a mode control and set clock for Model 37 R.O. and KSR sets operating at 150 wpm with 10 unit code (150 baud).

1.2 Two mutually exclusive mode selections are provided by one switch:

A. OFF-LINE

B. ON-LINE

1.3 The mode control circuit is associated with a switch and a 30 ma @24V lamp on the control panel located above the keyboard.

1.3.1 When the switch is lighted, the set is in the "OFF-LINE" (local) mode.

1.3.2 When the switch is not lighted, the set is in the "ON-LINE" mode.

1.3.3 Fixed outputs are provided to maintain any punch or reader, which may be associated with the set, in the "OFF-LINE" mode.

2. GENERAL TECHNICAL DATA (All card pins appear on the "B" (non-component) side of the card.)

2.1 Input Characteristics

The inputs to the assembly are positive nand type integrated Diode Transistor Logic (DTL) inputs. Each DTL input is approximately a 1.4 ma load to the device sinking current from it. At no time should any of these inputs be more positive than 8 volts or more negative than -.7 volts. Voltage levels represented by the 1-state (high) and 0-state (low) are approximately +5.25V and 0V respectively. A logic one (high) draws no current from the input of the logic element.

2.1.1 "OFF-LINE" Mode-Switch (N.O. Pin 13, N.C. Pin 14)

The momentary break-before-make transfer mode switch generates a square pulse through a latch circuit, formed by a pair of gates, and into the toggle input of a J-K flip-flop. The flip-flop changes output state each time the mode switch is pressed. The device driving this input must be capable of sinking two DTL loads. (See General Timing Diagram)

2.1.2 Motor Start (Pin 24)

This pin is low to start the printer and punch motors during "ON-LINE" operation and is one DTL load.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

2.1.3 Line Tabulation (Pin 23)

This pin is low throughout any tabulation function which is started while the printer is "ON-LINE" and high at all other times. The device driving this input must be capable of sinking one DTL load.

2.1.4 Answer Back Message Available (Pin B18)

This lead is low throughout any Answer Back cycle. It is high at all other times. The device driving this input must be capable of sinking one DTL load.

2.2 Output Characteristics

2.2.1 Off-Line Lamp (Pin 32)

When the flip-flop output, MLB1 Pin 9 is low, the lamp associated with the "OFF-LINE" switch is lighted by a lamp driver circuit, Q3 and Q4 (Pin 32) which applies approximately 24 volts across the bulb.

2.2.2 Keyboard Local (Pin 28) - (KSR only)

The output of the flip-flop is also routed off the card to control other circuitry in the set and will be low during the "OFF-LINE" (Local) mode (Pin 28). This output is capable of driving 7 DTL loads.

2.2.3 Printer Local (Pin 22)

This pin is low when the "OFF-LINE" (Local) mode is selected, (same as Pin 28), and is capable of driving 8 DTL loads.

2.2.4 Punch Local (Pin 25)

This pin is low at all times and will keep any associated punch in the "OFF-LINE" mode at all times.

2.2.5 Reader Local (Pin 6)

This pin is low at all times and will keep any associated reader in the "OFF-LINE" mode at all times.

2.2.6 Set Clock (Internal to Card)

The set clock is a crystal controlled multivibrator operating at 128 times the bit rate (19.2KHZ @ 150 baud). (See General Timing Diagram)

2.2.7 Clock Pulse (Pin 3,4,5)

The set clock frequency is divided by four by a pair of flip-flops and is available as an output of 32 times the bit rate and is capable of driving ten DTL loads.

2.2.8 10-11 Bit Code Selection (Pins 16, 17)

Strap A is provided to ground the 10 bit input lead on the electronic distributor used in the set. If this strap is removed, an 11 bit code will be generated, but a different crystal is required to obtain the correct bit rate as indicated in Section 2.2.5.

2.2.9 Printer Receive Message (Pin 20)

A low on this pin indicates to the printer that itsmotor should be started. This pin will be low when in the "OFF-LINE" mode or during tabulation on-line, or when "motor start" is low. This output is capable of driving eight DTL loads.

2.2.10 Control Character Blind Inhibit (Line) (Pin B19)

This output in the O-state, inhibits the line distributor from pausing for one character interval, following the transmission of a control character. This output is capable of driving eight DTL loads.

2.3 Mechanical Requirements

The 322067 card assembly is a standard 5-3/4 inch by 4-1/4 inch 36-pin circuit card which is inserted into a 36-pin edge card connector.

2.4 Power Supply Requirements

Vcc(DC)	Current Maximum
+5.0V - +6.6V (+5.25V Nom.)	60 ma
+11.65V - +13.75V (+12.5V Nom.)*	30 ma
-11.88 V - -13.12V (-12.5V Nom.)	30 ma

* +12.5 Volts is used for the lamps.

2.5 Temperature Rante

The ambient temeerature range for operation is from 0°C to 70°C in free air. Non-operating storage temperature is from -40°C to 70°C.

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly and schematic drawings 322067 (MC067) and 8387 WD.

1.2 Logic symbols and truth table 8399 WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 Mode Switching

The mode switch is comprised of a momentary contact transfer switch (break before make) containing a lamp indicator. When the switch is operated, the normally closed contact opens first enabling the input to the associated gate, which is part of a latch arrangement. The input of this gate is held low, however, by the other half of the latch associated with the normally open contact. Next, the normally open contact closes, driving the input of its associated gate low and switching the output high. The output of the gate associated with the normally closed contact then switches low, causing a high to low transition on the input to the J-K flip-flop, changing its state. (The output of the J-K flip-flop changes state each time a high to low input transition occurs on the input.)

When the mode switch is released, the normally open contact returns to its open condition and enables the input to its associated gate. Next, the normally closed contact returns to its closed condition, putting a low input on its gate, which returns the output of the latch to a high. This low to high transition occurs on the input to the J-K flip-flop, but has no effect on its output.

The output of the flip-flop drives a lamp through an amplifier (Pin 32), and also leaves the card to control other circuitry (Pin 22 and 28).

2.2 Lamp Driver

A low input to the lamp driver provides a current path through the 3.6K resistor and from the base of a PNP transistor. The transistor turns on, and provides a bias current through the 1.5K ohm resistor to turn on the NPN transistor. This transistor acts as a switch connecting the lamp from the +12.5 volt supply, through a 91 ohm limiting resistor, to the -12.5 volt supply. Thus the lamp is turned on.

2.3 Set Clock

2.3.1 The set clock is a crystal controlled, astable multivibrator composed of Q1 and Q2 operating at 128 times the bit rate. The transistors are arranged as grounded emitter inverting amplifiers with R7 providing

some stabilization and feedback for Q2 and R10 providing bias for Q1. R6 provides collector feedback and base bias for Q2. C2 couples the output of Q2 to the base input of Q1. A quartz crystal provides feedback from the collector of Q1 through current limiting resistor R5 and into the base of Q2 at the critical frequency of the crystal. A negative transition on the Q2 base momentarily turns it off, thus causing a positive transition to be coupled by C2 into the Q1 base, momentarily turning it on and causing a negative transition to be coupled through the crystal and again momentarily turn Q2 off. C2 decouples oscillations of higher harmonics that might occur due to stray capacitances associated with the crystal.

The output of Q1 is also connected to the input of the J-K flip-flop, where every negative transition causes a change in the state of its output, thus dividing the frequency in half. This signal is again divided in half by the other J-K flip-flop. The clock signal leaves the card as Fx32.

2.4 Motor Control (Line)

Punch and printer motors are turned on whenever the set is either in the "OFF-LINE" mode, or when a message is being received "ON-LINE". Additionally, the typing unit motors are held "on" while tabulating "ON-LINE", even though a message has been completed.

2.4.1 A "motor start" signal, signifying that a message is present "ON-LINE", enters the assembly and is gated with the keyboard local and line tabulation signals, and is then inverted, so that the "Printer Receive Message" output will be low when a "motor start" signal is received, or when the keyboard is in the "local" mode.

2.5 Control Character Blind Inhibit

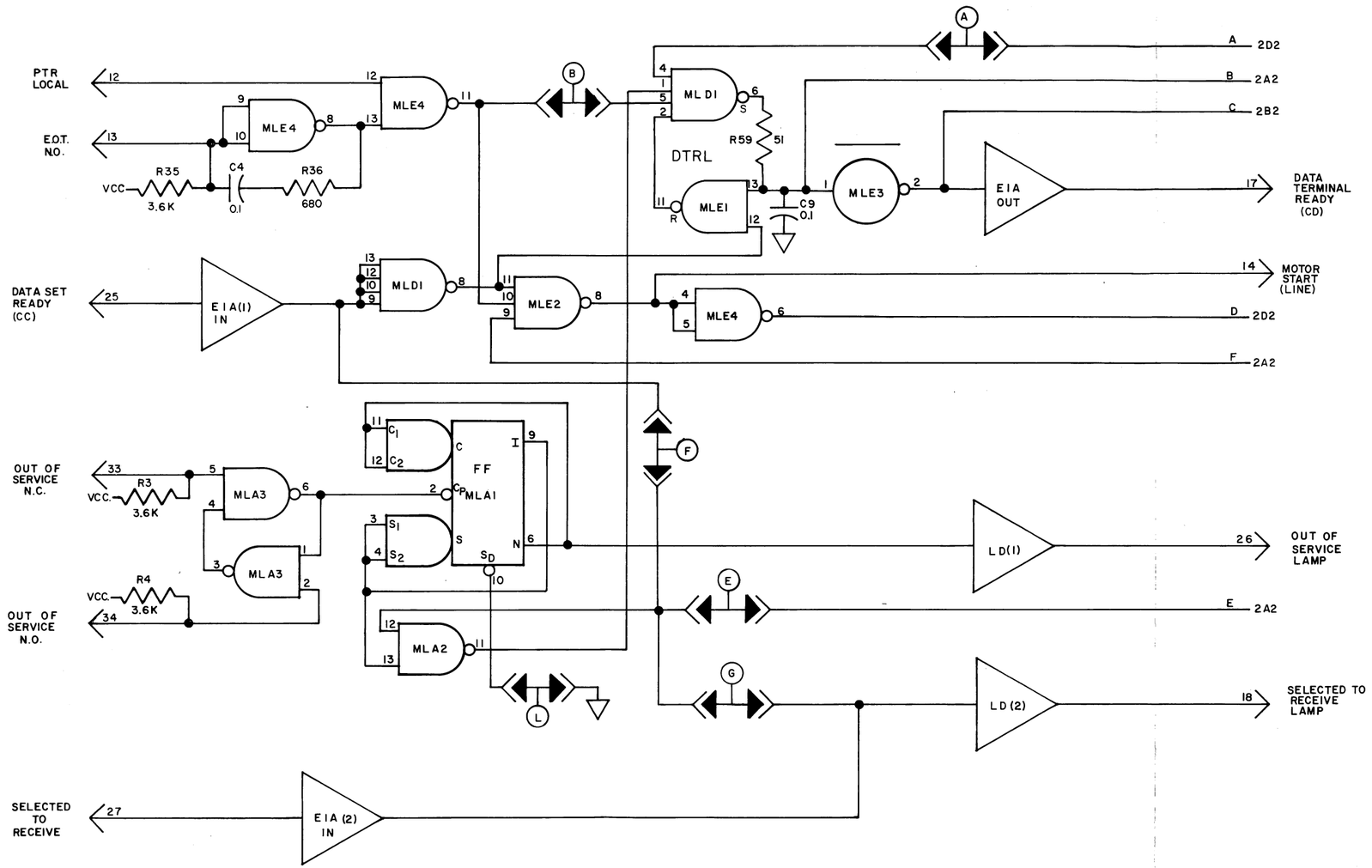
The control character blind is a 13 bit marking interval following the transmission of every control character. This delay is necessary to provide sufficient time for the printer to execute any one of its control functions, before beginning to receive the next character.

A low on Pin B19 inhibits the delay feature on the line distributor. The delay is disabled during all Keyboard transmission, because Answer Back Message Available is high during this time keeping MLB2-6 low. Whenever the Answer Back is sending, Answer Back Message Available is low, enabling the delay by keeping MLB2-6 high.

NO.	NOTES
1.	ALL VOLTAGES DC. UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
4.	INDICATES FEMALE AND INDICATES MALE TERMINALS
5.	REFER TO 322068 FOR ASSEMBLY INFORMATION.
6.	S NUMBER: 61,521S.
7.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD: ML D 2 — ROW, COLUMN, INTEGRATED CIRCUIT
8.	CROSS REFERENCE NOTATION ON SCHEMATIC: 3 B 4 — ROW, COLUMN, SHEET
9.	LOGIC NEGATION: A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
10.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER, THE GATE IS USE AS AN INVERTER.
11.	VCC IS PROVIDED TO THE INTEGRATED CIRCUIT PACKAGE ON PIN 14 AND GROUND ON PIN 7, THIS APPLIES TO ALL PACKAGES.
12.	SEE 8399 WD. FOR TRUTH TABLES.
13.	THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE I-STATE AND O-STATE ARE VCC. AND OV., RESPECTIVELY.
14.	CARD OPTIONS: STRAP MUST BE IN TO OBTAIN OPTION.

STRAP		OPTION
A	—	ALARM DISCONNECT.
B	—	EOT DISCONNECT.
C	—	PRIVATE LINE MOTOR CONTROL DISCONNECT.
D	—	PRIVATE LINE MOTOR CONTROL ENABLE.
E	—	PRIVATE LINE OUT OF SERVICE ENABLE.
F	—	DATAPHONE OUT OF SERVICE ENABLE.
G	—	PRIVATE LINE OUT OF SERVICE ENABLE.
H	—	BREAK DETECT DISABLE.
K	—	SEND BREAK ON PARITY ERROR.
L	—	OUT OF SERVICE DISABLE.
M	—	SEND BREAK DISABLE
Y	—	PROCEED CONTROL DISABLE

15.	REFERENCE CIRCUIT DESCRIPTION. 8388WD-CD.
16.	ABBREVIATIONS USED: MCL - MOTOR CONTROL LATCH. MTL - MARK TIME LATCH. RIL - RECEIVE INTERRUPT LATCH PCL - PROCEED CONTROL LATCH. DTRL - DATA TERMINAL READY LATCH
17.	INDICATES CIRCUIT GROUND.



NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8388WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R
2	11-15-69	99880

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 1 WDP

SCHEMATIC WIRING DIAGRAM FOR CHANNEL CONTROL

APPROVALS

D AND R	E OF M
HJR	

E-NUMBER

PROD. NO. 8388 WD.

DATE 3-29-68

P.D. FILE NO. G-A354AA

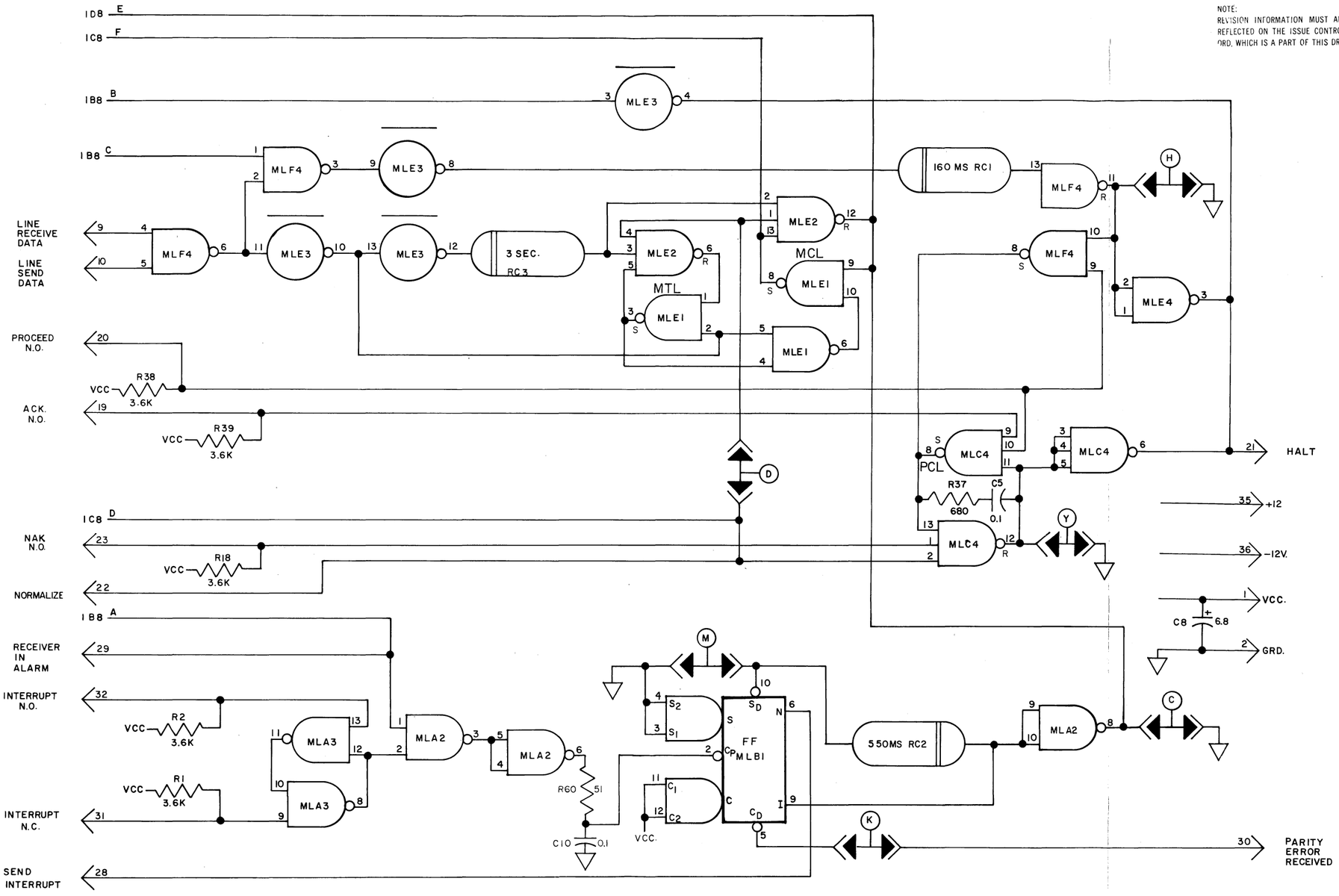
DRAWN W.P.B. CHKD.

ENGD. C.A.Y. APPD.

TELETYPE CORPORATION

8388WD

TC 434 (8-68)



NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING

8388WD

REVISIONS

ISSUE	DATE	AUTH. NO.
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2	2-21-69	96903
3	8-5-69	99359
4	11-15-69	99880

WDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 2

SCHEMATIC WIRING DIAGRAM FOR CHANNEL CONTROL

APPROVALS	
D AND R	E OF M

E-NUMBER

PROD. NO. 8388 WD.

DATE 3-29-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B.	CHKD.
ENGD. C.A.Y.	APPD.

TELETYPE CORPORATION

8388WD

TC 484 (2-69)

8388WD

NOTE
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

REVISIONS

ISSUE	DATE	AUTH. NO.
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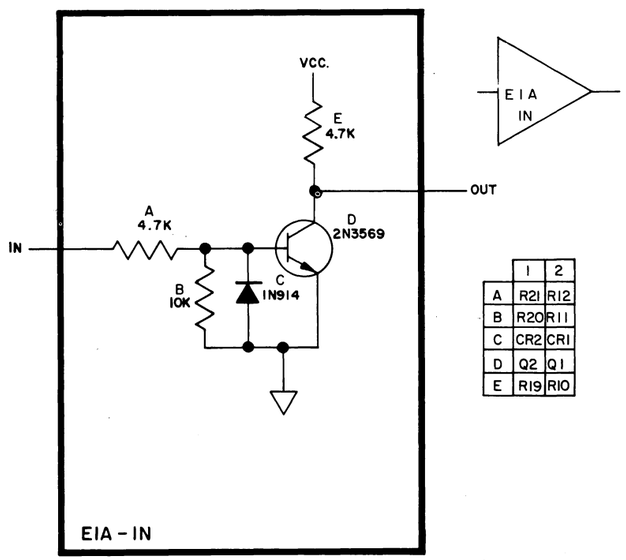
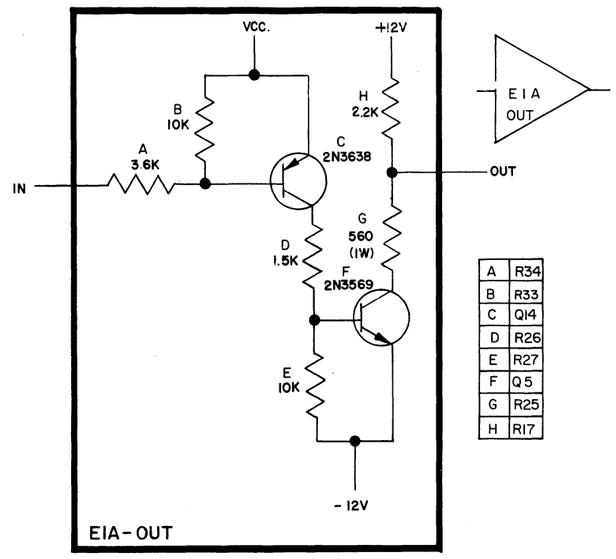
2	8-5-69	99359
3	11-15-69	99880



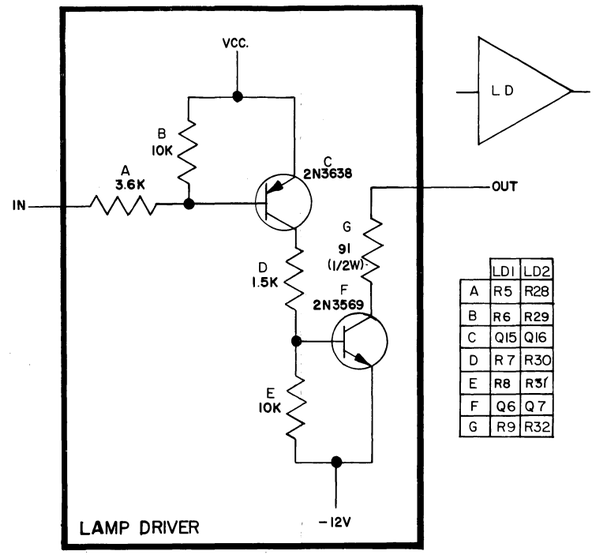
EIA IN

	1	2
A	R21	R12
B	R20	R11
C	CR2	CR1
D	Q2	Q1
E	R19	R10



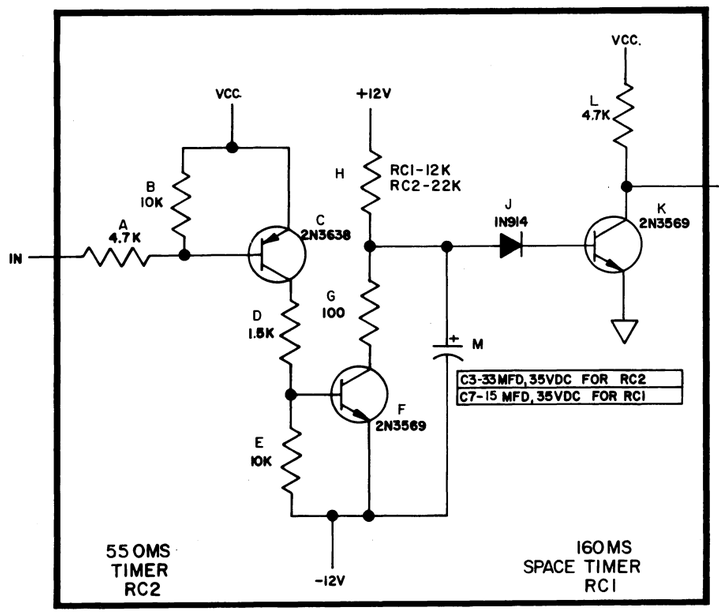
EIA OUT

A	R34
B	R33
C	Q14
D	R26
E	R27
F	Q5
G	R25
H	R17



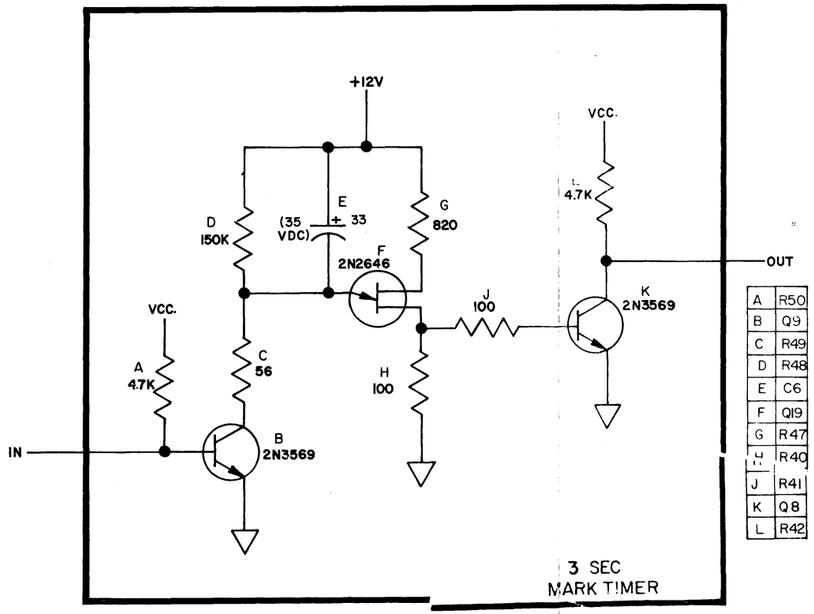
LD

	LD1	LD2
A	R5	R28
B	R6	R29
C	Q15	Q16
D	R7	R30
E	R8	R31
F	Q6	Q7
G	R9	R32



	RC1	RC2
A	R53	R22
B	R51	R24
C	Q17	Q13
D	R45	R15
E	R46	R16
F	Q10	Q3
G	R44	R14
H	R43	R13
J	CR4	CR3
K	Q11	Q4
L	R52	R23
M	C7	C3

3 SEC.
RC 3



A	R50
B	Q9
C	R49
D	R48
E	C6
F	Q19
G	R47
H	R40
J	R41
K	Q8
L	R42

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS WD

SHEET 3 ADP

SCHEMATIC
WIRING DIAGRAM
FOR
CHANNEL
CONTROL

APPROVALS	
D AND R	E OF M

E-NUMBER

PROD. NO. 8388WD.

DATE 1-2-68

P.D. FILE NO. G-A354AA

DRAWN RJP | CHKD.

ENGD. CAY | APPD.

TELETYPE
CORPORATION

8388WD

TC 434 (2-69)

CIRCUIT DESCRIPTION OF THE CHANNEL CONTROL CARD (ASSEMBLY NUMBER 322068)

TABLE OF CONTENTS

NOTE. REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF THE CHANNEL CONTROL CARD (ASSEMBLY NUMBER 322068)

SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The 322068 Circuit Card Assembly provides information to the data set or other line interface unit about the receiving status of the terminal and accepts information about the line connection status of the terminal.

1.2 Additional Features

Timed Send interrupt generation

Timed Receive interrupt detection

On-Line Motor start control for switched or non-switched service

On-Line transmission control

Out of service, do not answer

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

The inputs to the assembly are positive nand type integrated Diode Transistor Logic (DTL) inputs. Each DTL input is approximately a 1.4 ma load to the device sinking current from it. At no time should any of these inputs be more positive than 8 volts or more negative than - .7 volts. Voltage levels represented by the 1-state (high) and 0-state (low) are approximately +6V and 0V respectively. A logic one (high) draws no current from the input of the logic element.

2.1.1 Line Receive Data (Pin 9)

This pin is high when data is not being received or when the signal line is MARKING, and goes low when the signal line is SPACING. Interrupt, a space on line of at least 380 m.s., will appear on this pin.

2.1.2 Line Send Data (Pin 10)

This pin is high when data is not being sent or when a mark is being sent, and will go low when space is sent on line.

2.1.3 Proceed N.O. (Pin 20)

This lead is normally high and goes low when the proceed switch is operated. This low will reset the Proceed Control Latch, (PCL).

2.1.4 ACK N.O. (Pin 19)

This lead is normally high and goes low when an ACK character is detected in the printer function box. This low will reset the Proceed Control Latch (PCL).

2.1.5 NAK N.O. (Pin 23)

This lead is normally high and goes low whenever a NAK character is detected in the printer function box. This low will set the Proceed Control Latch (PCL).

2.1.6 Receiver in Alarm (Pin 29)

This lead is normally high and goes low when a line receiver goes into an alarm condition. A low on Pin 29 starts a SEND INTERRUPT signal and resets the Data Terminal Ready Latch (DTRL).

2.1.7 Interrupt Switch (N.O. Pin 32)(N.C. Pin 31)

These pins accept a break-before-make transfer switch, with the common terminal grounded. Operating the switch starts a send interrupt signal.

2.1.8 Parity Error Received (Pin 30)

A low on this pin starts a send interrupt signal.

2.1.9 Printer Local (Pin 12)

This pin must be made low when the printer function box is "off-line" (local).

2.1.10 EOT N.O. (Pin 13)

This pin must be made low momentarily when the ASCII character EOT is detected by the printer function box.

2.1.11 Data Set Ready (Pin 25) (EIA Lead CC)

The voltage, current, impedance and logic characteristics of this lead are defined by EIA Specification RS232B.

2.1.12 Out of Service Switch (N.O. Pin 34) (N.C. Pin 33)

These pins accept a break-before-make transfer contact with grounded common terminal. Operating the switch turns on the out of service lamp, and causes the line interface unit (e.g. Dataphone Data Set) not to answer any calls.

2.1.13 Selected to Receive (Pin 27)

The voltage, current, and impedance characteristics of this lead are defined by Section 4 of EIA Specification RS232B.

2.1.13 (Continued)

When the lead is "ON", the set will be prepared to receive a message and the "selected to receive" lamp will light.

2.2 Channel Control Outputs

2.2.1 Normalize (Pin 22)

This lead is low when there is no on-line call in process. The lead is used to restore circuits affecting on-line operation to a pre-selected "Normal" state after a call.

2.2.2 Send Interrupt (Pin 28)

This lead goes low for approximately 380 to 750 m.s. when the SEND INTERRUPT circuit is operated.

2.2.3 Halt (Pin 21)

This lead goes low when sending on-line is not permitted.

2.2.4 Selected to Receive Lamp (Pin 18)

See Section I, Paragraph 2.1.13 above.

2.2.5 Out of Service Lamp (Pin 26)

See Section I, Paragraph 2.1.12 above.

2.2.6 Motor Start (Pin 14)

This pin goes low when a call is in process, and is used to start all set motors.

2.2.7 Data Terminal Ready (Pin 17) (EIA Lead CD)

The voltage, current, impedance, and logic characteristics of this lead are defined by EIA Specification RS232B.

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly and Schematic Drawing 322068 (MC068) and 8388WD, respectively.

1.2 Logic symbols and truth tables per 8399WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 MOTOR CONTROL

The MOTOR START lead (Pin 14) low, starts all set motors. The conditions permitting "MOTOR START" are variable by strap option on the channel control card.

Output 8 of MLE2 controls "MOTOR START" and will be low only when Inputs 9, 10 and 11 of MLE2 are high.

MLE2 Input 9 controlled by MCL Section II, Paragraph 2.2.3 below
MLE2 Input 10 controlled by EOT Section II, Paragraph 2.2.2 below
MLE2 Input 11 controlled by DSR Section II, Paragraph 2.2.1 below

2.2 Switched Service Motor Control

In switched service, "MOTOR START" is controlled by "DATA SET READY" Pin 25 (EIA Lead CC). If the set motors are to be stopped or kept from starting by some condition in the terminal, "DATA TERMINAL READY" (Pin 17 - EIA Lead CD) will be turned off. The line interface unit must recognize DTR off as a request for "Disconnect" when DSR is on, and as a request for "DO NOT ANSWER" when DSR is off.

2.2.1 DATA SET READY (DSR) (EIA LEAD CC)

When Pin 25, "DATA SET READY" is high (per EIA Specification RS232B), amplifier A-1 is turned on, holding Inputs 9, 10, 12 and 13 of MLD1 low. Output 8 of MLD1 drives Input 11 of MLE2 high.

If Inputs 9 and 10 of MLE2 are also high, "MOTOR START" (Pin 14) will turn on (low).

Amplifier A-1 output is also connected to Strap F, to control the "OUT OF SERVICE" option. See Section II, Paragraph 3.2.3 below.

2.2.2 End of Transmission (EOT)

Input 10 of MLE2 will be low during the time that "EOT N.O." (Pin 13) is low and "PRINTER LOCAL" (Pin 12) is high. If Strap "B" is installed, the same signal will reset DTRL, turning off "DATA TERMINAL READY" (Pin 17 - EIA Lead CD).

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

2.2.3 Motor Control Latch (MCL)

For switched service, MCL is held reset, by installing Strap C, holding Input 9 of MLE2 high.

2.3 Private Line Motor Control (Non-Switched Service)

In non-switched service, DSR (Pin 25) may be on continuously, indicating that the line interface unit is always ready to operate. The set motors will run continuously.

If this condition is undesirable, the optional idle line motor turn off circuit may be enabled by removing Straps C, F and M, and installing Straps D and E.

2.3.1 Data Set Ready

The line interface unit should keep Data Set Ready (Pin 25) ON continuously, keeping Input 11 of MLE2 high (See Section II, Paragraph 2.2.1 above).

2.3.2 End of Transmission (EOT)

Output 11 of MLE4 will be momentarily low when EOT is detected (See Paragraph 1.12 above). Input 10 of MLE2 will be low, turning off "MOTOR START" (Pin 14) and turning on "NORMALIZE" (Pin 22) through MLE4 Output 6. Strap "D", installed, allows this signal to set MCL and MTL. MCL, Set, holds Input 9 of MLE2 low, keeping "MOTOR START" (Pin 14) off.

2.3.3 Idle Line Turn-Off

Timer E, nominally 3 seconds, sets the MARK TIMER LATCH (MTL) and the MOTOR CONTROL LATCH (MCL) when timed out. MCL, Set, holds Input 9 of MLE2 low, keeping "MOTOR START" (Pin 14) off. Timer E is saved (kept from timing out), by low (Spacing) signals on Pin 9, "LINE RECEIVE DATA", or Pin 10 "LINE SEND DATA". Either of these low inputs will force Output 6 of MLF4 high, Output 10 of MLE3 low, and Output 12 of MLE3 high. (MLE3 Output 12, low, shunts the base of Q9, allowing Timer E to time out. MLE3-12, high, allows Q9 to turn on, with base current through R50. The high state of MLE3 Output 12 will be voltage limited to the base emitter drop of Q9, about 0.6 volts. Measurements to determine the "ON" or "OFF" state of inverter MLE3-12 must be made at MLE3 Input 13).

2.3.3.1 Automatic Motor Turn Off

Uninterrupted marking (high) on line data Pins 9 and 10 for 3 seconds (nominal) allows Timer E to time out, setting MTL and MCL. Input 9 of MLE2 is held low by MCL Set and the motors stop.

2.3.3.2 Re-start from Automatic Stop

2.3.3.2.1 REMOTE Re-Start

A spacing signal (low) on either Pin 9 or Pin 10 resets MTL and saves Timer E. MTL, Reset, places a high on Input 4 of MLE1. When Pin 9 "LINE RECEIVE DATA" and Pin 10 "LINE SEND DATA" are both high, Input 5 of MLE1 will also be high. With Inputs 4 and 5 of MLE1 high, Output 6 of MLE1 will go low, resetting MCL. MCL Reset places a high on Input 9 of MLE2, and the set motors will start.

Since the set motors are not started until the signal line (Pins 9 and 10) is again marking in both directions, the receiving devices at the called terminal will detect a single ASCII "DELETE" character.

2.3.3.2.2 LOCAL Re-Start

The set motors are re-started in an originating terminal by sending INTERRUPT.

When INTERRUPT is sent, (see Section II, Paragraph 5 below) Inputs 9 and 10 of MLA2 are high, forcing Output 8 low, and resetting MCL. MCL Reset places a high on Input 9 of MLE2. If EIA Lead CC (Data Set Ready) is not off, and EOT is not received, the set motors will start. The receivers in the calling terminal do not detect spacing on line when INTERRUPT is sent. No "Hit" characters are generated.

The called station set motors are started on RECEIVE INTERRUPT as described in Section II, Paragraph 2.3.3.2.1 above. Receivers in the called station will detect one ASCII "Delete" character.

3. TERMINAL STATUS (DATA TERMINAL READY)

Data Terminal Ready (Pin 17 - EIA Lead CD) is driven by amplifier B. A low input to amplifier B drives Pin 17 negative, indicating to the line interface unit that the terminal is not ready to operate.

3.1 General

Three optional conditions are available to turn off Data Terminal Ready

Receiver in Alarm	Section II, Paragraph 3.2.1
EOT	Section II, Paragraph 3.2.2
Out of Service	Section II, Paragraph 3.2.3

Any one of these conditions will reset DTRL, placing a high on Input 1, of MLE3, forcing Output 2 of MLE3 and the input of amplifier B low. This turns off Data Terminal Ready. The reset condition must be removed before DTRL can be set. DTRL is set by a low on Output 8 of MLD1, which is low when Data Set Ready, EIA Lead CC, Pin 25 is OFF (Negative on Pin 25).

If Data Set Ready (Pin 25) is on continuously, as in non-switched service, DTRL cannot be set and none of the terminal status options should be used.

3.2. Additional Outputs

DTRL Set output is connected to Input 3 of MLE3 to perform a transmitter control function. See TRANSMITTER CONTROL, Section II, Paragraph 4 below.

Output 2 of MLE3 is connected to Input 1 of MLF4 to inhibit detection of RECEIVED INTERRUPT when Pin 17, Data Terminal Ready, is low.

3.2.1 Receiver in Alarm

RECEIVER IN ALARM (Pin 29) is low when the condition of the line receivers prevents terminal operation, e.g. Paper out etc. See Specification Number 61434 for a description of the conditions on RECEIVER IN ALARM.

Strap A, installed, permits RECEIVER IN ALARM, low, to reset DTRL.

Pin 29, low, also initiates SEND INTERRUPT. See Section II, Paragraph 5 below for a description of the SEND INTERRUPT circuit.

3.2.2 EOT Received On Line (See Section II, Paragraph 2.2.2)

3.2.3 Out of Service

3.2.3.1 General

The Out of Service option allows the operator to disable the terminal. This may be desirable during routine maintenance. (Changing forms, printer ribbons, etc.)

The option is enabled by removing Strap "L", and is operative only when the terminal is idle. The idle condition of the terminal is determined on the basis of strap options depending on the type of service in which the terminal is being used.

3.2.3.2 Operation

The lighted "OUT OF SERVICE" transfer switch is connected to Pins 33 and 34. Cycling the switch produces a single positive to negative transition on the toggle input of the "OUT OF SERVICE" flip-flop, MLA1 Input 2, causing the flip-flop to change state. When Output 6 of MLA1 is low, the "OUT OF SERVICE" lamp will be lighted.

The inverse output of MLA1, Output 9, is connected to Input 13 of MLA2 and will be high when the "OUT OF SERVICE" lamp is lit.

When Input 12 of MLA2 is also high, Output 11 of MLA2 will be forced low, resetting DTRL. DTRL, reset, turns off Data Terminal Ready (Pin 17).

Three straps are provided for optional control of MLA2 Input 12, depending on the type of service in which the terminal is being used.

3.2.3.2 (Continued)

Strap F installed: "OUT OF SERVICE" reset DTRL when "Data Set Ready" EIA lead CC, Pin 25, is off. Used in switched service.

Strap G installed: "OUT OF SERVICE" resets DTRL when "Selected to Receive" Pin 27, is off. Used in some non-switched services.

Strap E installed: "OUT OF SERVICE" resets DTRL when MCL is set. The set motors are stopped when MCL is set. Used with idle line turn off, in non-switched service.

4. TRANSMITTER CONTROL

HALT, Pin 21 is provided to inhibit on line transmission. The signal acts on the send control circuit (8382WD-CD;KSR sets or 8381WD-CD; ASR Sets) to light the "PROCEED" lamp when transmission is permitted.

The "HALT" signal should inhibit all transmitting devices except the answerback. This allows the answerback in a called terminal to generate the character which removes "HALT" (ACK).

"HALT", Pin 21 may be operated by the RECEIVE INTERRUPT circuit; see Section II, Paragraph 6 below.

4.1 "HALT", Pin 21, is controlled by the PROCEED CONTROL LATCH, (PCL). When PCL is set, Inputs 3, 4, and 5 of MLC4 are high and Output 6 is low, holding "HALT", Pin 21, low. PCL, reset, forces MLC4 Output 6 high, but "HALT" Pin 21 may be held low by "RECEIVE INTERRUPT". See Section II, Paragraph 6 below.

4.2 PCL Set (HALT in Effect)

4.2.1 NAK

Detection of the ASCII character NAK causes a contact closure on Pin 23, "NAK N.O.", setting PCL.

4.2.2 NORMALIZE

The "NORMALIZE" output (Pin 22) is derived from the Motor Start lead Pin 14. When Motor Start is high, indicating no MOTOR START, Inputs 4 and 5 of MLE4 are high and Output 6 of MLE4 is low, indicating "NORMALIZE". NORMALIZE sets PCL.

4.2.3 Received interrupt- Detection of interrupt signal sets PCL.

4.3 Proceed Control Latch (PCL) Reset (HALT not in effect)

4.3.1 ACK

Detection of the ASCII character ACK causes a contact closure on Pin 19, "ACK N.O.", resetting PCL.

4.3.2 PROCEED Switch

The normally open PROCEED switch, connected to Pin 20, when operated, resets PCL Operation of the PROCEED switch assumes that "HALT" (Pin 21) will go high.

4.4 PCL Disable

PCL may be held reset by installing Strap Y. This will prevent operation of "HALT" by PCL. Install Strap H to inhibit operation of HALT by RIL.

5. SEND INTERRUPT

The INTERRUPT switch, a break-before-make transfer switch, is connected to Pins 31 and 32. Cycling the switch produces a single positive to negative transition on Input 2 of MLA2. This transition is inverted twice by MLA2-3 and MLA2-6, then integrated by the network C-10 - R60 and applied to the toggle input of MLB1. MLB1 is primed by having "clear" Inputs 11 and 12 connected to Vcc and "Set" Inputs 3 and 4 grounded. This prime causes the negative going transition on Input 2 to drive the Normal output, Output 6, low. Output 6 is connected to Pin 28, send interrupt. Output 9, the inverted output, goes high when Output 6 goes low.

Output 9, high, removes the bias current sink for Q13, which turns off, turning off Q3. Q3 off allows C3 to charge through R16, with a time constant of 730 milliseconds. When the voltage at the anode of CR3 reaches approximately +1.2 volts with respect to ground, Q4 turns on with bias current through R16. The time required to reach turn on will be .806 (730) milliseconds or about 580 milliseconds, nominal.

Q4, turned on, holds Input 10 of MLB1, the set direct input, low. This drives MLB1 Output 6 high, ending the INTERRUPT, and forces MLB1 Output 9 low. This turns on Q13 and Q3, capacitor C3 discharges through R14 and Q3, and Q4 turns off. When Q4 turns off, the low on MLB1, Input 10 is removed, MLB1 remains set, with Output 6 high, and Output 9 low, until another positive to negative transition is detected at MLB1 Input 2.

The SEND INTERRUPT circuit is also triggered, as described above, when "RECEIVER IN ALARM" (Pin 29) is low. For the conditions under which "RECEIVER IN ALARM" is low, see Specification No. 61,434.

6. RECEIVED INTERRUPT

RECEIVED INTERRUPT timer RC1 controls PCL, which can operate "HALT" (Pin 21).

"INTERRUPT" is detected on Pin 9, LINE RECEIVE DATA, and is defined as a continuous Space on Line of more than 380 ms. LINE SEND DATA (Pin 10) must not contain the "SEND INTERRUPT" signal, generated byMLB1 and RC2.

6. (Continued)

Pin 9, "LINE RECEIVE DATA" is low when the received data lead from the line interface unit is spacing. Output 6 of MLF4 will be high, holding Input 2 of MLF4 high. If DTRL is set, indicating that the terminal is ready to operate, Input 1 of MLF4 will also be high, and output 3 of MLF4 will be forced low. This drives Output 8 of MLE3 high, removing the bias current sink for Q17, the input transistor of RC1. Q17 turns off, turning off Q10. Q10 off allows C7 to charge through R43. When the anode of CR4 reaches approximately +1.2V DC with respect to ground, Q11 turns on with bias current through R43.

C-7 charges to +1.2V in approximately .806 (12K ohms)(15 mfd) = 144 ms.

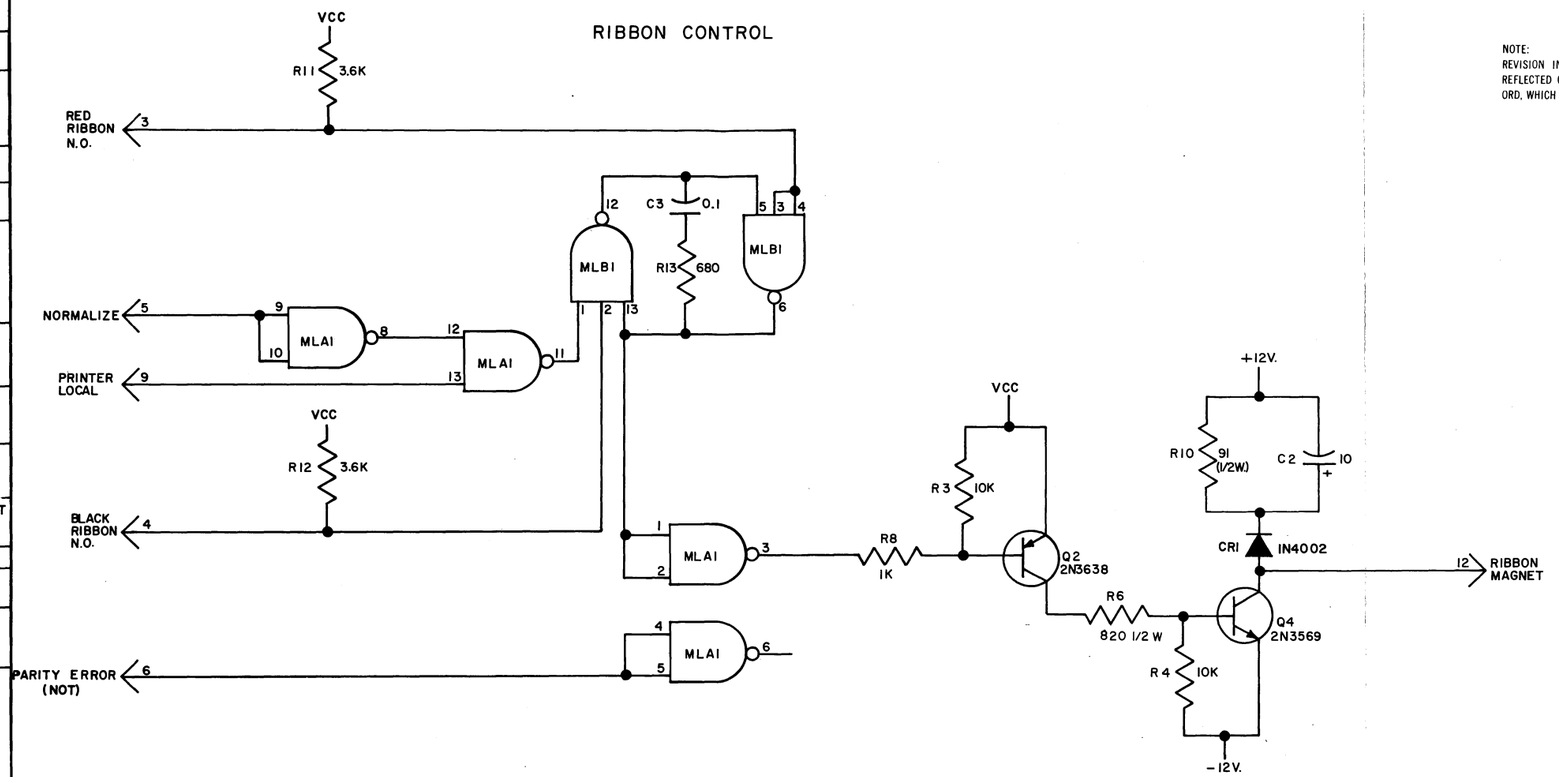
Q11, turned on, sets PCL, forcing "HALT" low.

"HALT", low, should act on the send control card (8381WD-CD) to turn off the "PROCEED" lamp, and inhibit transmission from keyboard (KSR Sets) or keyboard and reader (ASR Sets).

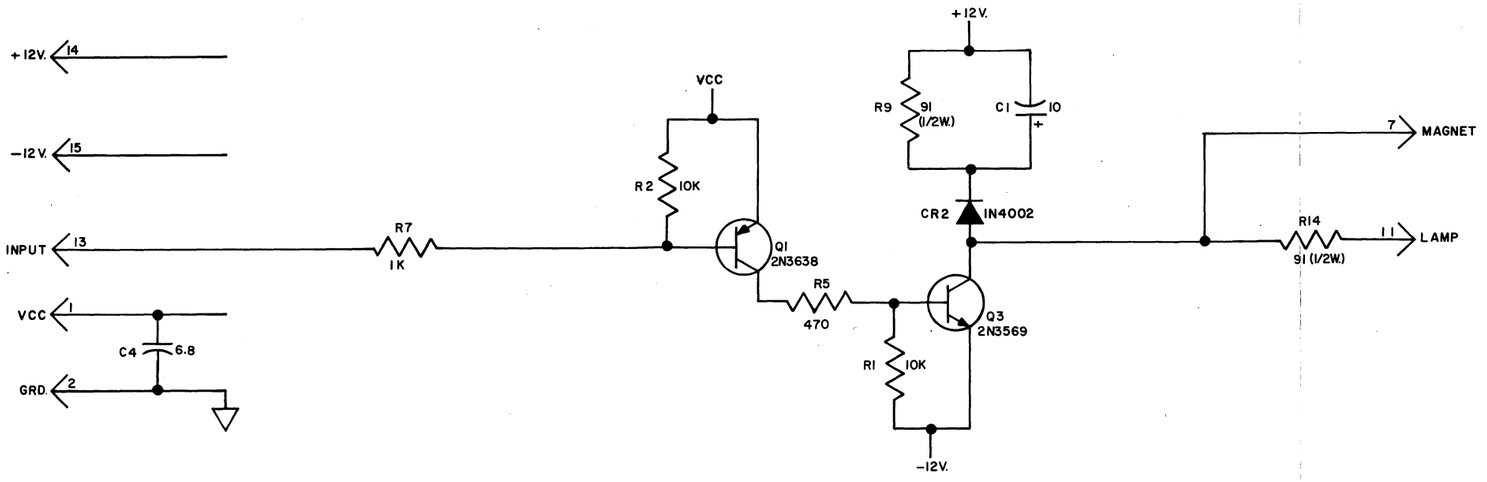
The "RECEIVE INTERRUPT DETECTION" circuit may be disabled by installing Strap H.

NO.	NOTES
1.	ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICRO FARADS UNLESS OTHERWISE SPECIFIED.
4.	INDICATES FEMALE AND INDICATES MALE TERMINAL
5.	REFER TO 322070 FOR ASSEMBLY INFORMATION.
6.	S NUMBER: 61,510 S.
7.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD: ML D 2 — ROW, COLUMN, INTEGRATED CIRCUIT
8.	THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC. AND 0V., RESPECTIVELY.
9.	LOGIC NEGATION - A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
10.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER, THE GATE IS USED AS AN INVERTER.
11.	VCC IS PROVIDED TO THE INTEGRATE CIRCUIT ON PIN 14 AND GROUND ON PIN 7, THIS APPLIES TO ALL PACKAGES.
12.	REFER TO 8399WD FOR TRUTH TABLES.
13.	REFERENCE CIRCUIT DESCRIPTION 8389 WD-CD.
14.	INDICATES CIRCUIT GROUND.

RIBBON CONTROL



AUXILIARY AMPLIFIER



NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8389WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET-1

ADP

SCHEMATIC WIRING DIAGRAM FOR TWO COLOR RIBBON CONTROL

APPROVALS

D AND R	E OF M
11JK	— 1

E-NUMBER

PROD. NO. 8389WD.

DATE 4-19-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. CHKD. RJK

ENGD. R.E.L. APPD. JEH

TELETYPE CORPORATION

8389WD

TC 494 (5-68)

CIRCUIT DESCRIPTION OF THE TWO COLOR RIBBON CONTROL CARD (ASSEMBLY NUMBER 322070)

TABLE OF CONTENTS

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF THE TWO COLOR RIBBON CONTROL CARD (ASSEMBLY NUMBER 322070)

SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The 322070 Two Color Ribbon Control Card performs the function of ribbon color selection (red or black) upon receipt of proper control signals.

1.2 Additional Features

1.2.1 An additional driver is available for application as a solenoid driver or lamp driver. (Optional suggested use would be to light a lamp upon receipt of SHIFT IN or OUT code.)

1.2.2 The ribbon mechanism is reset to black ribbon at the end of a call ("ON-LINE" mode).

1.3 Ribbon Magnet

The ribbon magnet sinks a steady state current of 230 ma DC (nominal) when a logic zero is present on MLA1 Pin 3 and is in the off state when a logic one is present.

1.4 Auxiliary Driver

When operating as a solenoid driver, the DC resistance of the winding must be at least 110 ohms in order to stay within the safe operating area of Q3. If operated as a lamp driver, a 24 volt DC lamp must be used, (recommended lamp Part No. 327061).

1.5 Two-Color Ribbon (Option)

The two-color ribbon control card is an option. It must be provided whenever two-color printing is a terminal requirement. The card plugs into a pre-wired printed circuit card connector and requires no field assembly or adjustment.

2. GENERAL TECHNICAL DATA

2.1 Input-Output Data

2.1.1 The ribbon magnet driver converts the integrated circuit logic inputs to current levels appropriate for ribbon magnet operation.

A logic one is defined as a voltage level between +5.0 volts and +6.6 volts (usually a logic one approximates the integrated circuit supply voltage). A logic one draws no current from the input of the logic element.

Signal voltages between circuit ground potential and +0.5 volts are considered logic zero. Logic currents that flow into the signal source are a function of the element driven, supply voltage, and the value of pull-up resistor used, if any. For additional loading information refer to the manufacturer's specification.

2.2 Input Characteristics

2.2.1 Red Ribbon N.O. (Pin 3)

This input is normally high except during receipt of a red ribbon signal. In Model 37 application, Pin 3 is connected to a N.O. stunt box contact which closes for approximately 20 ms when red printing is desired. The driving source must be capable of sinking approximately two DTL loads. (One DTL load approximately equals 1.4 ma.)

2.2.2 Normalize (Pin 5)

The NORMALIZE input resets the ribbon mechanism to black ribbon when the printer is ON-LINE. This input is high at all times except when a NORMALIZE signal is present. The driving source must be capable of sinking one DTL load.

2.2.3 Printer Local (Pin 9)

This input is low when the printer is operated in the LOCAL mode and high in the ON-LINE mode. The driving source must be capable of sinking one DTL load.

2.2.4 Black Ribbon N.O. (Pin 4)

This input is normally high except during receipt of a BLACK RIBBON signal. In Model 37 application, Pin 4 is connected to a stunt box contact which closes for approximately 20 ms when black printing is desired. The driving source must be capable of sinking one DTL load.

2.2.5 Parity Error Not (Pin 6)

The PARITY ERROR NOT input is low (LOCAL or ON-LINE mode) as long as proper coding exists and high when a parity error exists. The driving source must be capable of sinking one DTL load. THIS CIRCUIT IS PRESENTLY NOT BEING USED.

2.2.6 Input-Auxiliary Driver (Pin 13)

The input characteristics were designed to be compatible with DTL integrated circuit logic elements. A logic one (high) input causes current to flow through the load. A logic zero (low) results in no current flow through the load. The driving source must be capable of sinking approximately three DTL Loads.

2.2.7 Input Ribbon Magnet Driver (MLA1 Pin 3)

Refer to Section I - 2.2.6.

2.3 Output Characteristics

2.3.1 Auxiliary Driver

The auxiliary driver circuit is a two stage amplifier designed to operate full on or full off without intermediate levels. The collector circuit of Q3 contains a transient suppression network consisting of CR2, R9 and C1. When used as a lamp driver, R14 limits lamp surge current to a value within safe operating limits.

2.3.2 Ribbon Magnet

The ribbon magnet driver is a two stage amplifier designed to operate full on or full off without intermediate levels. The collector circuit of Q4 contains a transient suppression network consisting of CR1, R10, and C2. The output circuit is matched to the ribbon magnet assembly. The impedance values of the output circuit have been chosen to provide equal pick-up and drop-out times at some level of ribbon magnet armature spring tension.

2.4 Mechanical Requirements

The 322070 Card Assembly is a standard 15 pin circuit card which is inserted into a 15 pin edge card connector.

2.5 Power Supply Requirements

Vcc (DC)	Current (ma) Max.
+5.0V - +6.6V	125 ma
+11.65V - +13.75V (+12.5V Nom.)	500 ma
-11.[illegible]V to -13.13V (-12.5V Nom.)	500 ma

2.6 Temperature Range

The operating temperature range is from 0°C to 70°C in free air. The storage temperature range is from -40°C to +70°C.

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly and schematic drawings 322070 (MC070) and 8389 WD.

1.2 Logic symbols and truth table 8399 WD.

2. DETAILED DESCRIPTION

2.1 Ribbon Magnet Driver

Assume the printer is "ON-LINE" and a terminal is receiving and printing data in black, (ribbon magnet de-energized). Under these conditions Pins 3, 5, 9, 4 are high, Pin 6 is low, MLA1 Pin 3 is high, MLB1 Pin 13 is low, and MLB1 Pin 12 is high. Assume a "RED RIBBON" bit sequence has been detected by the stunt box and Pin 3 goes low for approximately 20 ms. Latch MLB1 Pin 13 changes states. MLB1 Pin 13 is high, MLB1 Pin 12 is low, and MLA1 Pin 3 is low. A low level (logic zero) input to the ribbon magnet driver causes collector current to flow through R4 and R6. The current flow through R4 results in a positive signal at the base of Q4 (NPN transistor). Q4 is turned full on and the ribbon magnet assembly is energized. The printer now prints the data in red. The ribbon magnet will remain energized until the end of the transmitted message at which time a "NORMALIZE" pulse (low) resets MLB1 (Pin 13 low, Pin 12 high) or a "BLACK RIBBON" bit sequence is detected by the stunt box and Pin 4 goes low for approximately 20 ms.

Assume a "NORMLIZE" pulse (low) has been received on Pin 5. A low on MLA1 Pin 11 resets MLB1 latch (Pin 12 high, Pin 13 low) and MLA1 Pin 3 is now high. Collector current ceases to flow through R4 which results in a negative going pulse at the base of Q4. Q4 is turned off and the ribbon magnet is de-energized. The ribbon magnet assembly has been reset to black printing.

If a "BLACK RIBBON" bit sequence detected by the stunt box causes Pin 4 to go low while printing in red, MLB1 latch is reset (Pin 12 high, Pin 13 low) and MLA1 Pin 3 high. Q4 is now in the "off" state and the ribbon magnet is de-energized. The ribbon magnet assembly has been reset to black printing.

When operating in "LOCAL" mode, Pin 9 is low and MLA1 gate is disabled (MLA1 Pin 11 high). MLB1 latch is now under direct control of the "Red Ribbon" and "Black Ribbon" inputs.

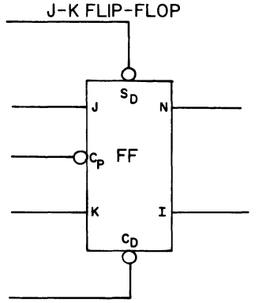
R13 and C3 constitute an RC noise filter. Noise voltages caused by stunt box contact closures or undesirable bounce are integrated so MLB1 latch does not switch to the wrong state.

The transient suppression network consisting of CR1, R10 and C2 dissipates the energy stored in the ribbon magnet winding when Q4 is turned off. This network prevents large inductive voltage spikes from avalanching Q4 collector to emitter.

The two stage auxiliary driver is identical to the ribbon magnet driver. Refer to Section I - 2.2.6 and 2.3.1 for information concerning input and output characteristics, respectively.

NO.	NOTES
1.	GRAPHICAL SYMBOLS AND THE ASSOCIATED TRUTH TABLES ILLUSTRATED ON THIS PAGE ARE TYPICAL SYMBOLS USED IN TELETYPE CORPORATION APPARATUS.
2.	LOGIC NEGATION - A SMALL CIRCLE (O) DRAWN AT THE POINT WHERE A SIGNAL LINE JOINS A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
3.	STATE DESIGNATIONS: 1 - STATE = +6V 0 - STATE = 0V
4.	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER THE GATE IS USED AS AN INVERTER.
5.	ABBREVIATIONS USED: 0 - LOW STATE (MORE NEGATIVE) 1 - HIGH STATE (MORE POSITIVE) X - STATE OF INPUT DOES NOT AFFECT STATE OF CIRCUIT NC - NO CHANGE U - INDETERMINATE STATE N_M - STATE OF N AT TIME M. $\overline{N}_M$ - INVERSION OF STATE OF N AT TIME M.

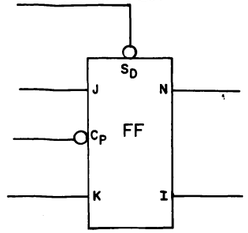
326852
J-K FLIP-FLOP



ASYNCHRONOUS TRUTH TABLE
326852

S_D	C_D	N	I
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

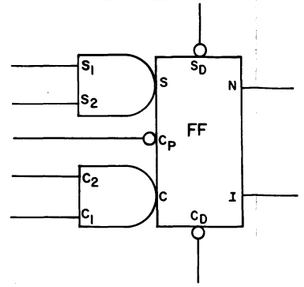
326853
J-K FLIP-FLOP



ASYNCHRONOUS TRUTH TABLE
326853

S_D	N	I
1	NC	NC
0	1	0

326845
CLOCKED FLIP-FLOP



ASYNCHRONOUS TRUTH TABLE
326845

C_D	S_D	N	I
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	1	1

SYNCHRONOUS TRUTH TABLE
326845

S_1	S_2	C_1	C_2	N
0	X	0	X	NC
0	X	X	0	NC
X	0	0	X	NC
X	0	X	0	NC
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

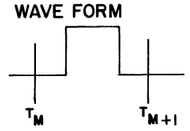
J-K TRUTH TABLES
(CONNECT S_2 TO I, C_2 TO N)

T_M		T_{M+1}
S_1	C_1	N
0	0	N_M
1	0	1
0	1	0
1	1	$\overline{N}_M$

J-K TRUTH TABLE
BOTH TYPES

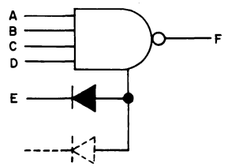
T_M		T_{M+1}
J	K	N
0	0	N_M
1	0	1
0	1	0
1	1	$\overline{N}_M$

CLOCKED PULSE WAVE FORM



ASYNCHRONOUS INPUTS, DIRECT SET (S_D) AND DIRECT CLEAR (C_D), OVERRIDE THE SYNCHRONOUS INPUTS. THEY ARE INDEPENDENT OF ALL OTHER INPUTS.

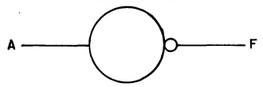
NAND GATE



A	B	C	D	E	F
1	1	1	1	1	0
1	0	0	0	0	1
0	0	0	0	0	1
0	1	1	1	1	1

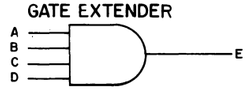
A, B, C, D OR E LOW (0) CAUSES F TO GO HIGH (1)

INVERTER



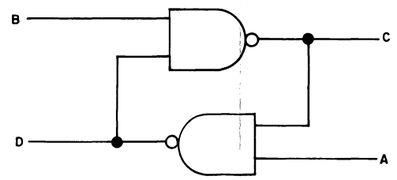
A	F
0	1
1	0

GATE EXTENDER



$E = A \cdot B \cdot C \cdot D$

SET-RESET FLIP-FLOP
UTILIZING NAND GATES



A	B	C	D
0	0	1	1
0	1	0	1
1	0	1	0
1	1	NC	NC

8399 WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	5-3-68	19208-R

LOGIC SYMBOLS AND TRUTH TABLES

APPROVALS

D AND R	E OF M

E-NUMBER

PROD. NO. 8399WD

DATE 2-12-68

P.D. FILE NO. G-A354AA

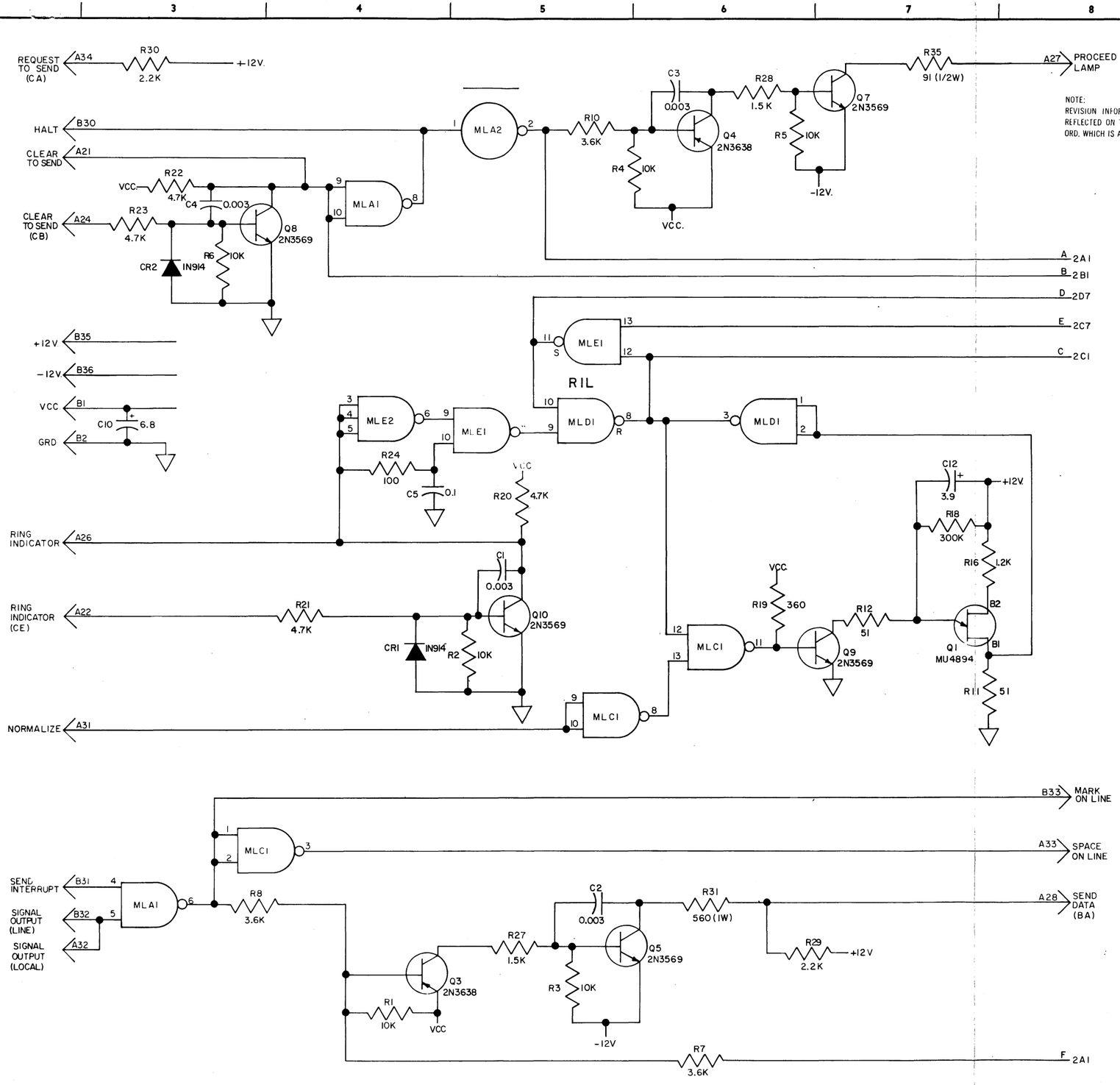
DRAWN RJP | CHKD.

ENGD. MJR | APPD.

TELETYPE CORPORATION

8399 WD

NO.	NOTES
1.	REFER TO 322304 FOR ASSEMBLY INFORMATION.
2.	S-NUMBER-61,618S.
3.	ALL RESISTORS 1/4 WATT, AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
4.	ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
5.	ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
6.	INTEGRATED CIRCUIT PACKAGE LOCATION ON CIRCUIT BOARD. ML B 2 ROW COLUMN INTEGRATED CIRCUIT
7.	CROSS REFERENCE NOTATIONS ON SCHEMATIC. 2 A 2 ROW COLUMN SHEET
8.	LOGIC NEGATION- A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
9	STATE DESIGNATIONS: 1- STATE = VCC. 0- STATE = 0V.
10.	REFER TO 8399 WD FOR TRUTH TABLES.
11	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER THE GATE IS USED AS AN INVERTER.
12	VCC IS PROVIDED TO THE INTEGRATED CIRCUIT ON PIN 14, AND GROUND ON PIN 7. THIS APPLIES TO ALL PACKAGES.
13	REFERENCE CIRCUIT DESCRIPTION 8773WD-CD.
14.	ABBREVIATIONS USED: RIL - RING INDICATOR LATCH CNL - CONTENTION LATCH CSL - CHARACTER SENT LATCH.
15.	ORIGINALLY KSR SEND CONTROL.



NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8773WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	11-21-68	19778R
2	2-5-70	99993

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 1 - NOTE 15 WDP

R.O. AND KSR SEND CONTROL

APPROVALS

D AND R	E OF M

E-NUMBER

PROD. NO. 8773WD

DATE 9-30-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. CHKD.

ENGD. C.A.Y. APPD.

TELETYPE CORPORATION

8773WD

TC 434 (12-68)

SEE SHEET 1 FOR NOTES.

NOTE
ANY CHANGE IN INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD WHICH IS A PART OF THIS DRAWING.

8773 WD

REVISIONS

ISSUE	DATE	AUTH. NO.
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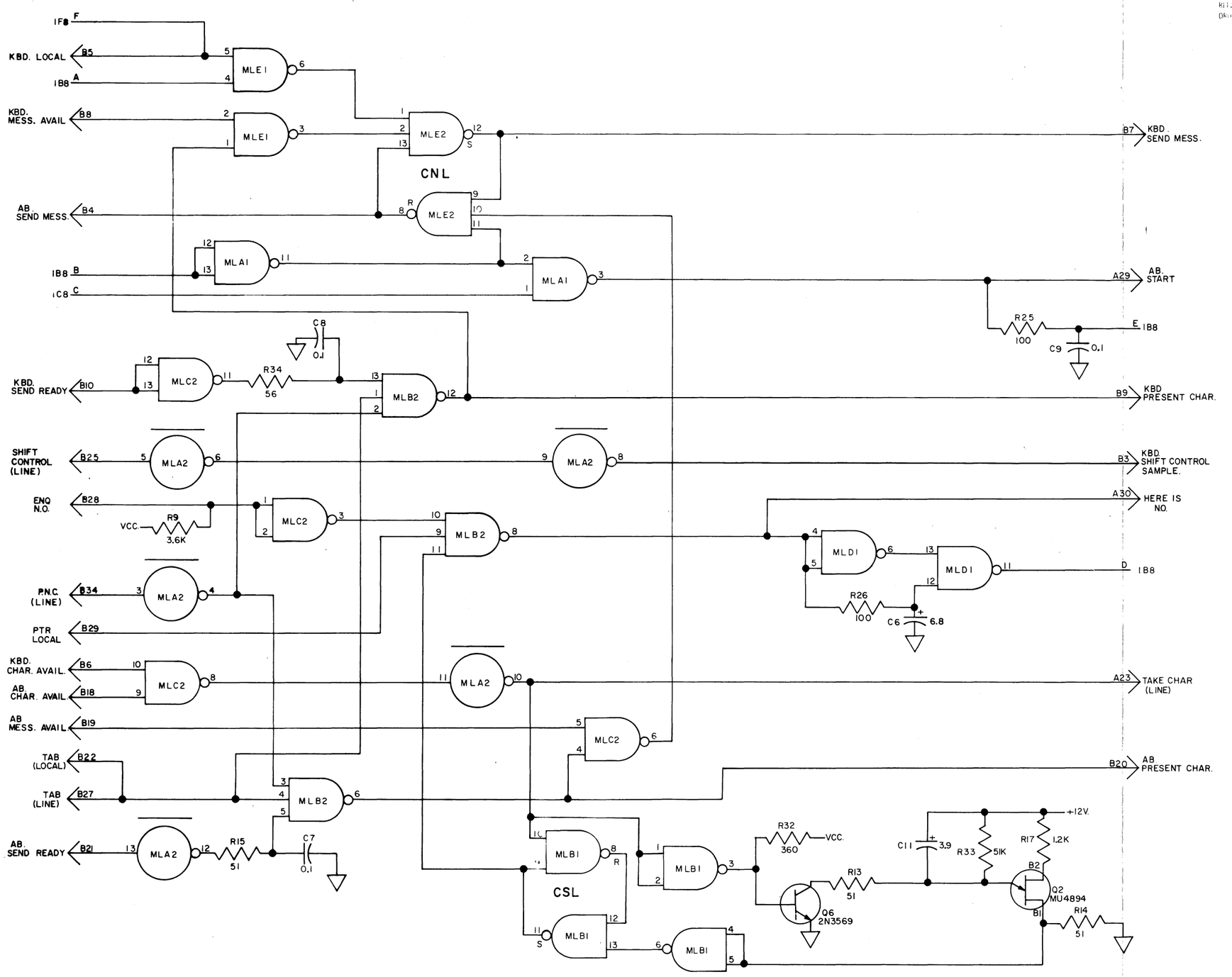
2	11-15-69	99880
3	2-5-70	99993



SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS WD

SHEET 2

WDP

R.O AND KSR SEND CONTROL

APPROVALS	
D AND R	E OF M

E-NUMBER

PROD. NO. 8773 WD

DATE 9-30-68

P.D. FILE NO. G-A354AA

DRAWN W P B | CHKD.

ENGD. C A Y | APPD.

TELETYPE CORPORATION

8773 WD

TC 484 (5-68)

WDP

CIRCUIT DESCRIPTION OF THE R.O. AND KSR CONTROL CARD (ASSEMBLY NUMBER 322304)

TABLE OF CONTENTS

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF THE R.O. AND KSR SEND CONTROL CARD (ASSEMBLY NUMBER 322304)

WDP

SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The basic function of the 322304 R.O. and KSR Send Control Card is to coordinate two sending devices, which are the Keyboard and Answer Back, for operation in conjunction with a transmitting distributor.

1.2 Each device works into the logic through a peripheral interface consisting of five leads. These are:

1.2.1 Message Available

When the lead is in the 0-state (low) the device is indicating to the Send Control, that it is capable of sending a message.

1.2.2 Send Message

This lead, in the 0-state, is an indication from the Send Control to the device that it was successful in obtaining sending priority.

1.2.3 Send Ready

A "low" on this lead tells the Send Control that the device is ready to start sending a message. This means that any or all functions necessary, before the device can begin sending, have been performed.

1.2.4 Present Character

When this lead is in the 0-state, the distributor is indicating to the device via the Send Control that its shift register is empty and is capable of accepting a character for distribution.

1.2.5 Character Available

This lead in the 0-state is an indication from the device to the distributor via the Send Control that a character is ready for distribution and the distributor should commence its distribution cycle.

1.3 A contention Latch (CNL) assigns sending priority to that device which first presents a Message Available indication.

1.4 There are three possible modes of operation.

1.4.1 KBD Sending "local". (KSR Only)

1.4.2 KBD Sending "on-line". (KSR Only)

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1.4.3 Answer Back Sending "on-line".

WDP

1.5 This assembly provides three methods of starting the Answer Back. These are:

1.5.1 Manual Start

1.5.2 Stunt Box Operated Start

1.5.3 Automatic Start (On Line Handshake)

1.6 This assembly provides the serial EIA Signal output to the line interface unit.

1.7 This assembly contains the Proceed Lamp driver.

2. Input Characteristics

2.1 The inputs to the circuit assembly are either EIA (RS-232-B) or Nand type integrated Diode Transistor Logic (DTL) inputs. EIA inputs are defined in Electronic Industries Association Standard RS-232-B. Each DTL input is approximately 1.4 ma load to the device sinking current crom it. At no time should any of these inputs be more positive than +6.6 volts or more negative than -.7 volts. Voltage levels represented by the 1-state (high) and 0-state (low) are approximately +6V and 0V respectively. A logic one (high) draws no current from the input of the logic element.

2.1.1 Keyboard Message Available (Pin B8) - (KSR Only)

This input when in the 0-state (low), is an indication from the Keyboard to the Send Control that the Keyboard is capable of sending a character. The device driving this input must be capable of sinking one DTL load.

2.1.2 Keyboard Send Ready (Pin B10) - (KSR Only)

A low on this input tells the Send Control that the Keyboard is ready to start sending a character. This lead is a turn-around of the Keyboard Send Message output (Pin B7) through the Keyboard interface card. The device driving this input must be capable of sinking one DTL load.

2.1.3 Keyboard Character Available (Pin B6) - (KSR Only)

When this input is low, the Keyboard is indicating to the distributor via the Send Control that a character is ready for distribution, and the distributor should start its distribution cycle. During normal operation this input will be low for 1 bit time before the start bit of each character. The device driving this input must be capable of sinking one DTL load.

2.1.4 Line Shift Control Sample (Pin B25) - (KSR Only)

This input is normally high and goes low .25 bits after the Keyboard Character Available goes low and remains low for .25 bits. The device driving this input must be capable of sinking one DTL load.

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2.1.5 Present Next Character (Pin B34) - KSR Only

This input, low in the idle state, is an indication to the Send Control that the distributor's shift register is empty and capable of accepting a character for distribution. It goes high at the beginning of the start bit of each character and remains high for the duration of the character. The device driving this input must be capable of sinking one DTL load.

2.1.6 Line Tabulation (Pin B27)

This input is low throughout any tabulation function of the printer while it is "on-line" and high at all other times. It serves to inhibit "on-line" transmission during tabulation. The device driving this input must be capable of sinking two DTL loads.

2.1.7 Local Tabulation (Pin B22)

This input is low throughout any tabulation function of the printer while it is off-line (local), and high at all other times. It serves to inhibit local transmission during tabulation. The device driving this input must be capable of sinking two DTL loads.

2.1.8 Send Interrupt (Pin B31)

This input is normally high and goes low (spacing) whenever an interrupt is generated. The device driving this input must be capable of sinking one DTL load.

2.1.9 Signal Output (Line) (Pin B32)

This input is the serial signal output of the distributor during "on-line" transmission. It is high for a MARK and low for a SPACE. The device driving this input must be capable of sinking one DTL load plus the loads required for local Signal Output (Pin A32).

2.1.10 Printer Local (Pin B29)

This input inhibits the answer back from starting if the Printer receives the ENQ character, while in the local mode. It is high in the "on-line" mode and low in the "local" mode. The device driving this input must be capable of sinking the one DTL load.

2.1.11 Normalize (Pin A31)

This input is high while the printer motor is running "on-line" and is used to disable the two-second Ring Indicator timer. Normalize low enables the timer. The device driving this input must be capable of sinking one DTL load.

2.1.12 Ring Indicator (CE) (EIA) (Pin A22)

This input is normally low (0 to -25V) and goes high (+3V to +25V) every time the bell in the data set rings. It is used to condition the answer back's automatic start circuit (RIL).

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SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

WDP

2.1.13 ENQ (S.B.) (Pin B28)

This input is normally high. It is switched low for a nominal period of 20 ms everytime the Printer receives the ENQ control character. The device driving this input must be capable of sinking one DTL load.

2.1.14 Here Is (Pin A30)

This input is normally high. Any negative transition on this input causes the answer back to start.

2.1.15 Answer Back Message Available (Pin B19)

This input behaves in the same manner as KBD MA (See Section I-2.1.1). It switches low at the beginning of a message and remains low for the entire duration of a message.

2.1.16 Answer Back Send Ready (Pin B21)

This input behaves in the same manner as KBD Send Ready (See Section I-2.1.2). It switches low at the beginning of a message and remains low for the entire duration of a message.

2.1.17 Answer Back Character Available (Pin B18)

This input behaves in the same manner as KBD Character Available (See Section I-2.1.3). It switches low at the beginning of a message and remains low for the entire duration of a message.

2.1.18 Keyboard Local (Pin B5) - (KSR Only)

This input conditions the Send Control for "line" or "local" operation of the keyboard. It is high if the KBD has been selected to send "on-line" and low if it has been selected to send locally. It inhibits locally generated data from being sent "on-line". The device driving this input must be capable of sinking two DTL loads.

2.1.19 Clear to Send (CB) (EIA) (Pin A24)

When this EIA input is high (+3V to +25V), it enables the Keyboard or Answer Back for "on-line" operation. If it is low (OV to -25V), the Contention Latch (CNL) is disabled and neither Keyboard nor Answer Back is able to operate "on-line".

2.1.20 Halt (Pin B30)

This input must be high during the time that Clear to Send is high to enable the Keyboard to send "on-line". If this input goes low and remains low during the time that the Keyboard is sending "on-line", Keyboard transmission will immediately stop. It has no effect on Answer Back operation. The device driving this input must be capable of sinking two DTL loads.

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2.2 Output Characteristics

The output from this assembly are either EIA (RS-232-B), Diode Transistor Logic (DTL), or transistor driver outputs. EIA outputs are defined in Electronic Industries Association Standard RS-232-B. DTL outputs are rated according to the number of DTL loads each can sink. Each load is approximately 1.4 ma.

2.2.1 Keyboard Send Message (Pin B7) - (KSR Only)

This output in the O-state is an indication from the Send Control to the Keyboard, that it was successful in obtaining sending priority. This output switches low at the beginning of each character, and is capable of sinking eight DTL loads.

2.2.2 Keyboard Present Character (Pin B9) - (KSR Only)

This output, when in the O-state, is an indication to the Keyboard that the distributor's shift register is empty and capable of accepting a character for distribution. KBD Message Available, Send Message, and Send Ready, must all be low and as long as they remain such, this output will be under the control of the Present Next Character output of the distributor. This output will sink seven DTL loads.

2.2.3 Keyboard Shift Control Sample (SCS) (Pin B3) - (KSR Only)

This output is normally high and goes low for -.25 bits after Keyboard Present Character has gone low. This output will sink eight DTL loads.

2.2.4 Line Take Character (Pin A23)

When this output switches to the O-state, the command is from the Send Control to the distributor to commence its distribution cycle. This output switches low for one bit time before the beginning of the start bit of each character and remains low for one bit time. This output will sink eight DTL loads.

2.2.5 Send Data (EIA) (Pin A28)

This output is the serial EIA data signal. It is marking when the voltage is between OV to -25V and spacing when it is between +3V to +25V.

2.2.6 Space On-Line (Pin A33)

This input is normally high (marking) and goes low whenever a spacing bit is generated "on-line" or "local". This output will sink eight DTL loads.

2.2.7 Mark On-Line (Pin B33)

This output is the inverse of Space On-Line (See Section I-2.2.6). This output will sink seven DTL loads.

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2.2.8 Request to Send (EIA) (Pin A34)

This EIA output is held high +3V to +25V continuously, indicating a continuous request to send to the Data Set.

2.2.9 Answer Back Start (Pin A29)

This output switching from high to low is the Answer Back start command. This output will sink seven DTL loads.

2.2.10 Answer Back Send Message (Pin B4)

This output behaves in the same manner as KBD Send Message (See Section I-2.2.1) except that it switches low at the beginning of a message and remains low for the entire duration of a message.

2.2.11 Answer Back Present Character (Pin B20)

This output behaves in the same manner as KBD Present Character (See Section I-2.2.2).

2.2.12 Proceed Lamp (Pin A27)

This output drives the Proceed Lamp located on the control strip. When this output is "on" it provides power to light the lamp indicating that the set is ready to commence sending "on-line".

2.2.13 Signal Output (Local) (Pin A32)

This output is the serial signal output from the distributor and is used for off-line (local) operation of the KSR Set. This output is driven by the distributor and has no load current sinking capability of its own.

2.2.14 Ring Indicator (Pin A26)

This output normally high, is the inverse of the EIA (CE) Ring Indicator signal on Pin A22. Data sets using a pulsed Ring Indicator will cause this lead to switch low for approximately one second, everytime the bell in the hand set rings. Data sets utilizing a continuous Ring Indicator, will cause this lead to switch low at the beginning of a call, and to remain low until the end of that call.

2.2.15 Clear to Send (Pin A21)

This output, normally high, is the inverse of the EIA (CB) Clear to Send signal on Pin A24. This output switching low at the start of a call and remaining low throughout the entire duration of a call enables on line transmission.

2.3 Mechanical Requirements

The R.O. and KSR Send Control is a 5-3/4 x 4-1/4 inch 72-pin circuit card designed to mate with a standard 72-pin connector.

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2.4 Power Supply Requirements

Pin	VDC	Current Maximum
B1	+5.0V to +6.6V (+5.25V Nom.)	
B2	Circuit Ground	
B35	+11.65V to +13.75V (+12.5V Nom.)	
B36	-11.13V to -13.88V (-12.5V Nom.)	

2.5 Temperature Range

The ambient operating temperature range is from 0°C to 70°C. Storage temperature range is from -40°C to +70°C.

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SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly and Schematic drawing 322304 (MC304) and 8773WD respectively.

1.2 Logic symbols and truth table 8399WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 General

Refer to the 8773WD schematic and attached timing diagrams as an aid to understanding the following description.

2.2 Keyboard Local Operation - (KSR Only)

The signal exchange between the Keyboard, Send Control and Distributor occurs in the following manner. Assume that the KSR Set has been selected to operate in the local mode. Pins B5 and B29 are both low. This forces the MLE2-1 input to the Contention Latch (CNL) high. With no Clear to Send present, the MLA1-11 output is low, keeping the Reset side of the latch high, inhibiting local operation of the Answer Back (Answer Back Send Message high).

The KBD Message Available, MLE2-2, input to CNL is low. Depressing a key on the Keyboard causes KBD M.A. (Pin B8) to switch low, forcing MLE2-2 to go high. Since all RESET inputs to the Contention Latch (CNL) are now high, the latch is SET and will indicate KBD Send Message (Pin B7 low). KBD Send Message, connected to KBD Send Rea y (Pin B10), via the KBD interface circuit card, forces the MLB2-13 input high. MLB2 inputs 1 and 2 both high, indicatethat no tabulation function is in process and that the distributor's shift register is empty and ready to accept a character for distribution. Consequently, since all inputs to MLB2-12 are high, KBD Present Character (Pin B9) will switch low, forcing MLE1-3 to remain high even if KBD Message Available should revert high, thereby keeping the KBD Send Message output low until the CNL is RESET.

A KBD Character Available indication received from the KBD on Pin B6 causes KBD Take Character (Pin A23) to go low. Take Character low causes the distributor to start its distribution cycle. One bit time later, the distributor will remove PNC (Pin B34 high) indicating that the character has been taken. PNC remains high until the character has been shifted out of the distributor's shift register, at which time it will revert low and wait for the beginning of the next character.

PNC going high causes MLB2-2 to go low, forcing KBD Present Character high enabling MLE1-3 to revert low at the end of the KBD message available indication. The KBD Present Character output is returned

to the KBD Character Available input (Pin B6 goes high) via the keyboard interface card and if Answer Back Character Available (Pin B18) is also high, the Take Character output (Pin A23) will switch high, thus preventing the distributor from starting another cycle.

Shift Control Sample (Pin B25) is an input coming from the distributor (low for .25 bit, .25 bits after Take Character has switched low) which is routed to the Keyboard interface card by way of MLA2-6 and 8 and output Pin B3 (KBD Shift Control Sample).

2.3 On-Line Operation - (KSR Only)

The signal exchange between the Keyboard, Send Control and Distributor during "on-line" operation is the same as that previously discussed for "local" operation. In this case, either the Keyboard or Answer Back is able to send on-line provided that MLA1-11 is high (CTS present) and MLE1-6 is high (Proceed indication from MLA2-2 low). There is no local mode for the Answer Back and it will receive an AB Send Message (Pin B4) whenever all inputs to MLE2-8 are high. If CTS is not present, the Contention Latch (CNL) will be disabled, due to lows on MLE2-11 and MLE2-1, and neither KBD nor Answer Back will be able to transmit "on-line". A Halt indication (Pin B30 low) will stop "on-line" transmission from the Keyboard by preventing KBD Send Message from switching low during the entire time the Halt indication is present. The MLA2-2 and MLE1-6 gates which force a low at the MLE2-1 input to the Contention Latch (CNL) during a Halt indication do not affect "on-line" operation of the Answer Back because the MLE2-11 input to the latch remains high as long as a CTS indication is present.

With the Keyboard "on-line" (Pin B5 high), Clear to Send present (+EIA), and no Halt indication (Pin B30 high), all inputs to the Contention Latch (CNL), except the two inputs coming from the MA gates (MLE1-3, MLC2-6) will be high. In this condition the set and reset sides of the CNL Latch are both high and ready for a Message available signal from either the Answer Back or Keyboard. If KBD Message Available occurs, first, the Keyboard has control and an Answer Back Message Available on MLE2-10 cannot affect the present state of the latch until KBD Send Message reverts high. If the Answer Back had sent the first Message Availa le, the KBD Send Message would have been disabled (MLE2-13 low) until Answer Back Send Message returned high.

2.4 Transmitter Stop

During tabulation, Line Tab (Pin B27) switching low at any time during the course of an "on-line" message, indicates that a Printer tabulation function is in process and will stop the line transmitter while it is low, by disabling the Present Character to the Keyboard or Answer Back by means of either input MLB2-1 or MLB2-4 respectively. A local tabulation indication (low) on Pin B22 performs the same function of stopping the KBD during local operation (Answer Back is never allowed to operate in the "off-line" mode).

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2.5 Answer Back Start Logic

The Answer Back can be started in any one of three ways, taking the first step of its cycle when a high to low transition appears on Pin A29.

2.5.1 Manual Start

The Answer Back is started manually by depressing the "Here Is," Switch located on the control panel. This action due to gates MLD1-6, MLD1-11 and components R26 and C6 is transformed into an approximately 1 millisecond long negative pulse into the set side of the Ring Indicator latch (RIL), setting the reset side of the latch high. The reset side of the RIL latch gated together with the CTS signal, which is a high on MLA1-3. This negative pulse, used to trip off the Answer Back, is formed by the RIL latch being reset approximately 1 milliseconds after it was set.

2.5.2 Stunt Box Operated Start

The Answer Back can also be started by operation of the Printer ENQ stunt box contact. For this to occur the Printer must be in the "on-line" mode, MLB2-9 input high, and the Line TC must be idle (no "on-line" transmission in process) keeping the MLB2-11 input high. Should the Printer now receive the ENQ character, the ENQ contact will close for approximately 20 ms forcing the MLB2-10 input high via MLC2-3, making the MLB2-8 output low, thereby starting the Answer Back.

The purpose of gating the set side of the Character Sent latch (CSL) with the inverse of the ENQ stunt box closure, is to prevent starting one's own Answer Back whenever the ENQ character is sent on line. This is accomplished by Line TC setting the set side of the CSL latch low for a period of 250 milliseconds from the beginning of the start bit of the ENQ character. The stunt box closure occuring 14 to 15 bits after the negative transition of the start bit is unable to cause MLB2-8 to go low, because the MLB2-11 input is keeping it high. The 250 millisecond time interval is the period of the CSL Reset timer, whicn resets the CSL latch at the end of its cycle.

2.5.3 Automatic Start

The Answer Back automatic start logic consists of the Ring Indicator latch (RIL) formed by MLD1-8 and MLE1-11, which is controlled by RI and the RIL Reset Timer. The circuit functions in the following manner. In the OFF state RI (CE), normalize and CTS (CB) are all low. The timer is not running and the RIL latch is reset keeping MLA1-3 high. RI (CE) going high starts the timer by switching the reset side of the RIL latch high. MLA1-3 remains high because CTS (CB) is still low at this time, keeping MLA1-2 low by way of MLA1-11. Normalize must switch high within 2 seconds after RI (CE) switched high for the RIL latch to remain in its present state. If normalize does not switch high within the specified time, the RIL reset timer will run its full 2 second cycle resetting the RIL latch, thereby preventing the CTS (CB) signal from starting the Answer Back.

WDP

2.5.3 (Continued)

Assume the RIL latch remains set. CTS (CB) switching high results in a negative pulse at MLA1-3. This negative pulse which starts the Answer Back is formed by the RIL latch being reset approximately 10 microseconds after CTS (CB) switched high. The 10 microsecond delay on reset is accomplished by the integrating network consisting of R25 and C9.

2.6 RIL and CSL Reset Timers

These timers are conventional unijunction (UJT) relaxation oscillators, with periods of 2 seconds and 250 milliseconds respectively.

The RIL Reset Timer functions in the following manner. Whenever MLC1-11 is high, transistor Q9 is on and capacitor C12 is charged to +12.5V holding the emitter of the UJT at ground potential. MLC1-11 switching low, turns off transistor Q9, which in turn allows C12 to discharge through R18 causing the voltage at the emitter of the UJT to rise exponentially toward +12.5V. When this voltage reaches a value VP (characteristic of the UJT $Vp = n\ V_{BB} + V_D$) the UJT will fire and the C12 charging current through R11 will produce a positive spike at B1 of the UJT. This spike is inverted by MLD1-3, resetting the RIL latch, forcing MLC1-11 high thereby disabling the timer.

The CSL Reset Timer functions in exactly the same manner in conjunction with the Character Send Latch (CSL). The only difference is in the values of C11 and R33 which establish the desired time constant.

2.7 EIA Input Amplifiers

EIA input amplifiers, such as those which route RI and CTS onto the card, are common emitter amplifiers which convert EIA voltages ranging from +3 to +25V volts to a DTL low (0 volts) and EIA voltages ranging from 0 to -25 volts to a DTL high (+Vcc). Thus there is a logic inversion when a signal passes through an EIA input amplifier (an EIA high is a DTL low and an EIA low is a DTL high). In the EIA RI amplifier, R21 is a base current limiting resistor, which presents an input impedance of 4.7K ohm to the device driving this input. Diode CR1 prevents an excessive BV_{EB} from damaging Q10. R2 reduces the effects of collector to base leakage and improves switching time. R20 is the collector load resistor.

2.8 Line Data Amplifier (EIA)

The serial signal output of the distributor, which is high for a MARK and low for a SPACE, is monitored by Pins A32 and B32. MLA1-6 inverts this signal, before it is used, to drive the EIA Signal output amplifier, consisting of Q3 and Q5. The amplifier output on Pin A28 is an EIA voltage as described in EIA Standard RS-232-B. It is low (0 to -25V) for a MARK and high (+3V to +25V) for a SPACE. The other input (Pin B31) to MLA1-6, monitors the Send Interrupt signal, which is a nominal 250 ms of continuous space. MLC1-3 inverts the signal input to the EIA output amp. Its output on Pin A33 is an exact duplication of either signal input to MLA1-6.

WDP

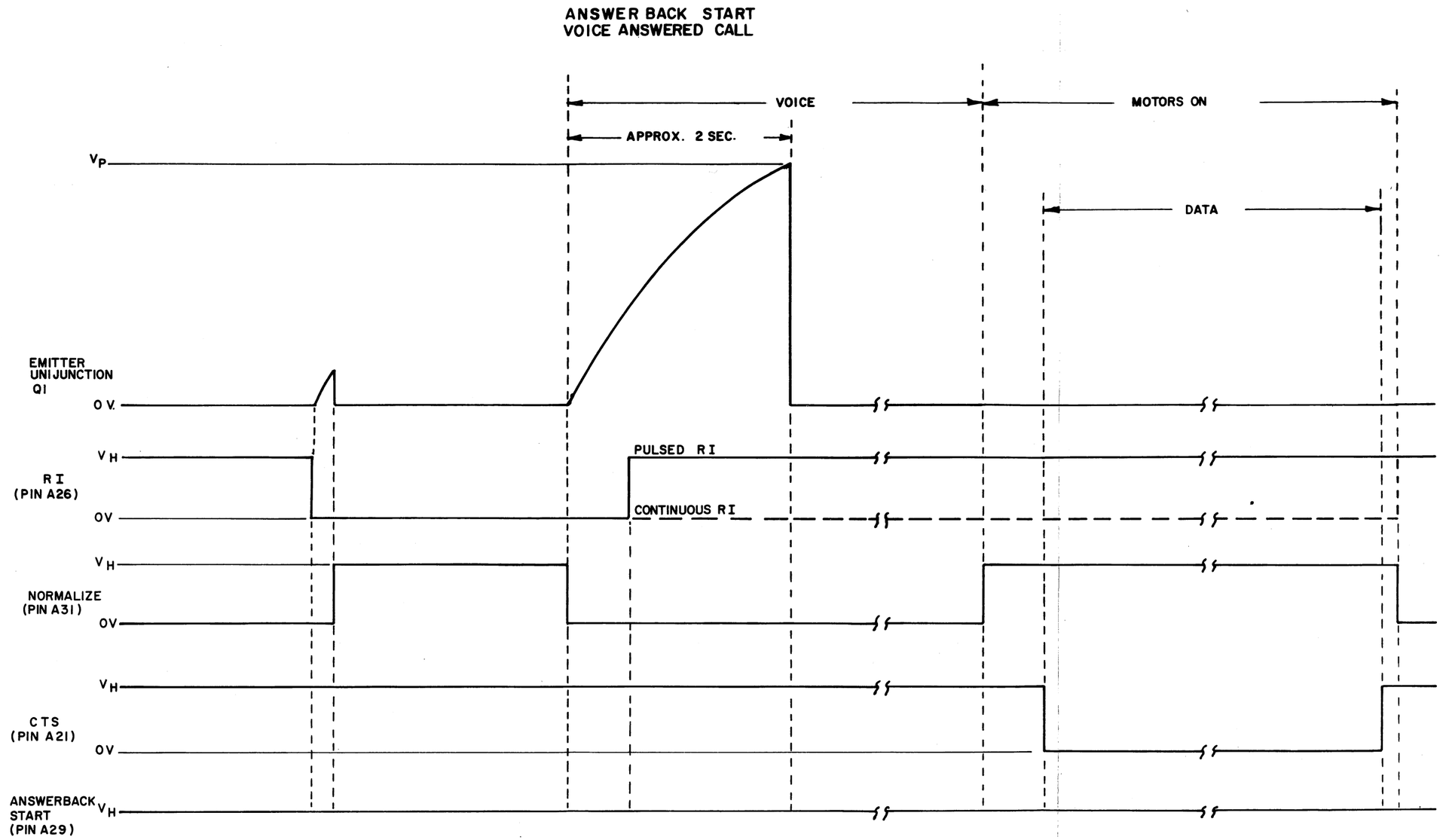
2.8 (Continued)

The MLA1-6 output brought out on Pin B33 is the inverse of either signal input to MLA1-6. Locally generated Keyboard data cannot be sent "on-line" because KBD "local" (low on Pin B5) keeps the line Data Amp marking by means of R7 connected to the base of Q3.

2.9 Proceed Lamp Amplifier

The Proceed Lamp Amplifier consisting of Q4 and Q7 is driven via MLA1-8 and inverter MLA2-2. The amplifier is used to light the "Proceed" lamp located on the control strip, by applying approximately 24 volts across the lamp through R35, a current limiting resistor. Any time a CTS indication is present, the MLA2-2 output will be low, turning the amplifier "On", thereby lighting the "Proceed" lamp. A "Halt" indication (low on Pin B30) will force MLA2-2 high and turn the "Proceed" light off.

2.10 The integrating networks throughout the card are for noise protection.



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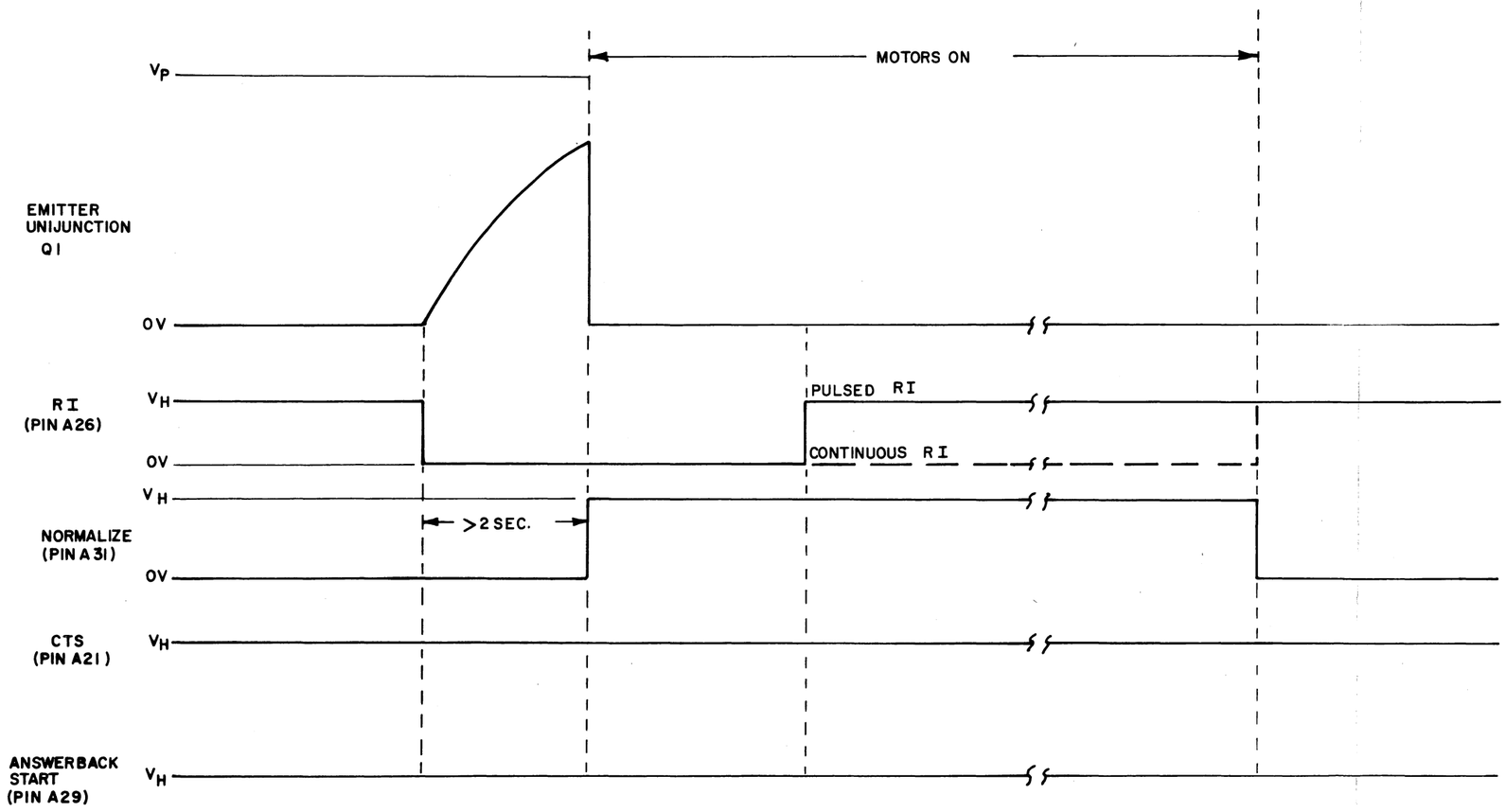
ANSWER BACK START
AUTOMATIC ANSWERED CALL
NO CLEAR TO SEND



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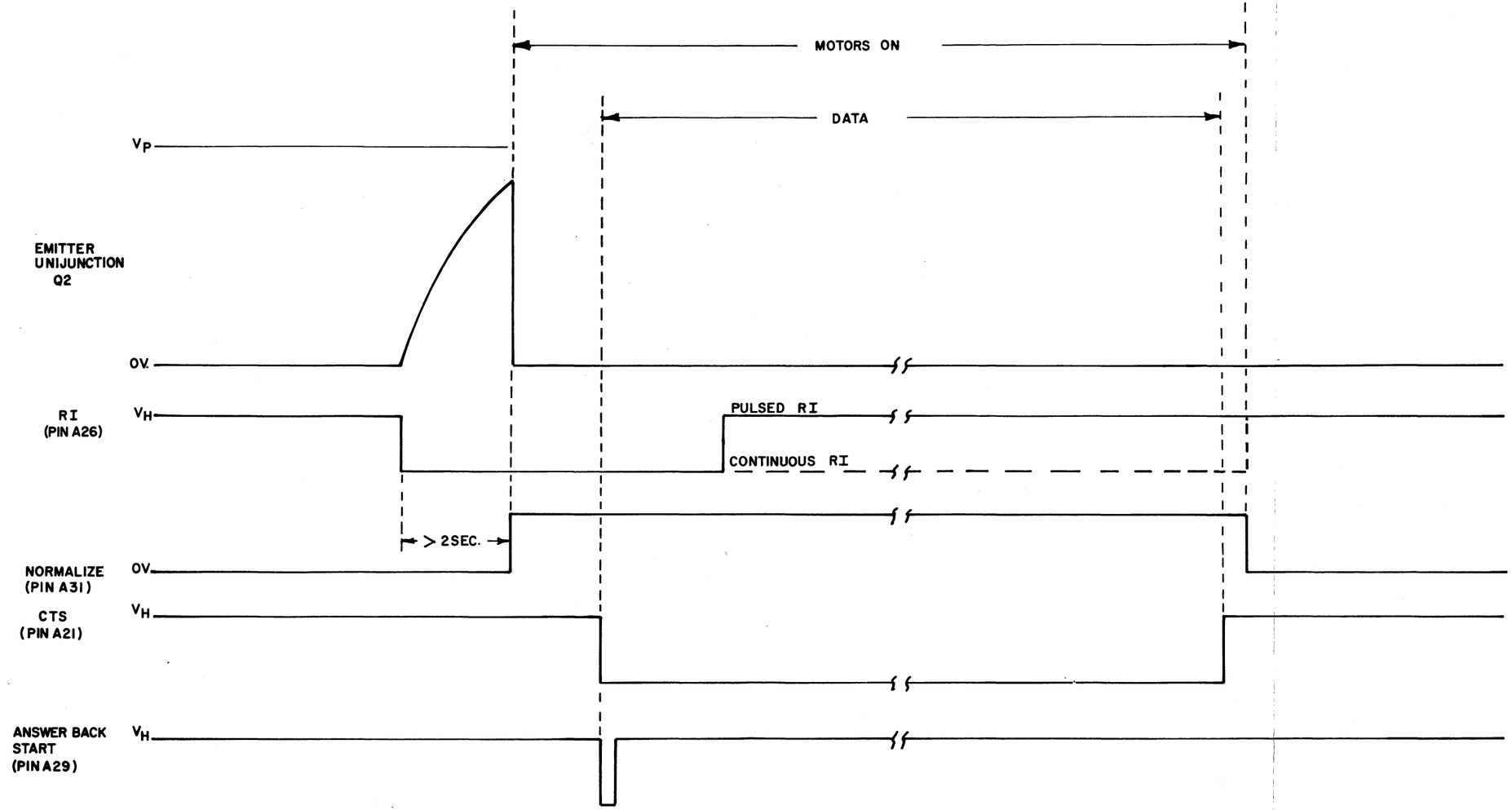
SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

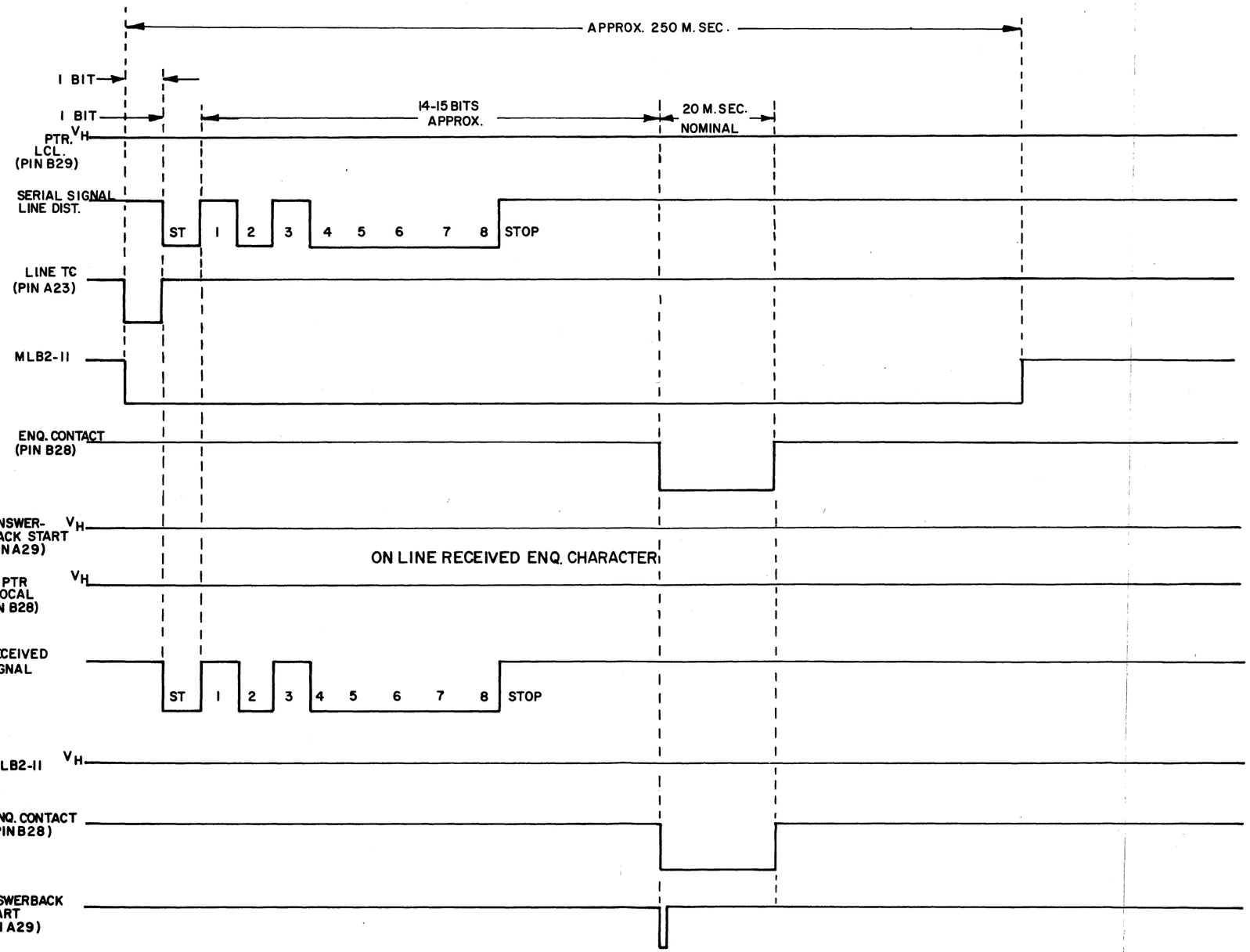
ANSWER BACK START
AUTOMATIC ANSWERED CALL.



NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

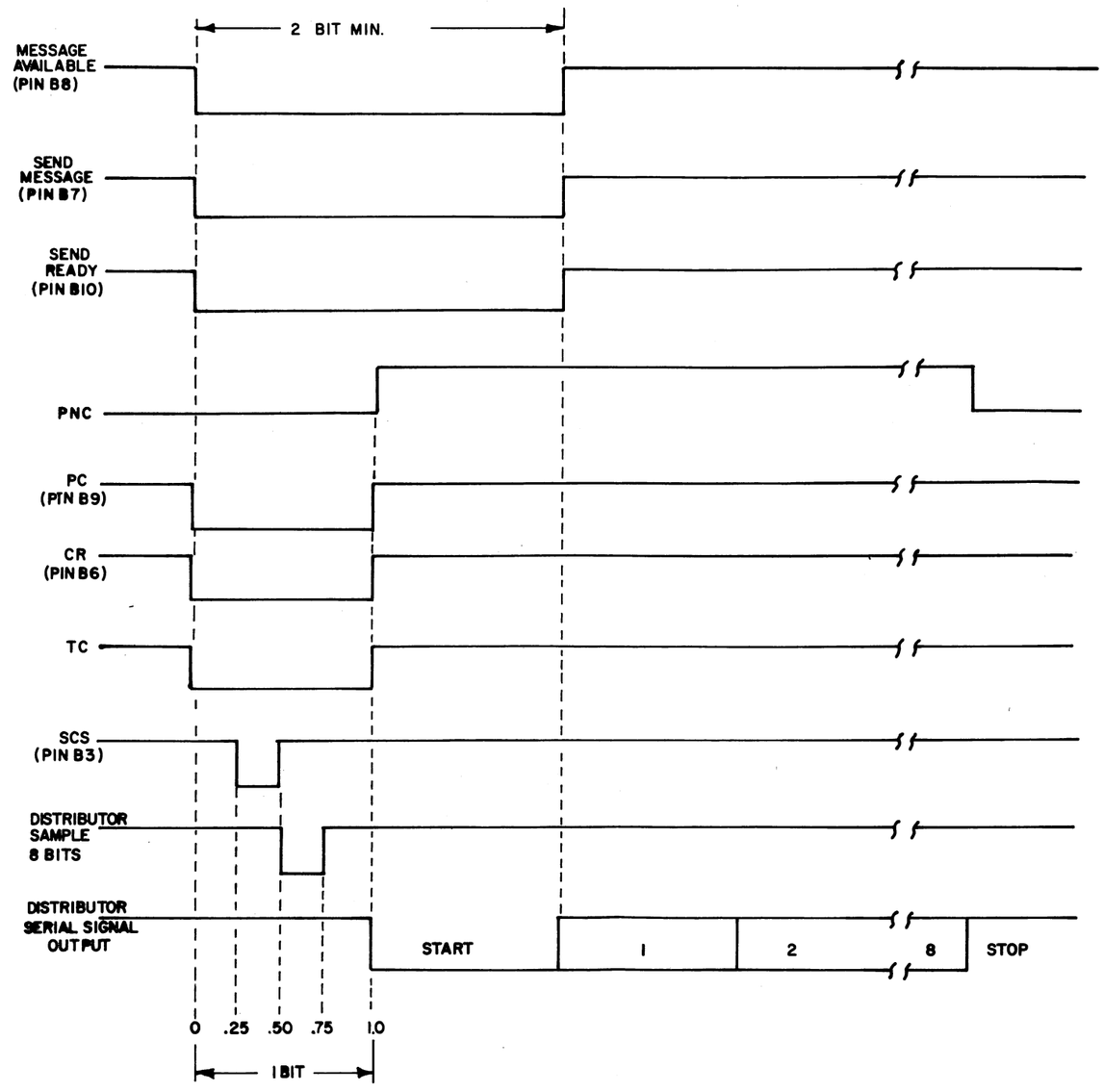
ON LINE GENERATED ENQ. CHARACTER.



NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

WDP

KEYBOARD LINE OR LOCAL OPERATION



NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

NO.	NOTES.
1.	ALL VOLTAGE DC UNLESS OTHERWISE SPECIFIED.
2	ALL RESISTORS 1/4 WATT, AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
4	INDICATES FEMALE TERMINAL INDICATES MALE TERMINAL. INDICATES CIRCUIT GROUND
5	REFER TO 322305 FOR ASSEMBLY INFORMATION
6.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD. MLD3 — ROW, COLUMN, INTEGRATED CIRCUIT.
7	LOGIC NEGATION - A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION
8	WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER, THE GATE IS USED AS AN INVERTER
9.	VCC IS PROVIDED TO THE INTEGRATED CIRCUIT PACKAGE ON PIN 14, AND GROUND ON PIN 7 THIS APPLIES TO ALL PACKAGES.
10	THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC AND 0V RESPECTIVELY.
11	REFER TO 8399WD FOR TRUTH TABLES.

J402 3 +12V. 1/2 AMP SL-BL

J403 ANSWERBACK COIL. W-G

C4 10 + R26 150 (1/2W.)

CR1 IN4002

ANSWERBACK COIL. W-Y

OFF NORMAL SWITCH. W-R J403 100 R27 R5 5.6K VCC.

2 MESSAGE AVAILABLE. MLA1 C6 47

VCC. R24 10K Q4 2N3638 R1 680 R25 220(3W.) Q1 2N3767 R16 1K. -12V.

VCC. R4 3.6K MLB4 C5 0.1 R20 100 R18 22K VCC.

4 START

MLC4 FF S_D C_P C_D S_1 S_2 C_1 C_2 I N C

VCC. R3 3.6K

+12V. R21 12K R22 42K 1/2 W C1 0.68 B_2 Q5 MU4894 B_1 R23 51 R2 680 Q2 2N3569 R19 100

Q3 2N3569 R15 1K

5 -12V. -12V.

6 MLB4 4 5 MLA1

1 PRESENT CHARACTER.

6 CHARACTER AVAILABLE

13 12 MLB4 11

3 MLB4 2 1

VCC R17 22 K C2 6.8

J401 J403 11 GRD. C3 6.8 12 VCC.

R12 5.6K MLB3 BR IN OUT BIT 1

R7 5.6K MLB3 R IN OUT BIT 2

R6 5.6K MLB3 O IN OUT BIT 3

R9 5.6K MLB2 Y IN OUT BIT 4

R8 5.6K MLB2 G IN OUT BIT 5

R11 5.6K MLB3 BL IN OUT BIT 6

R14 5.6K MLB2 P IN OUT BIT 7

R13 5.6K MLB2 S IN OUT BIT 8

R10 5.6K

W IN SUPPRESS

MLA1 MLA1 OUT

BK CODE COMMON.

8774WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	4-25-69	20004-R
2	10-20-69	99749

SCHEMATIC WIRING DIAGRAM FOR ANSWERBACK DRIVER.

APPROVALS

D AND R	E OF M
LDM	

S-NUMBER 61.6355

PROD. NO. 8774 WD.

DATE 9-16-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B. CHKD.

ENGD. APPD.

TELETYPE CORPORATION

8774WD

TC 434 2-69

CIRCUIT DESCRIPTION FOR THE ANSWER BACK DRIVER CARD (ASSEMBLY NUMBER 322305)

TABLE OF CONTENTS

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION FOR THE ANSWER BACK DRIVER CARD (ASSEMBLY NUMBER 322305)

SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The 322305 Circuit Card Assembly is the electronic circuit portion for the YAB802 Answer Back Assembly. The card contains logic necessary for the data outputs, and the logic required to drive the answer back coil. It is mounted to a plate with two circuit card clamps.

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

The inputs to the circuit assembly are Nand type integrated Diode Transistor Logic (DTL). Each DTL input is approximately a 1.4 ma load to the device sinking current from it. At no time should any of the DTL inputs be more positive than 8 volts or more negative than -.7 volts.

2.1.1 Present Character (Pin 1, J402)

The Present Character input controls the read-out of the data bits and initiates the timing to step the answer back drum to the next position. When this lead reverts to the 0-state, the answer back begins to step and the data leads are sampled. The device driving this input must be capable of sinking three DTL loads.

2.1.2 Data Inputs (Color BR, R, O, Y, G, BL, P, S, W)

These inputs are connected to the data contacts 1 through S and the suppress contact which ride the answer back drum. A contact closure is defined as a MARK while a contact open is defined as a SPACE. A closure on the Suppress input produces a suppression command. These contacts must be capable of sinking two DTL loads.

2.1.3 Start (Pin 4, J402)

A 0-state on this lead produces the pulse necessary to start the answer back cycle. The device driving this input must be capable of sinking two DTL loads.

2.1.4 Code Common (Pin BK)

This input is the common contact for the answer back code contacts. The lead connects to the circuit board ground lead.

2.1.5 OFF NORMAL (Pin W-R)

This contact input from a switch is closed when the answer back drum is in its home position. This switch must be capable of sinking two DTL loads.

2.2 Output Characteristics

The outputs from this assembly are Nand type integrated Diode Transistor Logic (DTL) outputs unless otherwise specified. The outputs will be rated by the number of DTL loads which may be driven. (Each DTL load is approximately 1.4 ma.).

2.2.1 Message Available (Pin 2, J402)

This output, when in the 0-state, indicates that the Answer Back is selectable and has a message. It is capable of driving seven DTL loads.

2.2.2 Character Available (Pin 6, J402)

This output is a turn-around of the present character input. It indicates that a character is present and should now be taken. This lead is capable of sinking three loads less than the capability of the present character input.

2.2.3 Data Outputs (Pins 1, 2, 3, 4, 5, 6, 7, 8, 9 of J401)

These outputs present the MARK or SPACE bit information of a character to external logic. A 1-state indicates a MARK while a 0-state indicates a SPACE A SUPPRESS command is indicated by a 0-state. Each output is capable of driving eight external DTL loads.

2.2.4 Answer Back Coil (Pin W-G)

This output supplies fused +12V DC to the Answer Back Coil.

2.2.5 Answer Back Coil (Pin W-Y)

This output supplies -12V DC to the Answer Back Coil when Q1 is turned on, energizing the coil.

2.3 Miscellaneous Requirements

2.3.1 Power Supply Inputs

Integrated Circuit Voltage and Current.

Pin	V DC	I Max. (MA)
J401-12	+5V to +6.6V	110
J401-11	GRD	

Coil Voltage and Current.

Pin	V DC	I Max. (A)
J402-3	+12	1.2
J402-5	-12	1.2

2.3.2 Operating Temperature Range

0°C to 70°C (free air).

2.3.3 Storage Temperature Range

-40°C to +70°C.

2.4 Size

The card size is 4 inches by 4-1/2 inches.

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly Drawing 322305 (MC305) and Schematic Drawing 8774WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

The answer back assembly consists of a mechanical mechanism and an electronic circuit. The mechanism contains a stepping motor which moves a codable drum. Contact fingers ride the tines of the drum. The electronic circuit drives the stepping motor and provides the read-out for the contacts. Operation of the answer back circuitry is as follows:

Symbols and nomenclature referred to in this discussion are found on 8774WD. Assume that the answer back drum is in its idle state; a START command is absent and no MESSAGE AVAILABLE is presented.

A START command initiates answer back operation. A low input in Pin 4 couples through a filter network consisting of R18, R20, R4 and C5 and into gate MLB4-8. This circuit combination provides a momentary clock pulse to the drive flip-flop, MLC4, for each START command. At clock time flip-flop MLC4 sets, commencing the initial answer back step. The drive circuitry, consisting of Q4 and Q1 provides current to the answer back coil while a timing circuit, consisting of Transistors Q2, Q5 and Q3, measures the current duration.

Q1 permits current to build in the answer back coil at an exponential rate. The timing circuit allows current to flow in the coil for a nominal time period of 30 milliseconds. At this time a pulse is issued to clear the drive flip-flop. The drive transistors turn off. The answer back coil releases the armature which subsequently pulls the answer back drum to the 1st position.

At this time the normally closed STOP switch contact has opened, providing a MESSAGE AVAILABLE indication and disabling the synchronous inputs of the MLC4 flip-flop (the START input now has no effect on the circuit). Control of the answer back is now under the direction of the PRESENT CHARACTER input, Pin 1.

The terminal logic takes the MESSAGE AVAILABLE indication from the answer back logic and decides when to issue a PRESENT CHARACTER command. When the terminal issues the PRESENT CHARACTER (PC) command, three functions occur: data bits are presented at the data output gates for the duration of PC, the drive flip-flop is set through the SD input, and a CHARACTER AVAILABLE is issued on Pin J402-6. Setting the drive flip-flop initiates the process of advancing the answer back drum to the next position in the same manner discussed previously. Flip-flop MLC4 turns transistor Q4 on which turns transistor Q1 on. The answer back armature begins to pick-up. After a timed interval the drive flip-flop is cleared and the answer back armature is released.

2. (Continued)

The PRESENT CHARACTER input has simultaneously initiated both the cycle to advance the answer back drum and provided the read-out of the character. The PRESENT CHARACTER command, normally one bit in length, must be removed before the answer back armature is fully attracted and before the drum is moved. Thus, sufficient time is allowed to read the character before the drum is advanced.

Reading and advancing the answer back drum occurs with each PC command. When the drum advances to the home position, the STOP switch closes, causing removal of the MESSAGE AVAILABLE indication and priming the synchronous input of the drive flip-flop. The terminal logic does not issue further PRESENT CHARACTER commands when MESSAGE AVAILABLE has been removed. The answer back circuit is now in an idle state. The answer back may be started again by a START command on Pin J402-4.

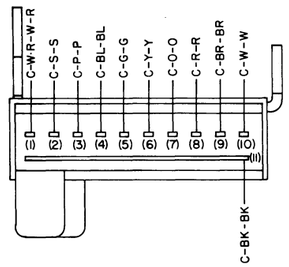
The network consisting of element C4, R26 and CR1 provides noise suppression from the answer back coil.

The network consisting of inverters MLB4-3, 6 and components R17 and C2 prevents the answer back from stepping off its rest position when power is applied to the circuit. Output 6 of MLB4, low for approximately 20 ms. after the initial power turn on, holds flip-flop MLC4 in the 0-state thereby preventing the answer back from stepping off NORMAL.

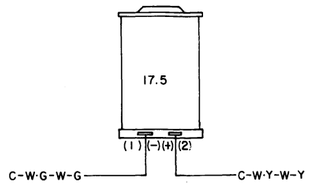
NO.	NOTES
1.	WIRING LEGEND: DISTANT TERMINATING AREA. DISTANT TERMINATING DESIGNATION A-W-R-W-R WIRE COLOR CODE
2.	COLOR CODE: Y - YELLOW G - GREEN W - WHITE R - RED S - SLATE O - ORANGE P - PURPLE B R - BROWN BL - BLUE BK - BLACK
3.	INDICATES MALE TERMINAL AND INDICATES FEMALE TERMINAL ON CONNECTOR.
4.	TERMINALS VIEWED FROM WIRED END.
5.	TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE AND ARE NOT MARKED ON COMPONENT.
6.	ALL WIRE 24 AWG, UNLESS OTHERWISE SPECIFIED.
7.	ASSOCIATED CABLE 333398.
8	

ACTUAL WIRING DIAGRAM

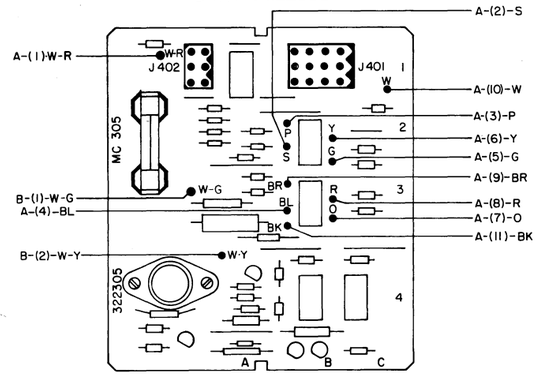
A
CONTACT ASSEMBLY 333382



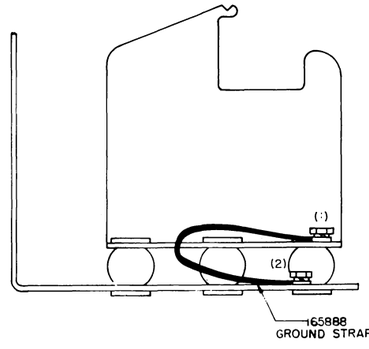
B
ANSWER-BACK COIL 307M



C
ANSWER-BACK DRIVER 322305

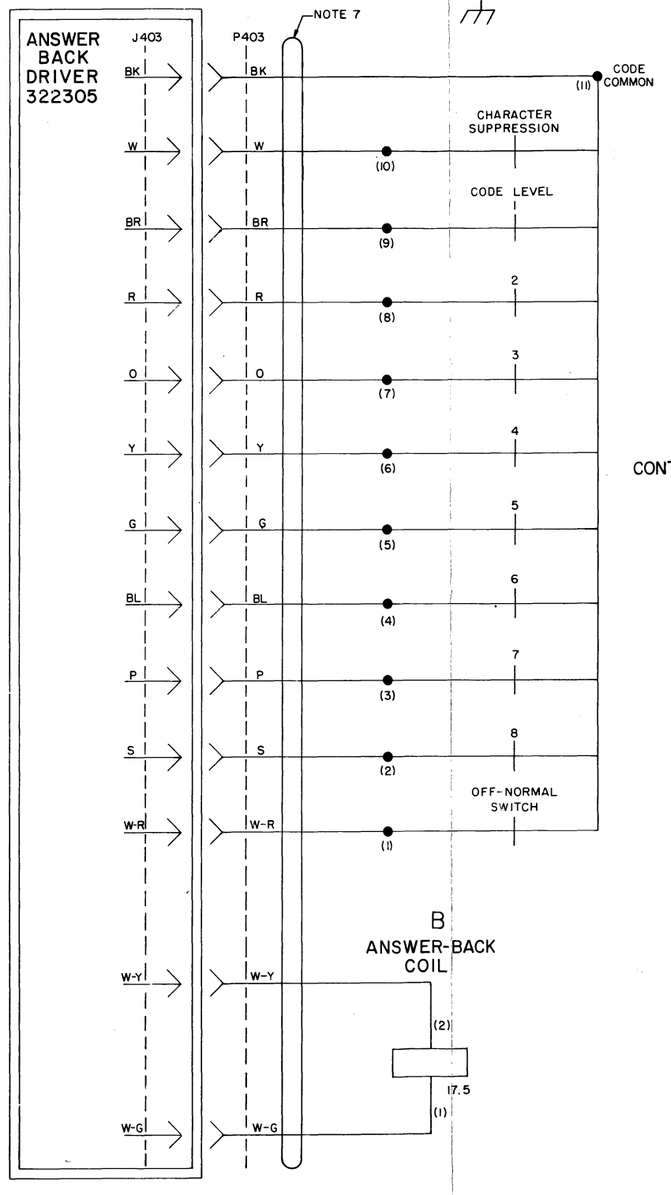


D
ANSWER-BACK ASSEMBLY YAB 802



SCHEMATIC WIRING DIAGRAM

D
ANSWER-BACK ASSEMBLY



A
CONTACT ASSEMBLY

B
ANSWER-BACK COIL

8845 WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	4-10-69	20006-R

ACTUAL AND SCHEMATI
WIRING DIAGRAM
FOR
YAB 802
ANSWER BACK

APPROVALS

D AND R	E OF M

S-NUMBER 61,635

PROD. NO. 8845 WD

DATE 11-6-68

P.D. FILE NO. G-A354AA

DRAWN D. W. J. | CHKD. RCB

ENGD. H. F. L. | APPD.

TELETYPE
CORPORATION

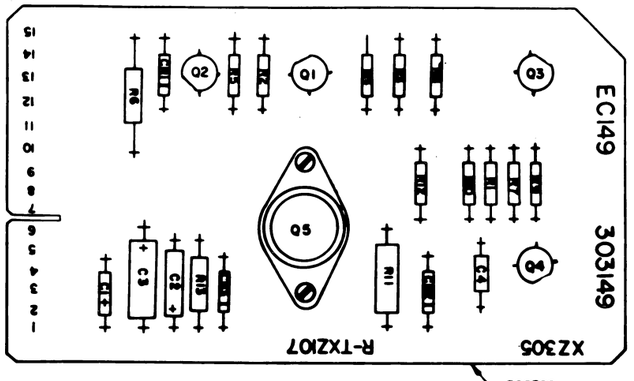
8845 WD

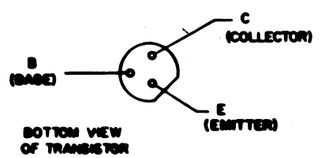
NO. NOTES

1 SEE SPECIFICATION MR2.001 FOR CIRCUIT BOARD REQUIREMENTS.

2 REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY

3 ASSOCIATED SCHEMATICS 8370WD





BOTTOM VIEW OF TRANSISTOR

CIRCUIT CARD EC

REF. DESIG.	TELETYPE PART NO	TOTAL QTY	NAME AND DESCRIPTION	LOCATING FUNCTION
R1-2	315958	2	RES. FIXED 3.6K	1/4W
R3	320275	1	" " 10K	1/4W
R4	315954	1	" " 1.5K	1/4W
R5	320275	1	" " 10K	1/4W
R6	182514	1	" " 91	1/2W
R7	315958	1	" " 3.6K	1/4W
R8	320275	1	" " 10K	1/4W
R9	320276	1	" " 470	1/4W
R10	321507	1	" " 1.8K	1/4W
R11	139336	1	" " 150	2W
R12	321213	1	" " 1K	1/4W
R13	118724	1	" " 220	1/2W
C1	327831	1	CAPACITOR DISC 6.8 MFD 6V DC	
C2	326591	1	" TANT. 3.9 MFD 35V DC	
C3	326592	1	" TANT. 33 MFD 35V DC	
C4	326752	1	" .03 MFD 50V DC	
Q2	324656	1	TRANSISTOR 2N3569	
Q1-3-4	315931	1	" 2N3638	
Q5	326594	1	" 2N3767	
CR1	321943	1	DIODE 1N4002	
CR2	197464	1	" 1N914	
CR3	321949	1	" 1N4002	
	326508	1	BOARD, ETCHED CIRC.	
	3598	2	NUT	
	154335	2	SCREW	
	107116	2	LOCKWASHER	

303149

REVISIONS

ISSUE	DATE	AUTH. NO.
6	11-15-68	9646-1

WDP

SHEET 1

RECEIVING DEVICE

APPROVALS

R AND D	E OF M
LWm	

E-NUMBER

PROD NO. 303149

DATE 8-11-67

R&D FILE G-A354AA

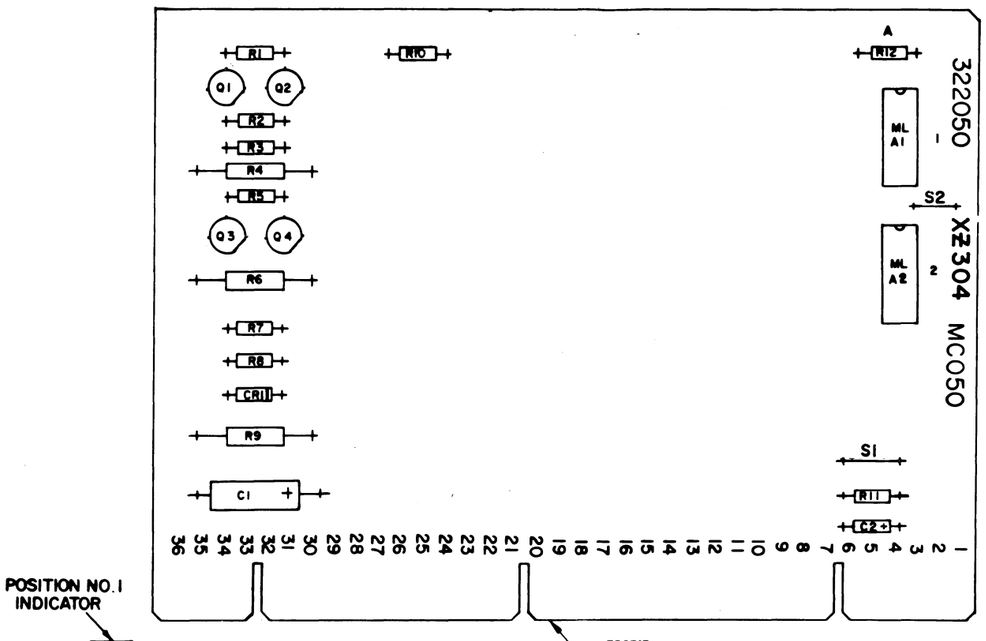
DRAWN R.J.P. CHKD.

ENGD. M.J.R. APPD.

TELETYPE CORPORATION

303149

NO.	NOTES
1	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD. ML D 2 — ROW — COLUMN — INTEGRATED CIRCUIT
2	SEE SPECIFICATION MR2,001 FOR CIRCUIT BOARD REQUIREMENTS.
3.	REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY 61519S.
4.	ASSOCIATED SCHEMATICS ARE: 8377 WD.



*R6 IS 470 OHMS ON SOME CARDS

CIRCUIT CARD MC050

REF. DESIG.	TELETYPE PART NO	TOTAL QTY	NAME AND DESCRIPTION	LOCATING FUNCTION
MLA1	326846	1	INTEGRATED CIRCUIT	
MLA2	326846	1	INTEGRATED CIRCUIT	
R1	320275	1	RESISTOR 10K 1/4W	
R2	315954	1	RESISTOR 1.5K 1/4W	
R3	320275	1	RESISTOR 10K 1/4W	
R4	182514	1	RESISTOR 91 OHMS 1/2W	
R5	320275	1	RESISTOR 10K 1/4W	
*R6	137439	1	RESISTOR 820 OHMS 1/2W	
R7	320275	1	RESISTOR 10K 1/4W	
R8	321213	1	RESISTOR 1K 1/4W	
R9	182514	1	RESISTOR 91 OHMS 1/2W	
R10-12	315958	3	RESISTOR 3.6K 1/4W	
C1	326590	1	CAPACITOR 10 MFD 50V	
C2	327831	1	CAPACITOR 6.8MFD,6 VDC	
CR1	321949	1	DIODE IN4002	
Q1	324656	1	TRANSISTOR 2N3569	
Q2	315931	1	TRANSISTOR 2N3638	
Q3	324656	1	TRANSISTOR 2N3569	
Q4	315931	1	TRANSISTOR 2N3638	
S1-S2	336470	2	INSULATED STRAP	
	326515	1	CIRCUIT BOARD	

322050

REVISIONS

ISSUE	DATE	AUTH. NO.
1	3-25-68	19091 R
2	6-7-68	95788
3	10-4-68	96309
3A	3-25-69	96618
4	11-15-69	96464
5	1-15-70	98935

WDP

SHEET 1 OF 2

ALARMS AND CONTROL

APPROVALS

R AND D	E OF M

E-NUMBER

PROD NO 322050

DATE 12-1-67

R&D FILE 8-A354AA

DRAWN WPB | CHKD

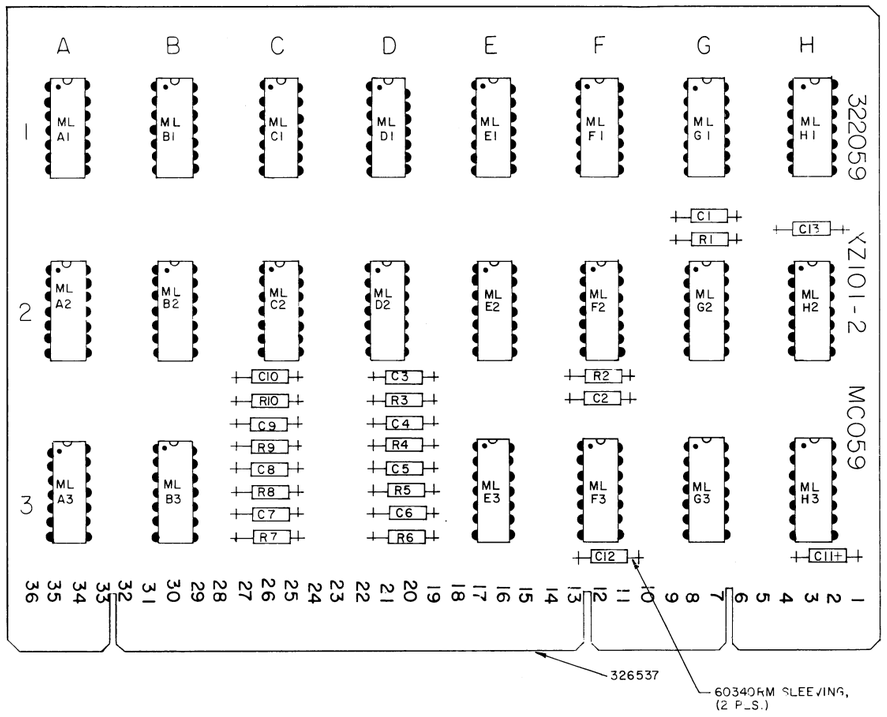
ENGD REL | APPD

TELETYPE CORPORATION

322050

TC 697(1-67)

NO	NOTES
1.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD ML D 2 ML — INTEGRATED CIRCUIT D — COLUMN 2 — ROW
2.	SEE SPECIFICATION MR 2.001 FOR CIRCUIT BOARD REQUIREMENTS.
3.	REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY:
4.	ASSOCIATED SCHEMATICS ARE 8371WD
5.	CIRCUIT DESCRIPTION 8371WD-CD.
6	ALL CHARACTERS ARE TO BE SILK SCREENED IN WHITE, RED, OR BLACK ENAMEL
7	CHARACTER HEIGHT .120-12 POINTS NEWS GOTHIC



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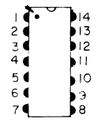


TOP VIEW OF DUAL IN-LINE

CIRCUIT CARD MC 059

REF. DESIG.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
MLA1	326853	3	INTEGRATED CIRCUIT 853	
MLA2			SAME AS MLA1	
MLA3	326852	5	INTEGRATED CIRCUIT 852	
MLB1	326833	1	INTEGRATED CIRCUIT 833	
MLB2			SAME AS MLA3	
MLB3	326846	8	INTEGRATED CIRCUIT 846	
MLC1	326830	2	INTEGRATED CIRCUIT 830	
MLC2			SAME AS MLA3	
MLD1			SAME AS MLC1	
MLD2			SAME AS MLA3	
MLE1			SAME AS MLA1	
MLE2			SAME AS MLA3	
MLE3			SAME AS MLB3	
MLF1	326862	2	INTEGRATED CIRCUIT 862	
MLF2			SAME AS MLB3	
MLF3			SAME AS MLB3	
MLG1	326832	1	INTEGRATED CIRCUIT 832	
MLG2			SAME AS MLB3	
MLG3			SAME AS MLF1	
MLH1			SAME AS MLB3	
MLH2			SAME AS MLB3	
MLH3			SAME AS MLB3	
R1-10	315948	10	RESISTOR, FIXED 100 OHM, 1/4W.	
C1,2,12,13	171583	4	CAPACITOR, .003MFD.	
C3-10	312385	8	CAPACITOR, 0.1MFD.	
C11	327831	1	CAPACITOR, 6.8MFD.	
	326537	1	CIRCUIT BOARD, ETCHED.	
	60340RM	2	SLEEVING.	

322059

REVISIONS

ISSUE	DATE	AUTH. NO.
1	3-10-69	19889 R

SHEET 1 OF 2

DISTRIBUTOR

APPROVALS

R AND D	E OF M

E-NUMBER

PROD NO 322059

DATE 6-18-68

R&D FILE G-A354AA

DRAWN W.P.B.	CHKD
ENGD. A.B.	APPD.

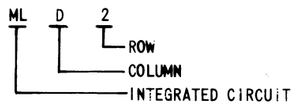
TELETYPE CORPORATION

322059

TC 637(1-67)

NO. NOTES

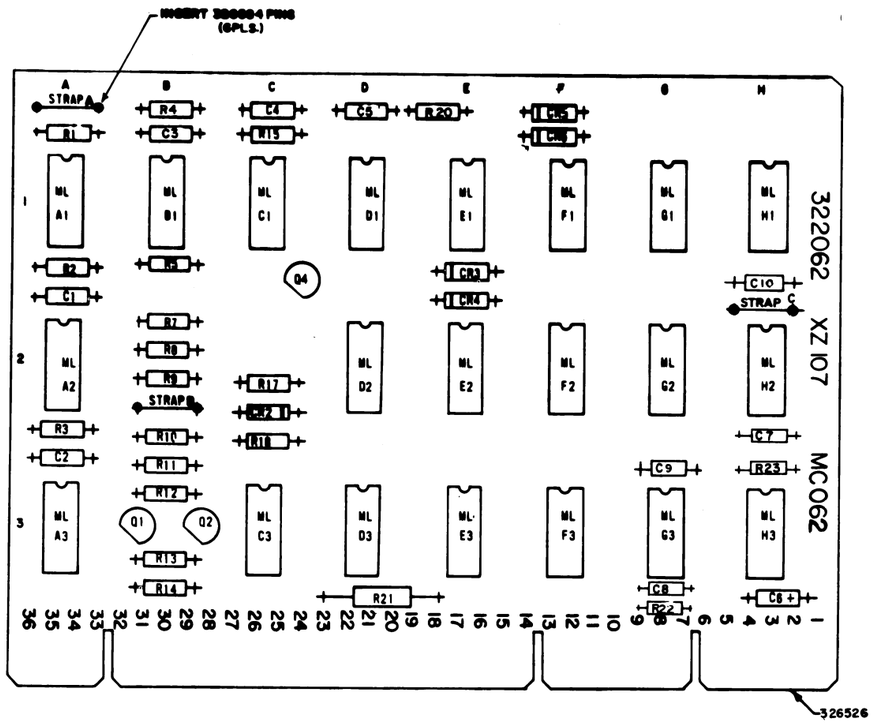
1 INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD

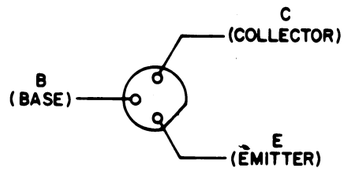


2 SEE SPECIFICATION MR2.001 FOR CIRCUIT BOARD REQUIREMENTS.

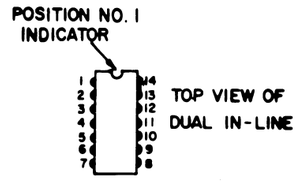
3. ASSOCIATED SCHEMATIC 8383WD

4. STRAPS A, B AND C ARE TO BE ADDED AFTER CARD MANUFACTURE TESTING HAS BEEN COMPLETED. REFER TO THE ASSOCIATED SCHEMATIC FOR STRAP OPTIONS.





BOTTOM VIEW OF TRANSISTOR



TOP VIEW OF DUAL IN-LINE

CIRCUIT CARD EC

REF. DESIG.	TELETYPE PART NO	TOTAL QTY	NAME AND DESCRIPTION	LOCATING FUNCTION
MLA1	326862	1	INTEGR. CIRC. 862	
MLB1	326846	1	" " 846	
MLC1	326846	1	" " 846	
MLD1	326845	1	" " 846	
MLE1	396830	1	" " 830	
MLF1	326846	1	" " 846	
MLG1	326852	1	" " [illegible]	
MLH1	326852	1	" " 852	
MLA2	326846	1	" " 846	
MLD2	326853	1	" " 853	
MLE2	326862	1	" " 862	
MLF2	326846	1	" " 846	
MLG2	326846	1	" " 846	
MLH2	326862	1	" " 862	
MLA3	326846	1	" " 846	
MLC3	326853	1	" " 853	
MLD3	326832	1	" " 832	
MLE3	326846	1	" " 846	
MLF3	326853	1	" " 853	
MLG3	326846	1	" " 846	
MLH3	326830	1	" " 830	
R1	315958	1	RES. FIXED. 3.6K	1/4W
R2	315986	1	" " 6.2K	1/4W
R3-R4	315971	2	" " 680	1/4W
R5-	315959	1	" " 4.7K	1/4W
R7-R10	315958	4	" " 3.6K	1/4W
R11	320275	1	" " 10 K	1/4W
R12	315958	1	" " 3.6K	1/4W
R13	315954	1	" " 1.5K	1/4W
R14	320275	1	" " 10 K	1/4W
R15 22.23	315948	3	" " 100	1/4W
R17	320275	1	" " 10 K	1/4W
R18	315959	1	" " 4.7K	1/4W
R20	315971	1	" " 680	1/4W
R21	182514	1	" " 91	1/2W
C1,2,3,7,8	312385	5	CAPACITOR .1 MFD	12V DC
C4,8,9,10	171563	3	" .003	100V
C5	312385	1	" .1 MFD	12V DC
C6	327331	1	" 6.8 MFD	6V DC
Q1	324858	1	TRANSISTOR 2N3569	
Q2	315931	1	" 2N3638	
Q4	324658	1	" 2N3569	
CR2-6	197464	5	DIODE 1N914	
	39803RM	3	STRAP - NOTE 5	
	326584	6	FORMED PIN	
	[illegible]	1	CIRCUIT BOARD	

322062

REVISIONS

ISSUE	DATE	AUTH. NO.
4	11-15-68	96464
5	2-24-69	96867-1
6	11-15-69	99881

WDP

SHEET 1

RECE CONTROL

APPROVALS

R AND D	E OF M
[signature]	[signature]

S-NUMBER 614345

PROD NO. 322062

DATE 12-12-67

R&D FILE G-A354AA

DRAWN R.J.P. CHKD.

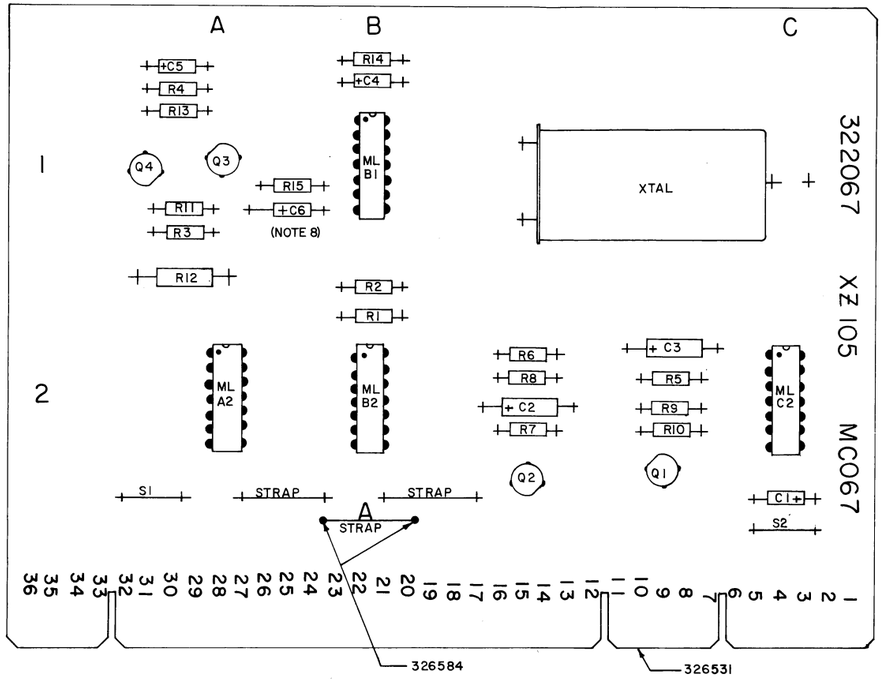
ENGD. A.B. APPD.

TELETYPE CORPORATION

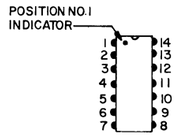
322062

TC 474 (1-66)

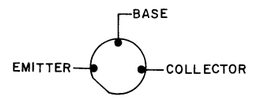
NO.	NOTES
1.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD. ML D 2 ML — INTEGRATED CIRCUIT D — COLUMN 2 — ROW
2.	SEE SPECIFICATION MR 2.001 FOR CIRCUIT BOARD REQUIREMENTS.
3.	S-NUMBER 61,516 S.
4.	ASSOCIATED SCHEMATIC: 8387 WD.
5.	STRAP "A" TO BE ADDED AFTER TESTING HAS BEEN COMPLETED.
6.	ALL CHARACTERS TO BE SILK SCREENED IN WHITE, BLACK, OR RED ENAMEL.
7.	CHARACTER HEIGHT .120-12 POINTS NEWS GOTHIC.
8.	R15 AND C6 NOT INCLUDED ON SOME CARDS
9.	ORIGINALLY KSR MODE CONTROL.



TOP VIEW OF INTEGRATED CIRCUIT PACKAGE.



BOTTOM VIEW OF TRANSISTOR



CIRCUIT CARD MC067

REF. DESIG.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
MLA2	326862	1	INTEGRATED CIRCUIT 862	
MLB1	326845	1	INTEGRATED CIRCUIT 845	
MLB2	326846	1	INTEGRATED CIRCUIT 846	
MLC2	326853	1	INTEGRATED CIRCUIT 853	
R1, 2	315958	3	RESISTOR, FIXED 3.6K, 1/4 W.	
R3,4,5	320275	3	RESISTOR, FIXED 10K, 1/4 W.	
R6	315974	1	RESISTOR, FIXED 300K, 1/4 W.	
R7	315947	2	RESISTOR, FIXED 510HM, 1/4 W.	
R8	315959	1	RESISTOR, FIXED 4.7K, 1/4 W.	
R9	315956	1	RESISTOR, FIXED 2.7K, 1/4 W.	
R10	321510	1	RESISTOR, FIXED 51K, 1/4W.	
R11	315954	1	RESISTOR, FIXED 1.5K, 1/4W.	
R12	182514	1	RESISTOR, FIXED 910HM, 1/2W	
R13			SAME AS R1.	
R14			SAME AS R7.	
R15	315972	1	RESISTOR, FIXED	22K 1/4W
C1, 6	327831	2	CAPACITOR, 6.8 MFD.	
C2	310926	1	CAPACITOR, 0.15 MFD.	
C3	315976	1	CAPACITOR, 470 PFD.	
C4	312385	1	CAPACITOR, 0.1 MFD.	
C5	171583	1	CAPACITOR, 0.003 MFD.	
Q1,2	315930	2	TRANSISTOR, 2N3568	
Q3	324656	1	TRANSISTOR, 2N3569	
Q4	315931	1	TRANSISTOR, 2N3638	
	39603RM	3	STRAP, 0.9 INCHES.	
S1- S2	336470	2	INSULATED STRAP	
	326584	2	PINS, FORMED.	
	326531	1	CIRCUIT BOARD.	
XTAL	327276	1	CRYSTAL 19.2 KHZ.	

322067

REVISIONS

ISSUE	DATE	AUTH. NO.
1	3-25-68	19091-R
2	6-7-68	95788
3	8-14-68	96060
4	10-22-68	96395
5	6-20-69	99181
6	1-15-70	98935
7	2-5-70	99993

SHEET 1 OF 2 WDP

NOTE 9

R.O. AND KSR MODE CONTROL

APPROVALS

R AND D	E OF M
HJK	

E-NUMBER

PROD NO 322067

DATE 9-12-68

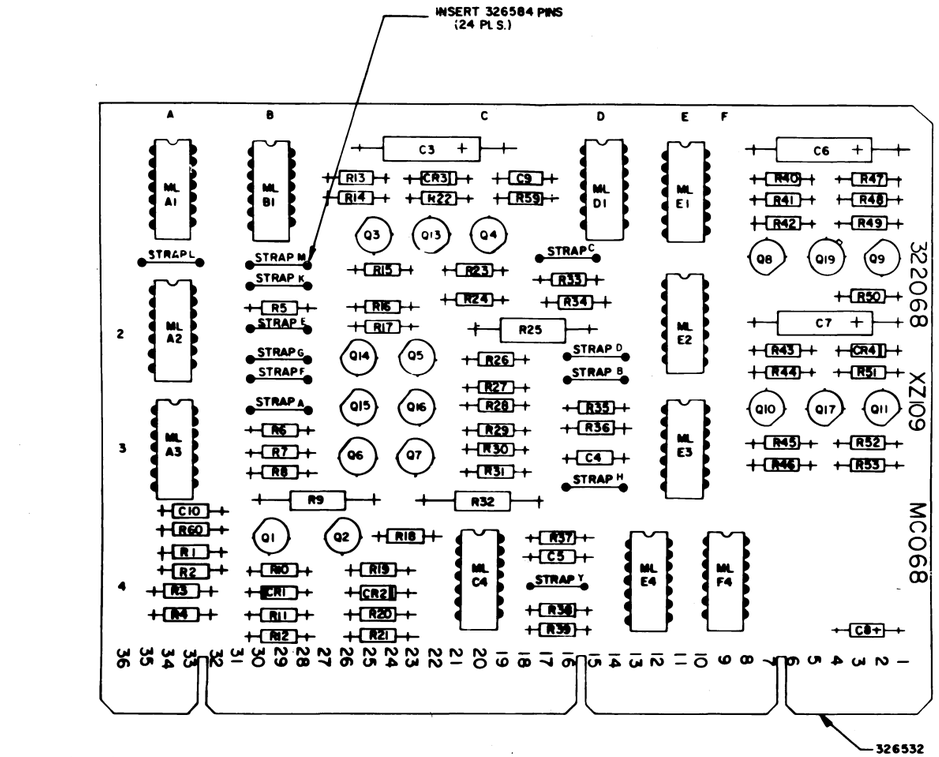
R&D FILE G-A354AA

DRAWN W.P.B.	CHKD
ENGD. C.A.Y.	APPD.

TELETYPE CORPORATION

322067

NO.	NOTES
1.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD ML D 2 ROW COLUMN INTEGRATED CIRCUIT
2.	SEE SPECIFICATION MR2.001 FOR CIRCUIT BOARD REQUIREMENTS
3.	ASSOCIATED SCHEMATICS ARE: 8388WD.
4.	STRAPS ARE TO BE ADDED AFTER CARD MANUFACTURE TESTING HAS BEEN COMPLETED. REFER TO ASSOCIATED SCHEMATIC FOR STRAP OPTIONS.



CIRCUIT CARD MC 068

REF DESIG.	TELETYPE PART NO	TOTAL QTY	NAME AND DESCRIPTION	LOCATING FUNCTION
MLA1	326845	1	INTEGRATED CIRCUIT 845	
MLB1	326845	1	INTEGRATED CIRCUIT 845	
MLD1	326830	1	INTEGRATED CIRCUIT 830	
MLE1	326846	1	INTEGRATED CIRCUIT 846	
MLA2	326846	1	INTEGRATED CIRCUIT 846	
MLE2	326862	1	INTEGRATED CIRCUIT 862	
MLA3	326846	1	INTEGRATED CIRCUIT 846	
MLE3	326836	1	INTEGRATED CIRCUIT 836	
MLC4	326862	1	INTEGRATED CIRCUIT 862	
MLE4	326846	1	INTEGRATED CIRCUIT 846	
MLF4	326846	1	INTEGRATED CIRCUIT 846	
R1	315958	4	RESISTOR, FIXED 3.6K 1/4W	
R59	315947	1	RESISTOR, FIXED 51 Ω 1/4W	
R5	315958	1	RESISTOR, FIXED 3.6K 1/4W	
R6	320275	1	RESISTOR, FIXED 10K 1/4W	
R7	315954	1	RESISTOR, FIXED 1.5K 1/4W	
R8	320275	1	RESISTOR, FIXED 10K 1/4W	
R9	182514	1	RESISTOR, FIXED 91 Ω 1/2W	
R10	315959	1	RESISTOR, FIXED 4.7K 1/4W	
R11	320275	1	RESISTOR, FIXED 10K 1/4W	
R12	315959	1	RESISTOR, FIXED 4.7K 1/4W	
R13	315972	1	RESISTOR, FIXED 22K 1/4W	
R14	315948	1	RESISTOR, FIXED 100 Ω 1/4W	
R15	315954	1	RESISTOR, FIXED 1.5K 1/4W	
R16	320275	1	RESISTOR, FIXED 10K 1/4W	
R17	315955	1	RESISTOR, FIXED 2.2K 1/4W	
R18	315958	1	RESISTOR, FIXED 3.6K 1/4W	
R19	315959	1	RESISTOR, FIXED 4.7K 1/4W	
R20	320275	1	RESISTOR, FIXED 10K 1/4W	
R21-3	315959	3	RESISTOR, FIXED 4.7K 1/4W	
R24	320275	1	RESISTOR, FIXED 10K 1/4W	
R25	171441	1	RESISTOR, FIXED 560 Ω 1W	
R26	315954	1	RESISTOR, FIXED 1.5K 1/4W	
R27	320275	1	RESISTOR, FIXED 10K 1/4W	
R28	315958	1	RESISTOR, FIXED 3.6K 1/4W	
R29	320275	1	RESISTOR, FIXED 10K 1/4W	
R30	315954	1	RESISTOR, FIXED 1.5K 1/4W	
R31	320275	1	RESISTOR, FIXED 10K 1/4W	
R32	182514	1	RESISTOR, FIXED 91 Ω 1/2W	
R33	320275	1	RESISTOR, FIXED 10K 1/4W	
R34-5	315958	2	RESISTOR, FIXED 3.6K 1/4W	
R36-7	315971	2	RESISTOR, FIXED 680 Ω 1/4W	
R38-9	315958	2	RESISTOR, FIXED 3.6K 1/4W	
R40-1	315948	2	RESISTOR, FIXED 100 Ω 1/4W	
R42	315959	1	RESISTOR, FIXED 4.7K 1/4W	
R43	321545	1	RESISTOR, FIXED 12K 1/4W	
R44	315948	1	RESISTOR, FIXED 100 Ω 1/4W	
R45	315954	1	RESISTOR, FIXED 1.5K 1/4W	
R46	320275	1	RESISTOR, FIXED 10K 1/4W	
R47	315952	1	RESISTOR, FIXED 820 Ω 1/4W	
R48	326601	1	RESISTOR, FIXED 150K 1/4W	
R49	326598	1	RESISTOR, FIXED 56 Ω 1/4W	
R50	315959	1	RESISTOR, FIXED 4.7K 1/4W	
R51	320275	1	RESISTOR, FIXED 10K 1/4W	
R52-3	315959	2	RESISTOR, FIXED 4.7K 1/4W	
R60	315947	1	RESISTOR, FIXED 51 Ω 1/4W	
Q1-11	324656	11	TRANSISTOR 2N3569	
Q13-17	315931	5	TRANSISTOR 2N3638	
Q19	321512	1	TRANSISTOR 2N2646	
CR1-4	197464	4	DIODE 1N914	
C9	312385	1	CAPACITOR .1 MFD 10V DC	
C3	326592	1	CAPACITOR 33 MFD	
C4-5	312385	2	CAPACITOR .1 MFD 10V DC	
C6	326592	1	CAPACITOR 33 MFD 35V DC	
C7	300027	1	CAPACITOR 15 MFD 35V DC	
C10	312385	1	CAPACITOR .1 MFD 10V DC	
	39603RM	12	STRAP .700 24 AWG NOTE 5	
	326584	24	FORMED PIN	
	326532	1	CIRCUIT BOARD	
C8	327831	1	CAPACITOR 6.8 MFD 6V DC	

322068

REVISIONS

ISSUE	DATE	AUTH. NO.
5	8-2-68	95997
5A	1-22-69	96747
5B	1-23-69	96771
6	11-15-68	96464
7	2-19-69	96464-1
8	8-5-69	99359
9	11-15-69	99880

SHEET 1 OF 2

CHANNEL CONTROL

APPROVALS

R AND D	E N M
L&M	

S-NUMBER 61521S

PROD NO 322068

DATE 1 2 68

PROD FILE G A354AA

DRAWN W P B	CHKD
ENGD C A Y	APPD D E H

TELETYPE CORPORATION

322068

TC 637(1-67)

NO. NOTES

1 INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD

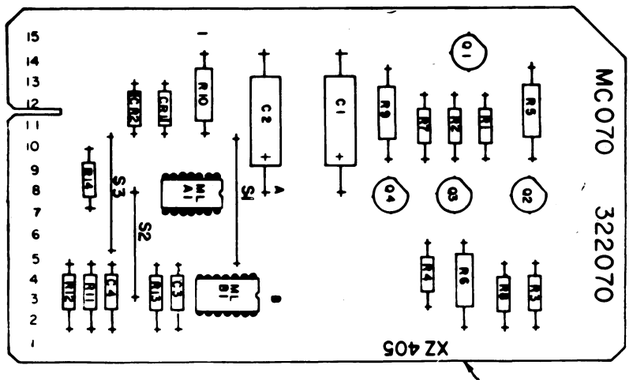
ML D 2

ROW
COLUMN
INTEGRATED CIRCUIT

2 SEE SPECIFICATION MR2.001 FOR CIRCUIT BOARD REQUIREMENTS.

3 REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY: 61,510S

4 ASSOCIATED SCHEMATIC IS 8389WD



*R6 IS 470 OHMS ON SERIE CARDS

	REF. DESIG.	TELETYPE PART NO	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
R1,2,3,4		320275	4	RES., FIXED 10K	1/4W
	R5	137602	1	" " 470	1/2W
	R7,R8	321213	2	" " 1K	1/4W
R9,R10,R14		10...1	3	" " 91	1/2W
R11 R12		315958	2	" " 3.6K	1/4W
	R13	315971	1	" " 680	1/4W
	R6	137439	1	" " 820	1/2W
	C1,C2	326590	2	CAPACITOR 10 MFD	50V DC
	C3	312385	1	" 0.1 MFD	10V DC
	C4	327831	1	" 6.8 MFD	5V DC
CR1,CR2		321949	2	DIODE IN4002	
	Q1,Q2	315931	2	TRANSISTOR 2N3638	
	Q3,Q4	324656	2	" 2N3569	
	MLA1	326846	1	INTEGR. CIRC. 846	
	MLB1	326862	1	" " 862	
	S1,S3	336470	3	INSULATED STRAP	
		326534	1	CIRCUIT BOARD	

ISSUE CONTROL RECORD

SHEET NO.	ISSUE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	X	X	X	X	X	X														
2	X	X	X																	

322070

REVISIONS

ISSUE	DATE	AUTH. NO.
4	11-15-68	96464
5	1-15-70	98935
6	3-2-70	98937

WDP

SHEET 1

TWO COLOR RIBBON CONTROL

APPROVALS

R AND D	E OF M

E-NUMBER

PROD NO 322070

DATE 11-15-67

R&D FILE G-A354AA

DRAWN W.P.B. CHKD

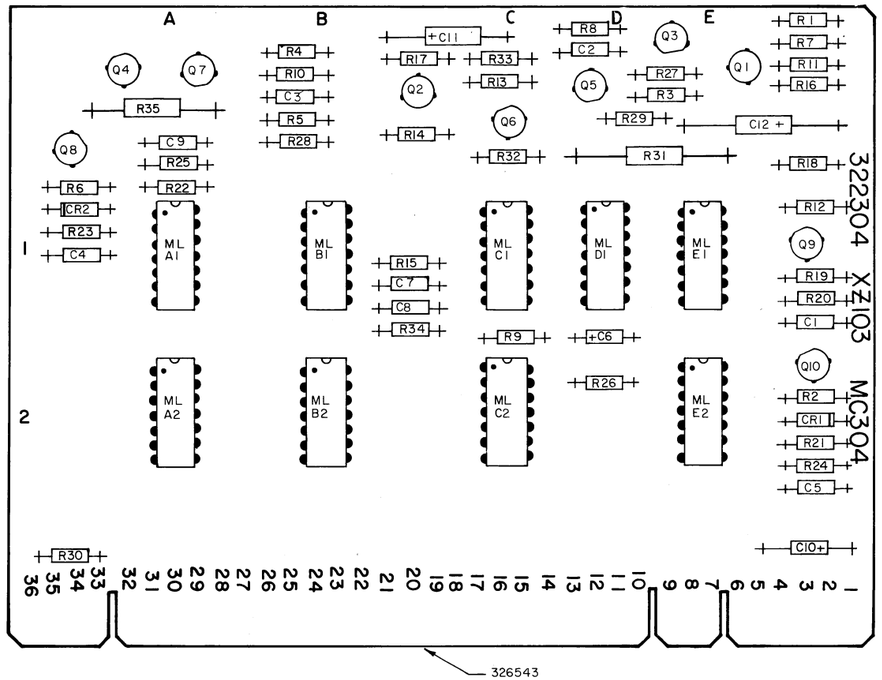
ENGD R... APPD

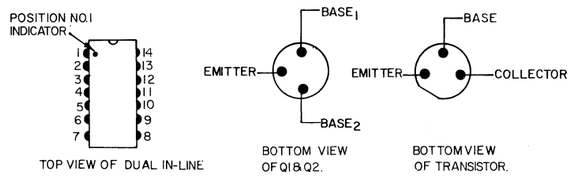
TELETYPE CORPORATION

322070

TC 474 1-66)

NO.	NOTES.
1.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD. ML A 2 ROW COLUMN INTEGRATED CIRCUIT
2.	SEE SPECIFICATION MR 2.001 FOR CIRCUIT BOARD REQUIREMENTS.
3.	S-NUMBER: 61,618 S
4.	ASSOCIATED SCHEMATIC: 8773 WD.
5.	ALL CHARACTERS TO BE SILK SCREENED IN WHITE, RED, OR BLACK ENAMEL.
6.	CHARACTER HEIGHT .120-12 POINTS NEWS GOTHIC.
7.	ORIGINALLY KSR MODE CONTROL.





CIRCUIT CARD MC304

REF. DESIG.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
ML A1	326846	6	INTEGRATED CIRCUIT 846	
ML A2	326836	1	INTEGRATED CIRCUIT 836	
ML B1			SAME AS ML A1	
ML B2	326862	2	INTEGRATED CIRCUIT 862	
ML C1			SAME AS ML A1	
ML C2			SAME AS ML A1	
ML D1			SAME AS ML A1	
ML E1			SAME AS ML A1	
ML E2			SAME AS ML B2	
R1-6	320275	6	RESISTOR, FIXED 10K, 1/4W.	
R7-10	315958	4	RESISTOR, FIXED 3.6K, 1/4W.	
R11-15	315947	5	RESISTOR, FIXED 51 OHM, 1/4 W.	
R16-17	315953	2	RESISTOR, FIXED 1.2K, 1/4W.	
R18	315974	1	RESISTOR, FIXED 300K, 1/4W.	
R19	326602	1	RESISTOR, FIXED 360 OHM, 1/4W.	
R20-23	315959	4	RESISTOR, FIXED 4.7K 1/4 W.	
R24-26	315948	3	RESISTOR, FIXED 100 OHM, 1/4W.	
R27-28	315954	2	RESISTOR, FIXED 1.5K, 1/4W.	
R29-30	315955	2	RESISTOR, FIXED 2.2K, 1/4W.	
R31	171441	1	RESISTOR, FIXED 560 OHM, 1W.	
R32	326602	1	RESISTOR, FIXED 360 OHM, 1/4W.	
R33	321510	1	RESISTOR, FIXED 51K, 1/4 W.	
R34	326598	1	RESISTOR, FIXED 56 OHM, 1/4W.	
R35	182514	1	RESISTOR, FIXED 91 OHM, 1/2W.	
C1-4	171583	4	CAPACITOR, 0.003 MFD. 75V.	
C5,7,8,9	312385	4	CAPACITOR, 0.1 MFD. 10V.	
C6,10	327831	2	CAPACITOR, 6.8 MFD. 6V.	
C11-12	326591	2	CAPACITOR, 3.9MFD. 35V.	
CR1-2	197464	2	DIODE, IN914.	
Q1-2	327812	2	TRANSISTOR, MU4894	
Q3-4	315931	2	TRANSISTOR, 2N3638	
Q5-10	324656	6	TRANSISTOR, 2N3569	
	326543	1	CIRCUIT BOARD	

ISSUE CONTROL RECORD

SHEET NO.	ISSUE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	X	X	X																	
2	X	X																		

322304

REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-20-68	19777 R
2	2-5-70	99993
3	6-4-70	98943

WDP

SHEET 1 OF 2 - **NOTE 7**

RO AND KSR SEND CONTROL

APPROVALS

R AND D	E OF M

E-NUMBER

PROD NO. 322304

DATE 9-26-68

R&D FILE G-A354AA

DRAWN W.P.B.	CHKD.
ENGD. C.A.Y	APPD.

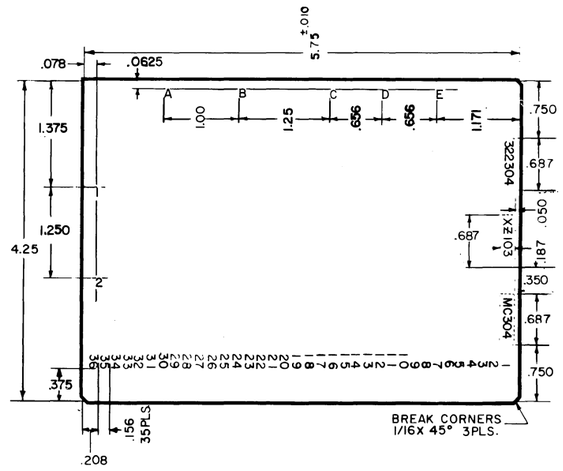
TELETYPE CORPORATION

322304

TC 637(1-67)

ALL DIMENSIONS ± 1/16
UNLESS OTHERWISE SPECIFIED.

SEE SHEET 1 FOR NOTES.



CIRCUIT CARD MC 304

322304

PARTS REQ.	NO. REQ.	USED ON	NO. REQ.
		326543	1

REVISIONS

ISSUE NO.	DATE	AUTHOR NO.
1	12-20-68	19777A
2	6-2-70	98943

WDP

SHEET 2 OF 2

APPROVALS

D AND R	E OF M
	7

E. NUMBER

PROD.NO. 322304

SCALE: 1/1

STOCK SPECIFICATION

SIZE	KIND	SHAPE	TEMPER

DRAWN	P.O. FILE NO.	DATE
W.P.B	G-A354AA	10-1-68
DESIGNED	ENGINEER	CHECKED	APPROVED
C.A.Y	C.A.Y		

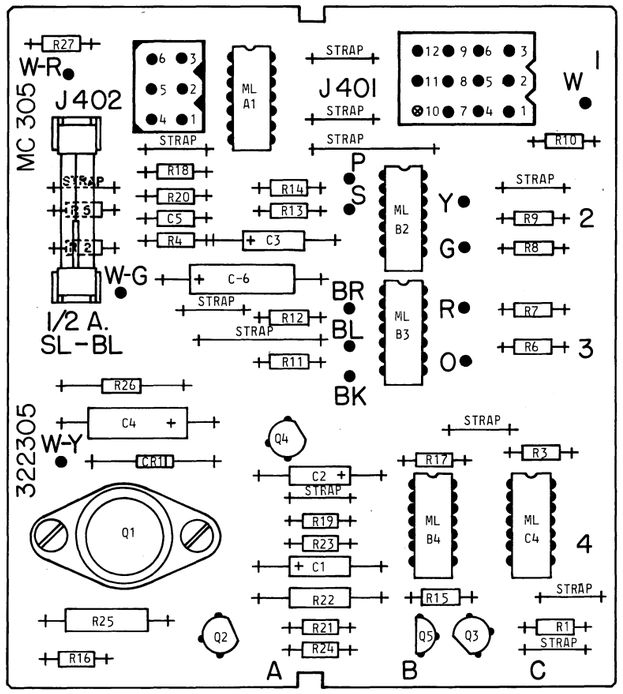
TELETYPE CORPORATION

322304

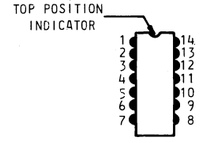
REF. DESIG.	PART NO. REQ.	QTY.	DESCRIPTION
MLA1	326846	4	INTEGRATED CIRCUIT
MLB2			SAME AS MLA1
MLB3			SAME AS MLA1
MLB4			SAME AS MLA1
MLC4	326845	1	INTEGRATED CIRCUIT
R1-2	315971	2	RESISTOR 680 1/4 WATT
R3-4	315958	2	RESISTOR 3.6K 1/4 WATT
R5-14	315960	10	RESISTOR 5.6K 1/4 WATT
R15-16	321213	2	RESISTOR 1K 1/4 WATT
R17-18	315972	2	RESISTOR 22K 1/4 WATT
R19-20,27	315948	3	RESISTOR 100 1/4 WATT
R21	315953	1	RESISTOR 1.2K 1/4 WATT
R22	193269	1	RESISTOR 42K 1/2 WATT
R23	315947	1	RESISTOR 51 1/4 WATT
R24	320275	1	RESISTOR 10K 1/4 WATT
R25	199839	1	RESISTOR 220 3 WATT
R26	124856	1	RESISTOR 150 1/2 WATT
C1	310928	1	CAPACITOR 0.68 MFD 35V
C2-3	327831	2	CAPACITOR 6.8 MFD 6V
C4	326590	1	CAPACITOR 10 MFD 50V
C5	312385	1	CAPACITOR 0.1 MFD 10V
C6	310931	1	CAPACITOR 47 MFD 20V
CR1	321949	1	DIODE IN4002
Q1	326594	1	TRANSISTOR 2N3767
Q2-3	324656	2	TRANSISTOR 2N3569
Q4	315931	1	TRANSISTOR 2N3638
Q5	327812	1	TRANSISTOR MU4894
	336470	11	STRAP
	117176	1	FUSE 1/2 AMP SL-BL
	171595	2	FUSE HOLDER
	326584	13	CONNECTOR PINS (MALE)
	182641	17	CONNECTOR PINS (FEMALE)
J402	182650	1	6 PIN CONNECTOR
J401	182647	1	12 PIN CONNECTOR
	151637	4	SCREW 4-40
	151880	4	NUT 4-40
	3640	4	LOCK WASHER
	326527	1	CIRCUIT BOARD

NOTE: MANUFACTURE PER MR2001

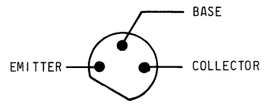
NO.	NOTES
1.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD. ML A 2 ML — INTEGRATED CIRCUIT A — COLUMN 2 — ROW
2.	ALL CHARACTERS TO BE SILK SCREENED IN WHITE, BLACK, OR RED ENAMEL. CHARACTER HEIGHT .120 - 12 POINT NEWS GOTHIC.



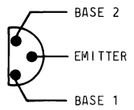
TOP VIEW OF INTEGRATED CIRCUIT PACKAGE



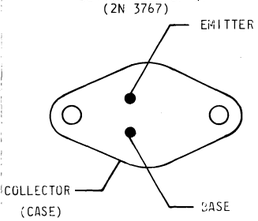
TYPICAL BOTTOM VIEW OF TRANSISTOR



BOTTOM VIEW OF Q5 (MU 4894)



BOTTOM VIEW OF Q1 (2N 3767)



REVISIONS		
ISSUE	DATE	AUTH. NO.
1	4-15-69	19981-R
2	10-20-69	99749
3	3-20-70	99749-1

ISSUE CONTROL RECORD																			
SHEET NO.	ISSUE																		
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1																				
2																				

WDP

CIRCUIT CARD

MC 305

APPROVALS		
PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.
ENGR.	DSGNR.	
DRN. D.W.J.	DATE 10-27-69	
E-NUMBER		
SD-CD NO. 8774		
R&D FILE G-A354AA		

TELETYPE

322305 (1)