3A PROCESSOR
DESCRIPTION
COMMON SYSTEMS

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1. GENERAL

INTRODUCTION

1.01 This section describes the physical and general operational characteristics of the 3A Processor used in a variety of control and processing systems.

1.02 Whenever this section is reissued, the reasons for reissue will be listed in this paragraph.

1.03 This section includes:

(a) Physical description of 3A Processor and its major components

(b) General discussion of the operational characteristics and capabilities.

1.04 The 3A Processor receives information from a variety of sources such as teletypewriters, magnetic tape transports, magnetic disks, ferrod switches, relays, etc. This information is stored in main store (MAS) or in registers in the 3A central control (3A CC) unit, and is acted upon as directed by the programs stored in MAS, or the microprogram control in the 3A CC. As a result of these programs, the 3A Processor issues commands to control peripheral devices, controls operation of relays or other equipment, and supervises transfer of information from MAS to peripheral devices or between peripheral devices.

PURPOSE

1.05 The 3A Processor is used to monitor and control the operation of a physical system of equipment in accordance with a set of programs that are stored in the 3A Processor. Data manipulations are performed by the 3A Processor as necessary to provide proper control of its external system. This is in contrast to computing machines whose primary purpose is data processing.

CONFIGURATION

1.06 For purposes of this document, the 3A Processor is defined to consist of a duplicated frame containing 3A CC, parallel channel (PCH) units, direct memory access (DMA) unit, MAS, and associated power supplies, a maintenance frame containing two tape data controllers (TDCs), two cartridge tape transports (CTTs), teletypewriter (TTY), and two teletypewriter controllers (TTYCs), and two programmable magnetic tape transport systems (PROMATS). Refer to Fig. 1. Two supplementary store frames may be added to increase memory capacity.

1.07 The label "central control 0" (CC 0), or "central control 1" (CC 1) is applied to the equipment frame which contains the 3A CC unit, PCH unit, DMA unit, and MAS. Other documentation may refer to CC 0 or CC 1 as "system control" (SYC), or as "3A Processor." Care must be taken to avoid confusing other references with the ones specified in this section. Refer to Fig. 2.

1.08 CC 0 and CC 1 occupy the left half and right half, respectively, of a double frame. The two CCs are identical and are duplicated to provide greater system reliability. One CC is normally on-line, controlling system operations. The other is off-line, but normally available to immediately take over control if a fault occurs in the on-line machine. The on-line CC can also exercise and run maintenance and diagnostic procedures on the off-line unit. The on-line CC normally writes into both on-line and off-line MASs simultaneously so that both stores contain identical data. If the on-line store performs a faulty read, the same address will be read from the off-line store provided that the system is in update mode.

1.09 The equipment complement of a 3A Processor will vary according to the requirements of the system in which it is installed. A basic CC could consist of a 3A CC, 32K words of MAS memory and the first serial input/output (I/O) channel. Additional memory may be installed in the CC frame up to 256K words in 32K word increments. A supplemental store frame is also

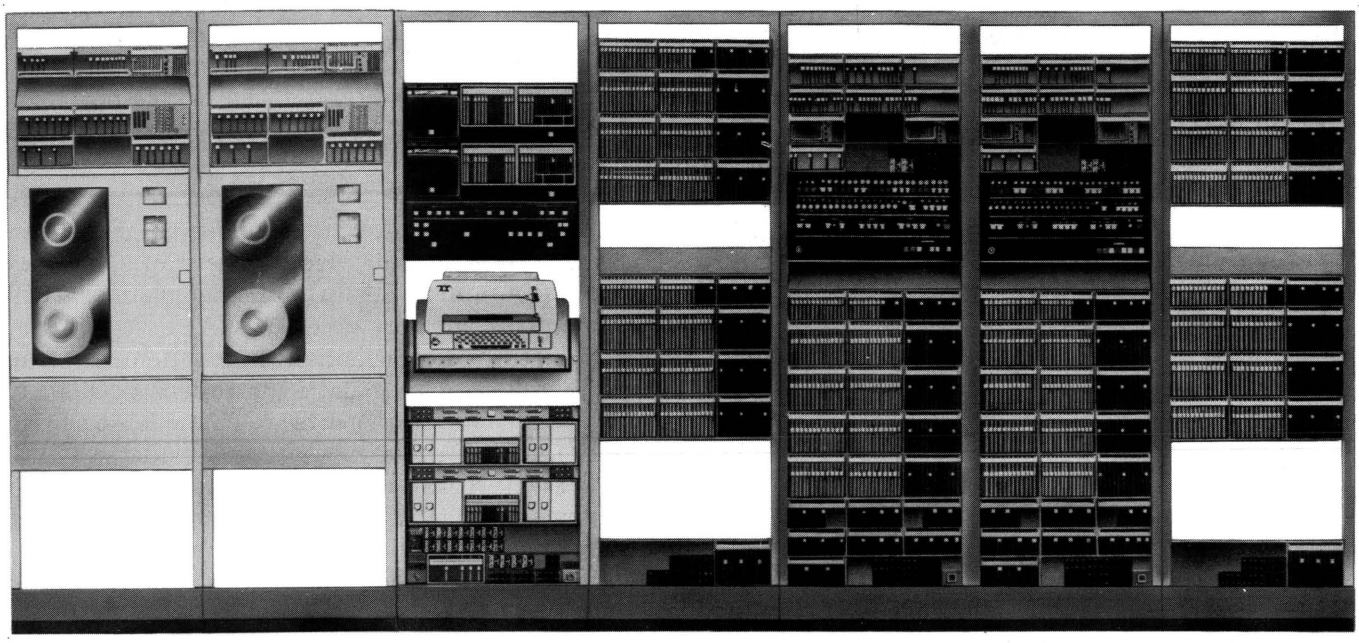


Fig. 1—Typical 3A Processor

available to increase main store capacity to 768K words (Fig. 3). Other options include up to 19 additional serial I/O channels, up to 2 PCH units, and a DMA unit. Duplicate PROMATS are installed to increase system reliability.

1.10 A maintenance frame (Fig. 4) is always included in the 3A Processor, and provides the means by which craft personnel can communicate directly with the CCs and peripheral devices. It contains an E2A telemetry unit (if that option is taken), CTTs 0 and 1, TDCs 0 and 1, system status panel (SSP), a TTY, TTYCs 0 and 1, system status panel controller (SSPC), system status panel relay (SSPR) unit, and related power and alarm circuitry.

1.11 The SSP (Fig. 5) contains lamps and switches to indicate system status, control alarms, and perform manual system initialization. Manual system control can be exercised from the SSP, as well as power and test control.

1.12 The CTT (Fig. 6) located in the maintenance frame provides a nonvolatile semipermanent storage medium for generic programs, nonresident programs, and office data, as well as other information which must not be lost if power failures occur.

1.13 When a system initialization is required, the programs and data required to perform a bootstrap and memory reload are read from a magnetic tape in the CTT. Duplicate CTTs are installed to increase system reliability.

1.14 Tape data controllers (TDC) (Fig. 4) receive commands and data from 3A CC and translate them into formats that cause the CTTs to perform their functions. Detailed information on the TDCs is available in Section 254-300-170, Tape Data Controller, Description and Theory of Operation.

1.15 A TTY (Fig. 4) located on the maintenance frame provides the principal communications interface between a craftsperson and the operating system. Commands and data are inputted to the 3A CC from the TTY keyboard, and system responses, status reports, results of diagnostics, etc, are printed out. One TTY and two TTYCs are normally installed in the maintenance frame. Particular system requirements may result in variation in the quantity and locations of TTYs and their associated controllers. Refer to Section 254-300-190, TTY and TTY Controller, Description and Theory of Operation, for detailed information on these units.

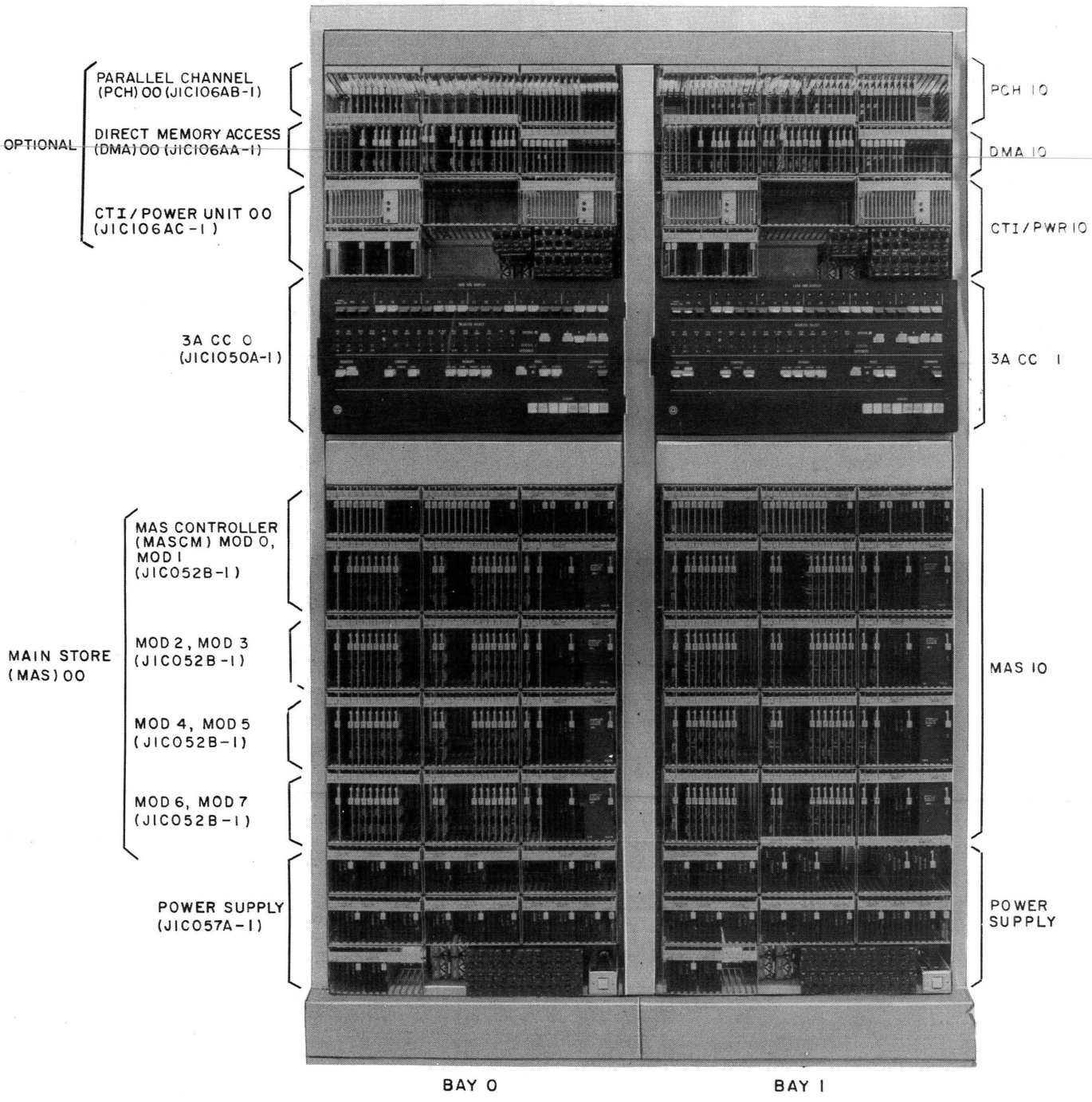


Fig. 2—Typical 3A Central Control Frame

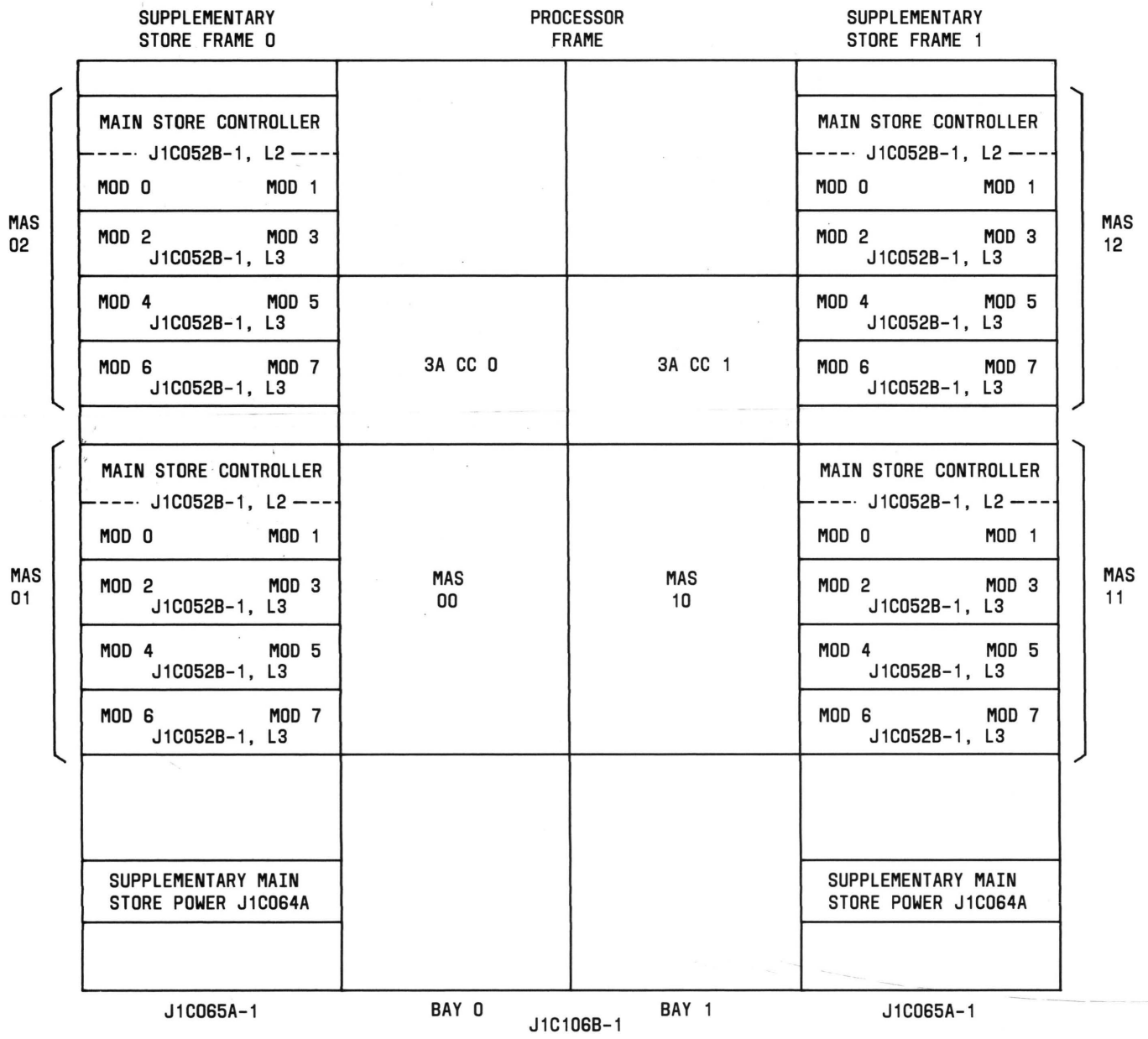


Fig. 3—Supplementary Store Arrangement

1.16 The system status panel controller (SSPC) (Fig. 4) provides the interface between the serial channel output of the 3A CC and the SSP. Outputs from the 3A CC directed to the SSP are buffered and used to light the various lamps and indicators. Operation of the pushbutton switches on the SSP results in generation of messages that are returned to the 3A CC over the serial channel interface. These messages are decoded into appropriate system responses. Section 254-300-180 contains detailed information on the SSPC.

1.17 System status panel relay (SSPR) unit (Fig. 4) contains relays which control system power and provide switch closures to indicate alarm and status conditions. Manual control of the power relays may be exercised from the SSP when manual operation is not inhibited (ie, when the 3A CC is in TEST mode or off-line). Alarm relays are activated by external conditions such as equipment failure, power failure, or high temperature. Other alarm conditions may be sensed, depending on system requirements. Additional information on

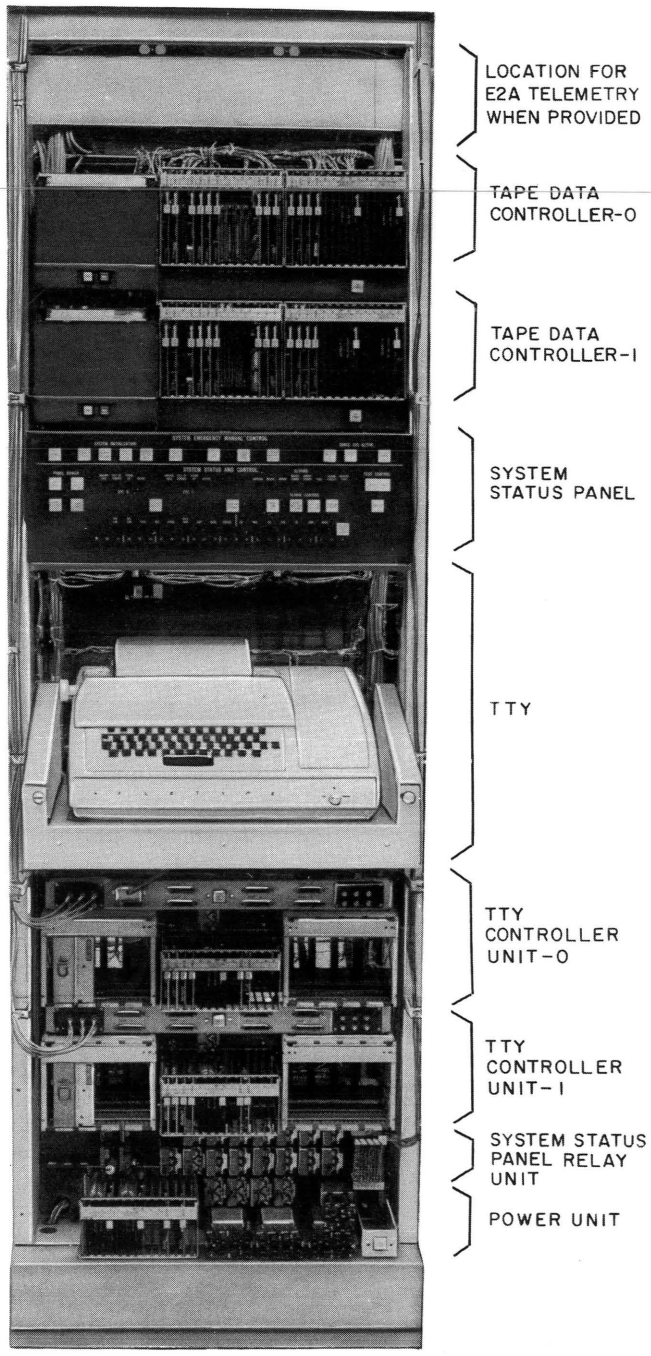


Fig. 4—Maintenance Frame

SSPR is contained in Section 254-300-140, Processor Power System.

1.18 E2A telemetry unit (Fig. 4) is an optional unit which may be installed when the 3A Processor and its associated operating system are to be monitored or controlled from a remote point such as a switching control center (SCC). In this case, system alarm and status conditions are transmitted to the remote location. System control and data transfers are executed by means of a TTY at the remote point.

1.19 The maintenance frame is supplied with -48 volt and +24 volt power from station power. Fuses provide circuit protection and contacts for fuse alarm indications. The dc-to-dc converters in the power unit provide +3 volts for distribution to logic circuitry in the SSP and controllers. Refer to Section 254-300-140, Processor Power System, for additional information on power and alarm circuits.

1.20 PROMATS (Fig. 7) is a semiautonomous magnetic tape system which is designed to require a minimum of control from its parent system. PROMATS accepts data and high level instructions from the peripheral bus interface (PBI), and returns data and status information to the PBI. Decoding of commands, error checking, data formatting, writing on and reading from tape are all controlled by programmable controllers (PROCONs) which are part of PROMATS logic unit. Data is recorded on standard computer tape in a 9 track, 1600 bits per inch phase encoded format.

2. PHYSICAL DESCRIPTION

2.01 The central control processor frame is a double bay frame 7 feet high by 4 feet 3 15/16 inches wide and 1 foot 6 inches deep. Each bay contains a J1C057A processor power and fuse unit, J1C052B main store controller (MASC) and MAS unit, ED-4C006-30 control panel, and J1C050A 3A CC. Optional equipment installed according to system requirements include J1C106AC collector diffusion isolation to transistor-transistor logic interface/power unit (CTI/power unit), one or two J1C106AB, PCH unit, and J1C106AA DMA unit.

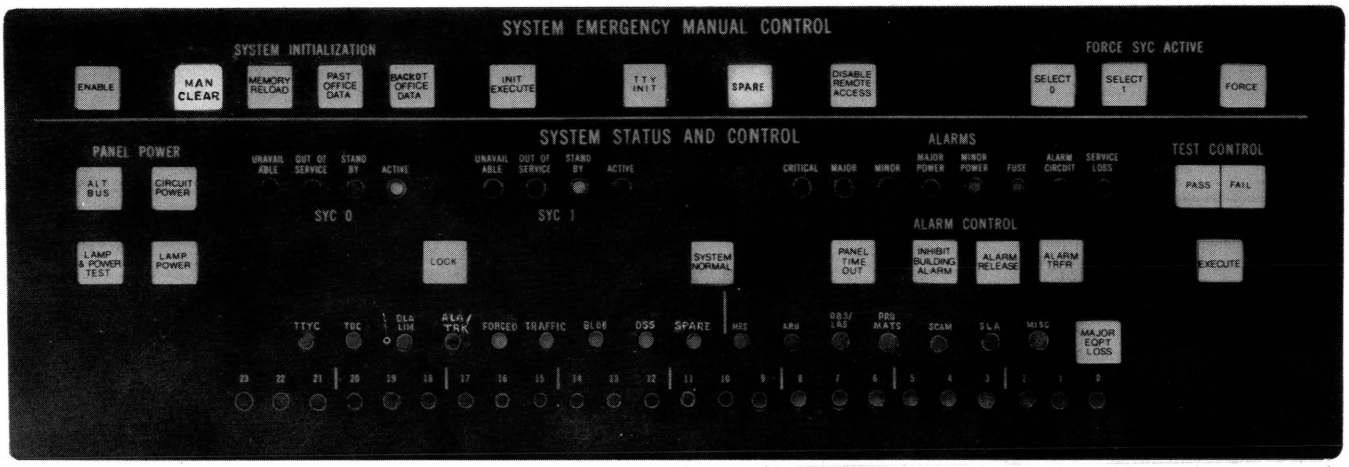


Fig. 5—System Status Panel

PROCESSOR POWER UNIT

2.02 One processor power unit for each 3A CC is located on each bay as shown in Fig. 1.

2.03 This unit is equipped on one 12-inch mounting plate which consists of three levels: 02, 06, and 10. The back of levels 06 and 10 are equipped with multilayer printed wiring board (MLPWBs) and six 347F terminal strips per level. The back of level 02 is equipped with terminal pins, alarm and battery bus bars, a strapping board, resistors, capacitors, and a terminal strip.

2.04 The front of levels 06 and 10 are each equipped with nine 83A apparatus mountings. These mountings may house up to nine dc-to-dc converters which plug into the nine 947C (82-pin) backplane connectors. An FC210 circuit pack is located on level 06, position 44. The front of level 02 is equipped with two 83B apparatus mountings which house two dc-to-dc converters. These plug into two 947C (82-pin) backplane connectors. Also, there are four AK-type relays; 1/2, 1-1/3, and 3 amp fuses; and 72A dummy fuses for the spare positions.

2.05 Connectorized cables from the initial power bay and the miscellaneous power bay pass down through the channel of the frame uprights and through the filter unit located in the base of the frames to provide -48 volts and filtered +24 volts to the processor power unit.

MAIN STORE CONTROLLER AND MAIN STORE

2.06 Equipment, wiring, and apparatus for a MASC and one main store memory (MASM) unit equipped with two memory modules (0 and 1) of 32K each (K=1024, 18-bit words) are concentrated on a 10-inch mounting plate. For the MASC a 4- by 23-inch MLPWB is attached to the rear of the mounting plate, and for the MASM a 6- by 23-inch MLPWB is attached. The 947- and 959-type connectors used for the MASC and the MASM are attached to the front of the mounting plate; they extend through and make contact with their respective terminals on the MLPWBs.

2.07 The MASC consists of three 80C and two 82A apparatus mountings which house 16 FA-type circuit packs, one FC-type circuit pack, and four power converters for the MASC. Designation strips (126A) are mounted on the apparatus mountings to identify the circuit pack located in that position. Terminal strips (347A) are mounted on the MLPWB backplane to interface between the 3A CC and the MASM.

2.08 The MASM consists of three 87A apparatus mountings which house 18 memory and two fan-out circuit packs in both modules 0 and 1. The MASM is also equipped with two power converters. The FC21 +3 volt reference and filter circuit accommodates inputs from two power converters and is located in the MASC unit. A power cable equipped with three plugs connects to the rear of

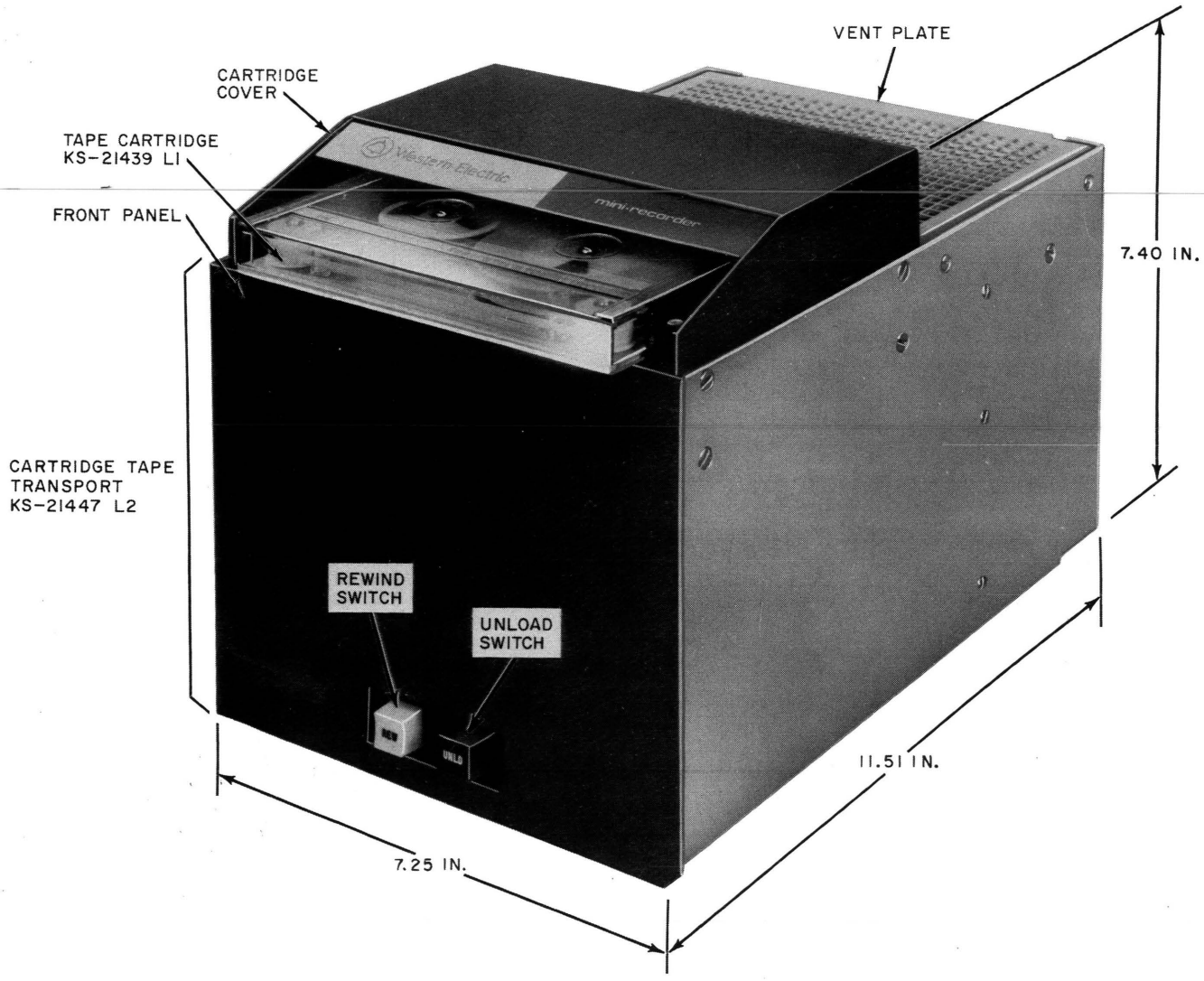


Fig. 6—Cartridge Tape Transport

the MASM providing power from the fuse panel at the bottom of the processor frame.

2.09 The MAS is growable by modules (groups of ten plug-in circuit packs 6 by 7-3/4 inches), each having a capacity of 32K. A 6-inch mounting plate provides space for two modules. The capacity required is determined by the particular application of a 3A Processor. For example, a memory of 64K is provided for an office having a capacity of up to 1152 terminals (up to 3 network frames). A 96K memory is provided for an office of greater capacity. The additional 32K of memory is added when customer growth requires four or more network frames. This occurs when the office capacity exceeds 1152 lines. This growth requires the addition of one MASM equipped with one 32K module, and utilizes an additional 6 inches of vertical space.

2.10 A 3-inch baffle (heat dissipater) occupies the space of a 4-inch mounting plate and is mounted between the 3A CC and the MASC (Fig. 1).

3A CENTRAL CONTROL

2.11 Equipment, wiring, and apparatus for one central control is concentrated on one 12-inch mounting plate located on each frame (Fig. 8).

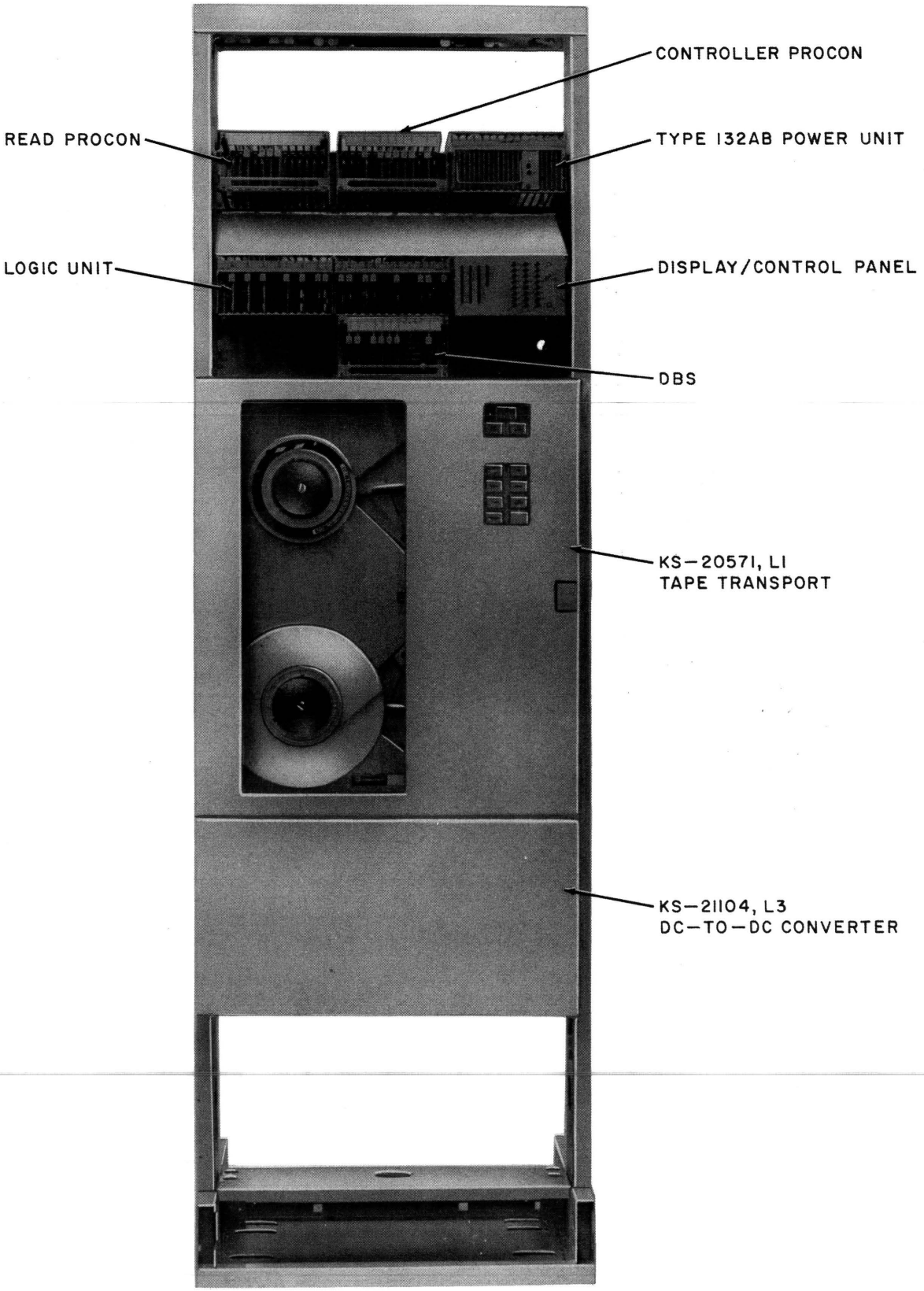


Fig. 7—PROMATS Frame

An MLPWB is attached to the rear of this mounting plate. Eight 80C apparatus mountings are installed on the front of this plate and house the 3A CC plug-in circuit packs. A 12-inch control panel hinged to the side bracket of the 3A CC unit provides access to the circuit packs. Mounted on the front of the panel are status indicator lamps and switches, light emitting diodes (LEDs), register-select, and manual function-select switches. Interconnections between the panel and the 3A CC are made with connectorized flat tape cable assemblies and coaxial cables.

2.12 The 3A CC occupies levels 50 through 62 of the frame. Eight type 80C apparatus housings are mounted on a 12-inch mounting plate to contain the 3A CC circuit packs.

2.13 An MLPWB forms the backplane which distributes power and ground among the circuit packs. Connectors are attached to the MLPWB to receive the circuit pack. Wire wrap connections are made to the backplane connectors by means of pins which project through to the rear of the backplane. In addition, ribbon type cables are equipped with connectors which are plugged onto the pins.

3A CENTRAL CONTROL PANEL (OPTIONAL)

2.14 The control panel (Fig. 9) consists of a 12 inch by 23-1/2 inch panel which is silk-screened with the appropriate nomenclature. The panel includes the following apparatus:

(a) Status indicator lamps and switches

(b) LEDs which display register contents or status information

(c) Register select switches for loading or displaying internal registers

(d) Switches for selecting particular manual functions.

2.15 The panel is mounted to an aluminum frame and has a printed wiring board which supports the apparatus and circuitry necessary for the control panel to function. The entire assembly is hinged to the side brackets of the 3A CC logic unit to provide access to the circuit packs within the unit. Most of the interconnections between the panel and the rest of the 3A CC are accomplished by means of a connectorized flat tape cable assembly. Some interconnections are by coaxial cable.

2.16 The panel is subdivided into the following areas:

(a) LOAD AND DISPLAY

(b) REGISTER SELECT

(c) REGISTER

(d) COMPARE

(e) MEMORY

(f) MODE

(g) COMMAND

(h) STATUS.

2.17 The CTI/power unit (Fig. 10) occupies levels 64 through 71 of the processor frame. One type 80C apparatus housing mounted on the left side of levels 64 through 67 contains circuit packs for the CTI/power unit, while the right side of these levels contains fuses and power relay.

2.18 The upper half of the CTI/power unit, levels 68 through 71, contains three type 80C apparatus housings in which type 132M power converters are installed as required to supply the first and second PCH units and the DMA unit.

2.19 The DMA unit (Fig. 11), when installed, occupies levels 72 through 75 of the processor frame. Three type 80C apparatus housings contain circuit cards which comprise the DMA.

2.20 The PCH I/O unit (Fig. 12) consists of circuit packs located in the upper part of the processor frame. A front-removable 4-inch mounting plate and three 14-card apparatus housings (type 80C) are used. A basic unit is equipped with one set (four) of main parallel channel (MPCH) circuit packs and one set (three) of subparallel channel (SPCH) circuit packs. Additional SPCHs (each SPCH requires three circuit packs) are added, as required, to provide additional capacity for each application. A fully loaded PCH I/O unit contains circuit packs for one MPCH and eight SPCHs. When more than one MPCH is required, a second

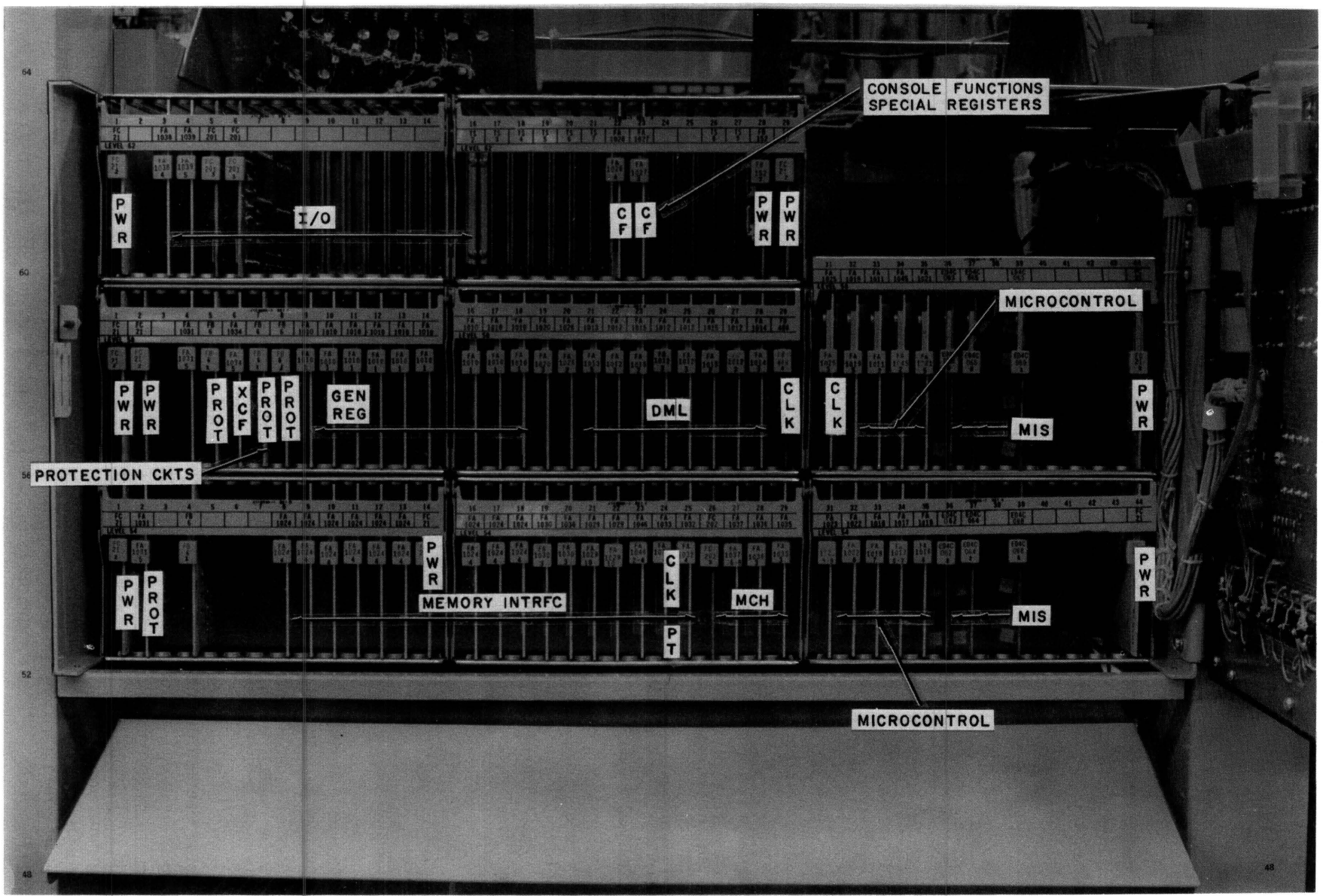


Fig. 8—3A Central Control

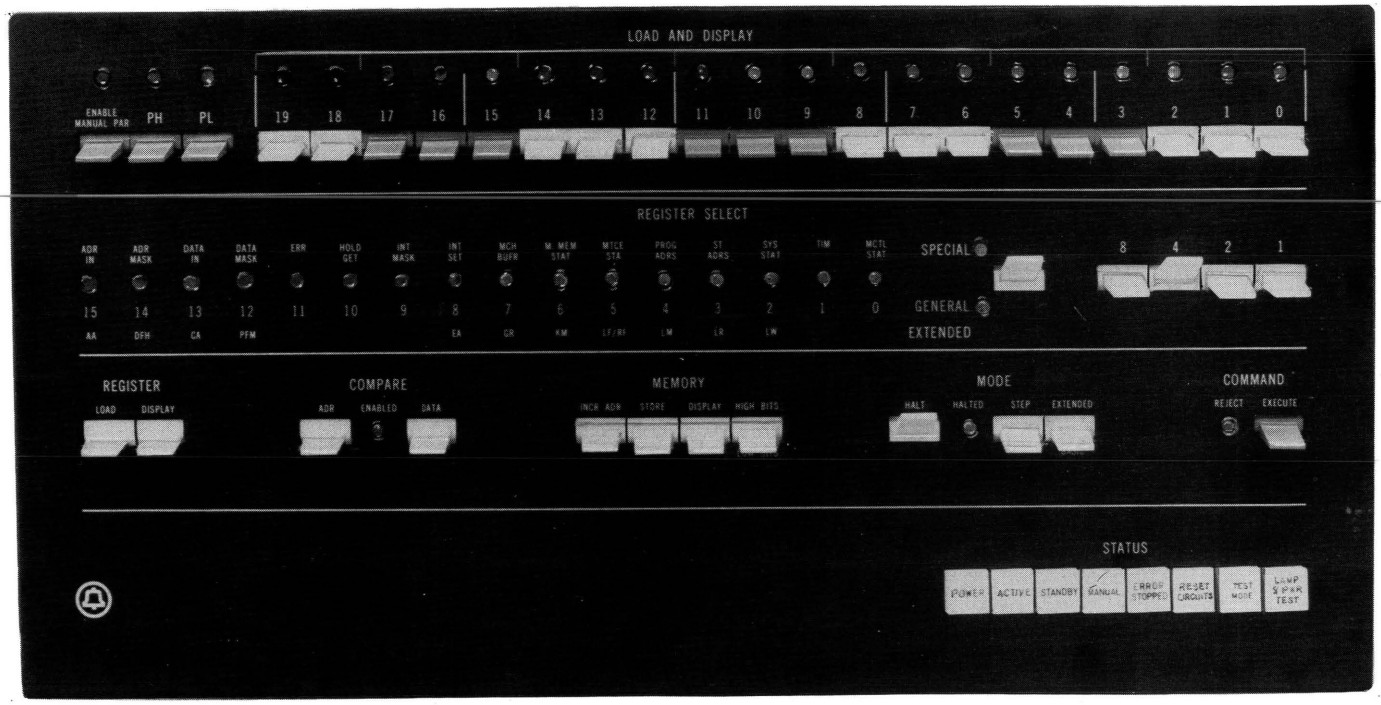


Fig. 9—3A CC Control Panel

PCH I/O unit can be mounted directly above the first unit in the processor frame. Interconnection between the two PCH I/O units and the CTI/power unit is accomplished via tape cable and 942-type connectors. This provides a maximum parallel channel capability for controlling a total of 256 peripheral devices (PDs) (2 MPCHs X 8 SPCHs X 16 PDs = 256 PDs).

2.21 Fig. 13 depicts a typical I/O interface between the 3A CC and its periphery.

MAINTENANCE FRAME

2.22 The maintenance frame (Fig. 4) is a 7-foot high, 2-foot 2-inch wide, single-bay frame. It consists of the following units:

(a) E2A telemetry unit

(b) Tape data controller units

(c) System status panel and system status panel controller units

(d) Teletypewriter and teletypetwriter control units

(e) System status panel relay unit

(f) Maintenance frame power unit.

A. E2A Telemetry Unit

2.23 Assembly, equipment, wiring, and apparatus for one E2A telemetry unit are concentrated on one 8-inch mounting plate. This unit is located on the top of the maintenance frame as shown in Fig. 4. This mounting plate is equipped with circuit packs and a 202T data set mounted in slots provided on the front right side of the mounting plate. The data set is connected to the E2A unit with connectorized cables. The E2A is required with the 3A Processor if it is to be connected to the SCC.

B. Tape Data Controller Units

2.24 Assembly, equipment, wiring, and apparatus for one TDC unit is concentrated on one 8-inch mounting plate. This unit is duplicated and the two units are located on the maintenance frame as shown in Fig. 4.

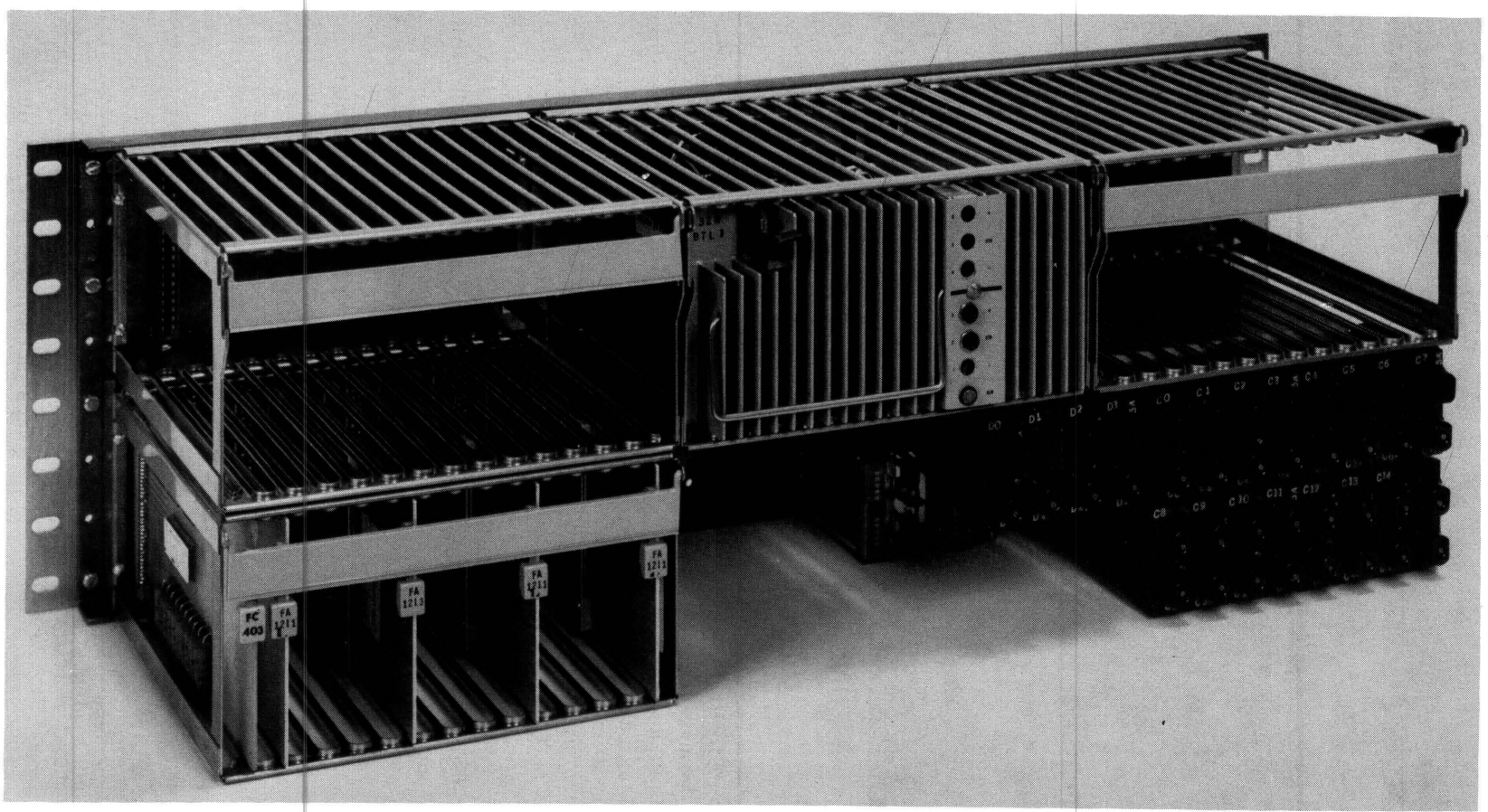


Fig. 10—CTI/Power Unit

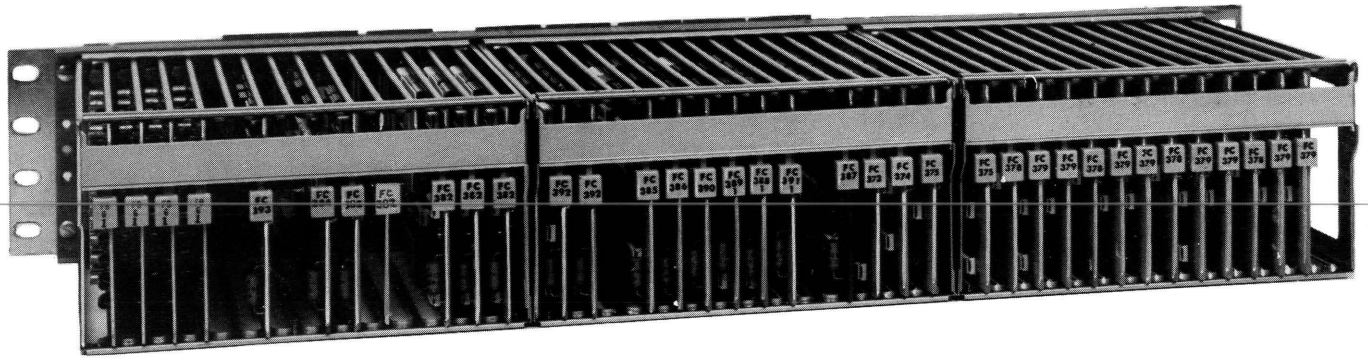


Fig. 11—DMA Unit

2.25 The 87B apparatus mountings house the JK-type circuit packs, and the 130A designation strips identify each JK-type circuit pack and its position. The two dc-to-dc power converters plug into the two 947C (82-pin) connectors. The TDC POWER switch is located on the right side of the switch bracket assembly. CTTs are mounted adjacent to the 87B apparatus mountings.

C. System Status Panel and System Status Panel Controller

2.26 The SSP is 8 by 23 inches and is located on the maintenance frame as shown in Fig. 4. The panel consists of keys, lamps, and LEDs. The SSP is hinged to side brackets on the frame and opens outward to reveal the SSPC. A magnetic latch on the panel keeps it securely closed when not in use. Interconnections between the SSP and SSPC are made with connectorized flat tape cable, twisted pair cable, and coaxial cable.

2.27 The SSPC is 4 by 23 inches and is mounted to the frame in back of the SSP. The circuit packs plug into the 947A and 947C connectors which connect to the MLPWB. The SSPC interfaces with the SSP, SSP relay unit, E2A telemetry unit, 3A CC, and maintenance frame power and alarm circuitry.

D. Teletypewriter and Teletypewriter Control Units

2.28 The TTY is a 35-type or equivalent keyboard send-receive (KSR) and occupies 16 inches of vertical space on the maintenance frame as shown in Fig. 4.

2.29 Equipment, wiring, and apparatus for one TTYC unit are provided on one 8-inch mounting plate. This unit is duplicated and the two units (0 and 1) are located on the maintenance frame. Each TTYC unit houses two TTYCs (left and right). The right controller of either unit is normally not equipped, but can be ordered as an option. The TTYC is equipped with a TTYC POWER-ON button, connector ports 0 through 3 for up to four TTYs, and input or output leads on the coaxial connectors to their associated processor (0 and 1). The left 58C apparatus mounting houses up to four port interface circuit packs (which may be AR17s or 108Ds in any combination). The 80C apparatus mounting houses controller logic and power circuit packs.

E. System Status Panel Relay Unit

2.30 Assembly, equipment, wiring, and apparatus for one SSP relay unit are concentrated on one 4-inch mounting plate located on the maintenance frame. The mounting plate consists of fourteen AF10 relays, one AK30 relay, four 278A terminal strips, and one 288M terminal strip.

F. Maintenance Frame Power Unit

2.31 Assembly, equipment, wiring, and apparatus for one maintenance frame power unit are concentrated on one 4-inch mounting plate located on the bottom of the maintenance frame as shown in Fig. 4. Two dc-to-dc converters plug into two 947C (82-pin) connectors equipped with two 83B apparatus mountings. The two FC210 circuit packs and one terminal strip plug into three 947C connectors equipped with three 82B apparatus mountings. Also mounted on the front of the

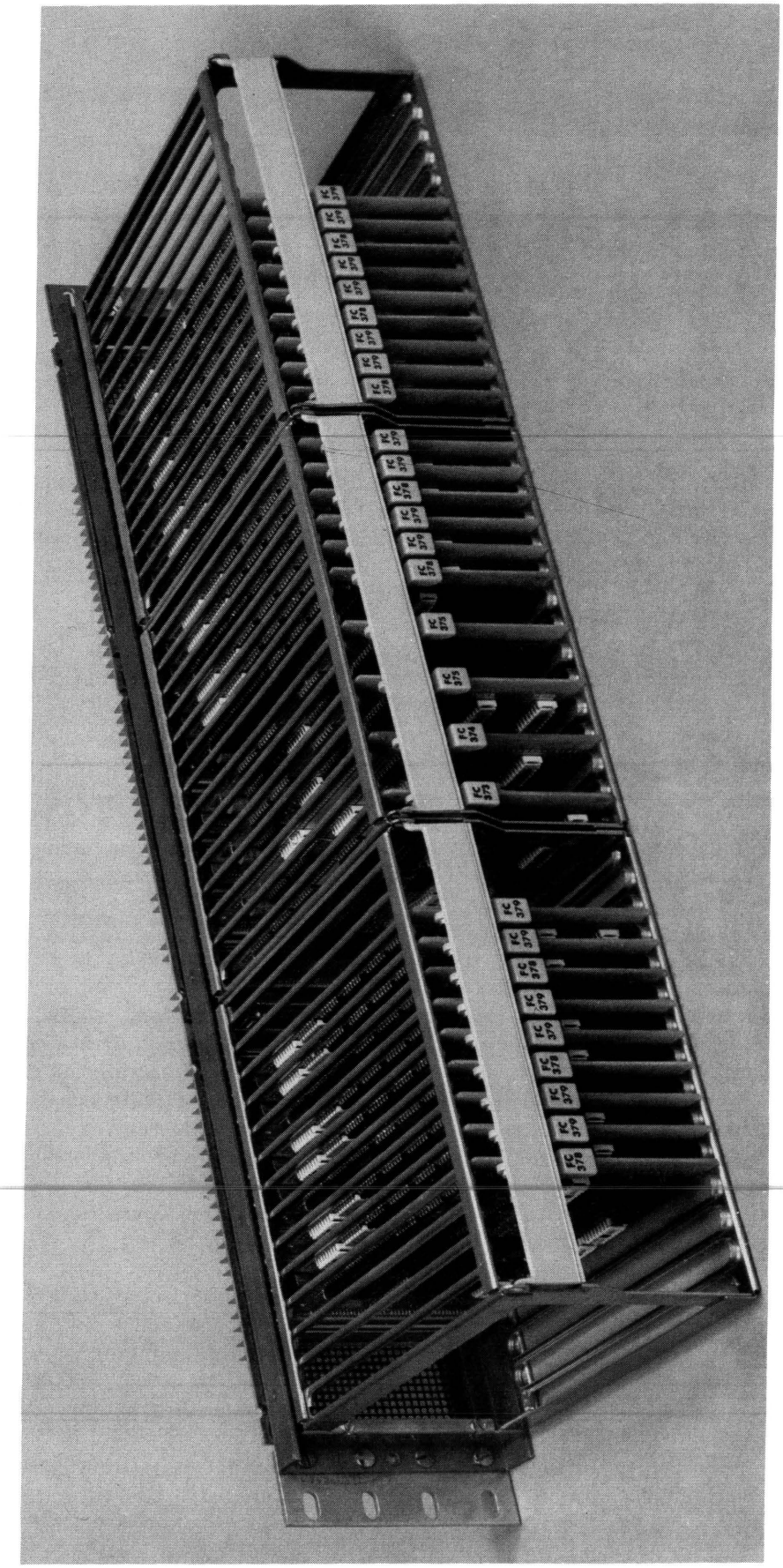


Fig. 12—PCH Unit

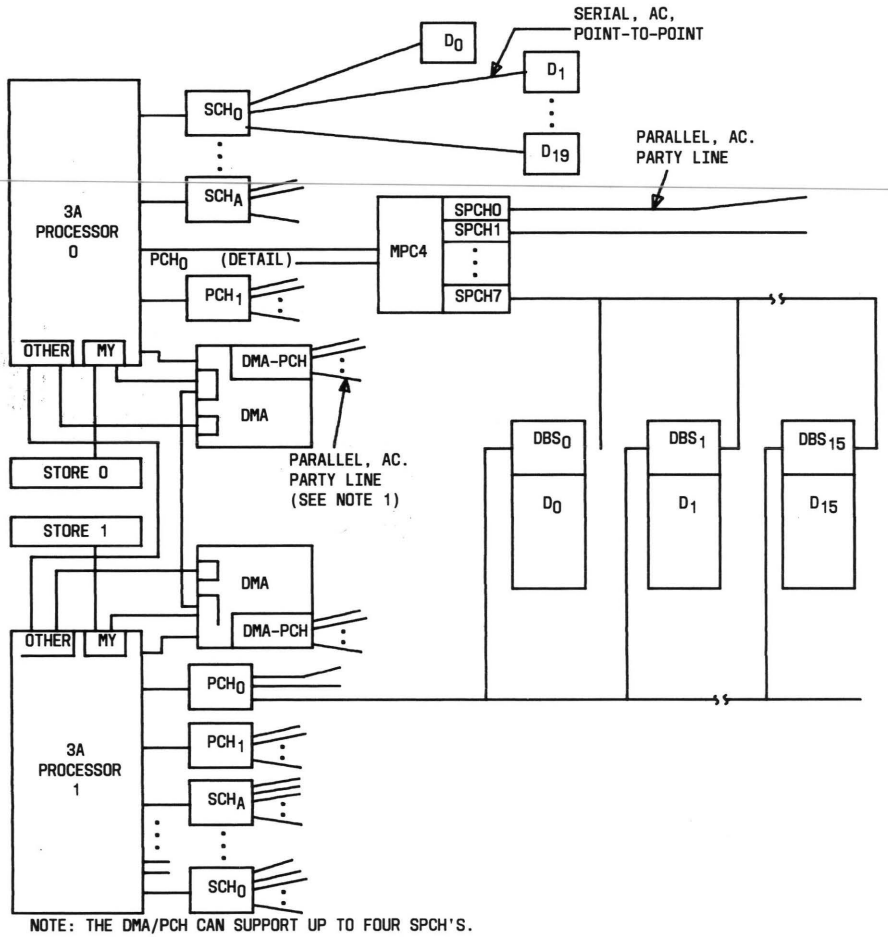


Fig. 13—Typical I/O Interfaces

mounting plate are four AK30 relays, two terminal blocks, power and reset switch, A and B bus bars supplying +24 volts and -48 volts to 1/2 and 1-1/3 amp 70-type fuses.

2.32 Connectorized cables from the initial power bay and miscellaneous power bay pass down through the channel of the maintenance frame upright and through the filter unit located in the base of the frame to supply -48 volts and filtered +24 volts to the maintenance frame power unit.

PROGRAMMABLE MAGNETIC TAPE SYSTEM

2.33 The PROMATS (Fig. 7) is installed in a standard 2-foot, 2-inch wide by 7-foot high single bay frame and consists of the following units:

(a) J99384AA PROCON unit located at levels 71 through 75 of the frame

(b) J99384AB logic unit located at levels 63 through 67 of the frame

(c) J99384AC I/O unit located at levels 59 through 63 of the frame

(d) KS-20571 tape transport located at levels 30 through 59 of the frame

(e) KS-21104 power supply (dc-to-dc converter) located at levels 18 through 30 of the frame.

PROGRAMMABLE CONTROLLER

2.34 The PROCON unit J99384AA (Fig. 7) consists of a J1C082B read PROCON, a J1C082A L20 controller PROCON, and an associated type 132AB power supply located in a 4-inch mounting plate assembly. The PROCON unit occupies levels 71 through 75 in the PROMATS frame. The PROCONs

are 16-bit microprocessors whose functioning is controlled by a series of instructions read from microstore (a fixed, nonvolatile read only memory) which is an integral part of the PROCON. The read and controller PROCONs are essentially identical, differing principally in the amount of self-checking ability provided, the quantity of microstore furnished, and the instructions encoded in the microstore. High-level instructions (from the 3A CC or DMA channels) are translated into detailed instructions by PROCONs and used by PROMATS to execute each task.

2.35 The PROCONs consist of integrated circuit packages mounted on multilayer etched circuit boards. The circuit boards, usually referred to as "circuit packs," are connected to the multilayer printed wiring backplane via 80-pin connectors. The circuit packs are contained in a 12-card housing similar to the ESS type 80-card housing. Power and ground connections to the packs in the housing are made through the various layers in the backplane. System interconnects are made by multipin connectors and tape cable.

2.36 The read PROCON is equipped with the fast clock (500 nanoseconds) and 1K of microstore memory. It uses two data manipulation cards, one 16-bit control unit card, and one program storage unit card.

2.37 The controller PROCON is equipped with the fast clock and 2K of microstore memory. Its card complement consists of four data manipulation cards, one 16-bit control unit card, and two program storage unit cards.

LOGIC UNIT

2.38 The J99384AB logic unit (Fig. 7) consists of 16 circuit cards and an ED-97810 control and status display panel assembly mounted in three 14-card housings located at levels 63 through 67 in the PROMATS frame. The logic unit provides the internal interfaces from the tape transport unit to the read and write PROCONs, the duplex bus selector (DBS), and the local control panel. The logic unit:

- Receives and decodes commands from the external system
- Receives and formats data to be recorded by the tape transport
- Provides error detection capability
- Provides status report capability
- Processes analog signals (read from magnetic tape) into digital format for use by the parent system.

INPUT/OUTPUT UNIT

2.39 The J99384AC I/O unit (Fig. 7) consists of a J1C107A DBS unit located in the center third of a standard 4-inch mounting plate. The DBS includes one FC398 circuit pack, one FC399 circuit pack, one FC400 circuit pack, three FC401 circuit packs, and one FC402 circuit pack. These packs are located in equipment locations 18, 19, 21 through 24, and 29, respectively. The DBS is used to provide the interface between the PROMATS and the data buses from the duplicated 3A CCs.

TAPE TRANSPORT

2.40 The KS-20571 tape transport (Fig. 7) occupies levels 30 through 59 of the PROMATS. It serves as the recording and reproducing medium for digital data supplied to and from the peripheral devices. The tape transport uses standard 1/2 inch wide magnetic tape and accommodates reels up to 10-1/2 inches in diameter. Data is recorded as phase-encoded signals at 25 inches per second and 1600 bits per inch. A 9-track format is used.

2.41 The tape transport contains only the electronic circuits that control the mechanical operation such as drive motors, solenoids, and relays. The circuitry for the read, write, and erase heads is contained in the logic unit.

2.42 A control panel (Fig. 7) is provided on the tape transport so that local control of the tape motion can be exercised for maintenance purposes or for loading or unloading tapes.

POWER SUPPLY

2.43 The KS-21104 power supply (Fig. 7) for the tape transport is located in levels 18 to 30 of the PROMATS frame. It is a dc-to-dc converter that converts the standard -48V primary power into +5V at 3.5A, +15V at 4.5A, and -15V at 1.5A for the tape transport electronics and +15V at 4.5A, -15V at 4.5A, and -24.5V at 14.0A for the mechanical operations. Over- and under-voltage

and over- and under-current sensors and protective circuits are included in the power supply.

3. 3A PROCESSOR INTERFACES

3.01 The 3A Processor communicates with its parent system over serial and parallel I/O channels. Information is transferred between the 3A Processor and low speed data devices over the serial channel at a rate of 6.67 megabits per second. High speed devices communicate over the parallel channel transmitting or receiving a full 18-bit word at a time. In addition, high speed transfers of blocks of data may be made to and from MAS over the DMA channel when that option is installed.

3.02 The addressing capability of the 3A Processor is such that it can address up to 400 devices on the serial channels. Two parallel channels may be installed, each of which may contain eight subparallel channels. Since 16 devices may be connected to a subparallel channel, up to 256 devices may be addressed. Up to 64 devices may share the DMA channels.

3.03 I/O operations are conducted under program control through general registers R9, R10, and R11 in the 3A CC. Register R9 contains the device address and control data, R10 contains output data, and R11 receives input data from the peripheral device. Contents of these registers are placed on the serial leads a bit at a time, or on the parallel bus a word at a time. Although the 3A Processor can address a large number of peripheral devices, actual communication takes place with only one device at any one instant in time.

3.04 When the 3A Processor is equipped with a DMA channel, high speed transfers of blocks of data can take place between MAS and peripheral devices such as magnetic tape transports. The 3A CC establishes the channel and conditions of transfer, then the DMA unit functions autonomously to perform the operation without further intervention by 3A CC. This system minimizes the time that the 3A CC must devote to a routine repetitive task. Fig. 14 is a block diagram of 3A CC, and Fig. 15 is a block diagram of a typical use of the 3A Processor.

3.05 Each 3A CC in a duplicated 3A Processor installation communicates with the other 3A CC over a dedicated channel for diagnostic and maintenance purposes. Each 3A CC also accesses MAS in the other processor as well as its own MAS so that the on-line 3A CC keeps both MASs updated. This is done in order to maintain a duplicate file of information in case a fault occurs in the on-line MAS. Fig. 16 is a block diagram of typical 3A Processor interfaces.

4. FUNCTIONAL DESCRIPTION

3A CENTRAL CONTROL

4.01 The 3A CC is the control unit of a 3A Processor. The 3A CC (as well as some other units of the system) is duplicated to provide continuous real-time operation with a high degree of system reliability. It uses instructions and data stored in main store to direct and control messages as well as to aid in detecting and analyzing improper performance of the equipment involved. One 3A CC always has active control over the system while the other 3A CC is in a standby mode. The on-line 3A CC keeps both the on-line and standby memory up-to-date so that the standby 3A CC can assume control of the system with an up-to-date storage area in case of a failure in the on-line machine.

4.02 Since the 3A CC controls the operation of the 3A Processor, it must be able to communicate with various units within the system. This communication involves the sending/receiving of information to/from peripheral units. "Peripheral units" may include other 3A Processors or other processors which may be at remote locations.

A. Communications Functions of 3A Central Control Within 3A Processor

4.03 Functions performed by the 3A CC in relation to MAS are reading from or writing into a memory location. These functions are performed between 3A CC and MAS over the MAS bus.

4.04 The cartridge tape system of 3A Processor contains certain software not stored in MAS and a backup for the software stored in MAS. Therefore, the 3A CC must access or communicate with the tape system and perform the functions of reading the tape contents or writing information onto the tapes. These functions are performed between the 3A CC and the tape system over a serial I/O subchannel.

4.05 The TTY and SSP provide an interface between operating personnel and the system. The 3A CC must communicate with the TTY to perform the functions of outputting characters to the TTY and receiving input characters from the TTY. The 3A CC must also communicate with the SSP to perform the functions of sending status information to the SSP and receiving requested panel operations. These functions for both the TTY and SSP are performed over serial I/O subchannels.

4.06 Since the 3A CC is duplicated, both 3A CCs must be able to communicate with each other. This communication is over the maintenance channel. Refer to Section 254-300-120, 3A Central Control, Theory of Operation, for a detailed explanation of the maintenance channel and maintenance channel controller.

B. Communications Functions of 3A Central Control in Relationship to Periphery

4.07 For the 3A Processor to provide proper service, the 3A CC must communicate with and control the periphery. This communication is over parallel I/O subchannels as well as serial I/O channels and may perform such functions as polling of transaction terminals and transfer of data to and from a data bus.

C. Functional Sections Within the 3A Central Control and I/O Interface

4.08 The block diagram in Fig. 14 shows the functional sections within the 3A CC. These sections are:

- 3A CC system clock
- General registers
- Microprogram control
- Data manipulation
- Interrupt facility
- Processor bus controller
- Serial I/O channels and controllers
- Parallel I/O and DMA channels
- Maintenance channel and controller
- Control panel interface
- Gating bus and bus parity checker
- Miscellaneous registers.

3A CC System Clock

4.09 The 3A CC system clock supplies the basic timing pulses necessary to control system actions. Each timing pulse is nominally 37.5 nanoseconds in duration. Four of these pulses make up one cycle of 150 nanoseconds. Timing pulses are used for controlling various system functions such as data timing, gate control, synchronization of events, etc.

4.10 The 3A CC system clock contains counters, timers, and a clock signal generator. The basic timing signal is generated by a standard crystal oscillator and squaring circuit. The crystal oscillator generates a sine wave which is then passed through a squaring circuit to generate a square wave with a period of 37.5 nanoseconds. By the use of a flip-flop and combinational logic, four clock phases are generated. Every cycle of 150 nanoseconds, a 10-bit counter within the clock is incremented by one. This 10-bit counter indirectly increments the timing counter (TC) and program timer (PT). The TC is used to generate timed interrupts for software use and to increment the PT. The PT is an overall system sanity check for both hardware and software faults.

3A CC Registers

4.11 The central control registers provide quick access storage media for data being stored in a current data processing operation. The two basic types of registers in the 3A CC are as follows:

- General registers
- Special registers

The general register organization provides for flexibility in data handling and processing. The general registers are designated R0 through R15. Each general register stores 18 bits: 16 bits of data and 2 parity bits (parity on bits 0 through 7 and parity on bits 8 through 15).

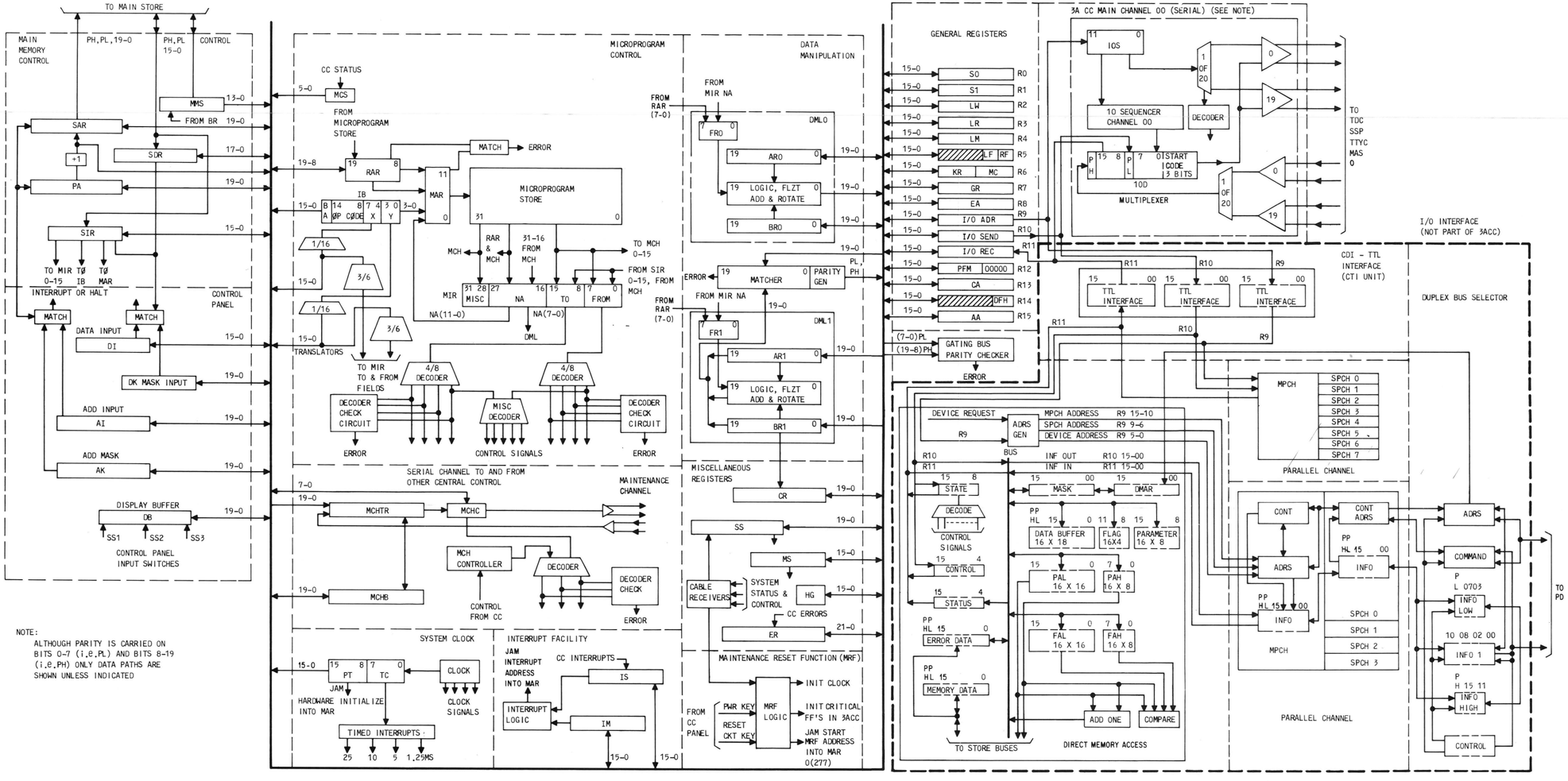


Fig. 14—3A CC Block Diagram, Including I/O Interfaces

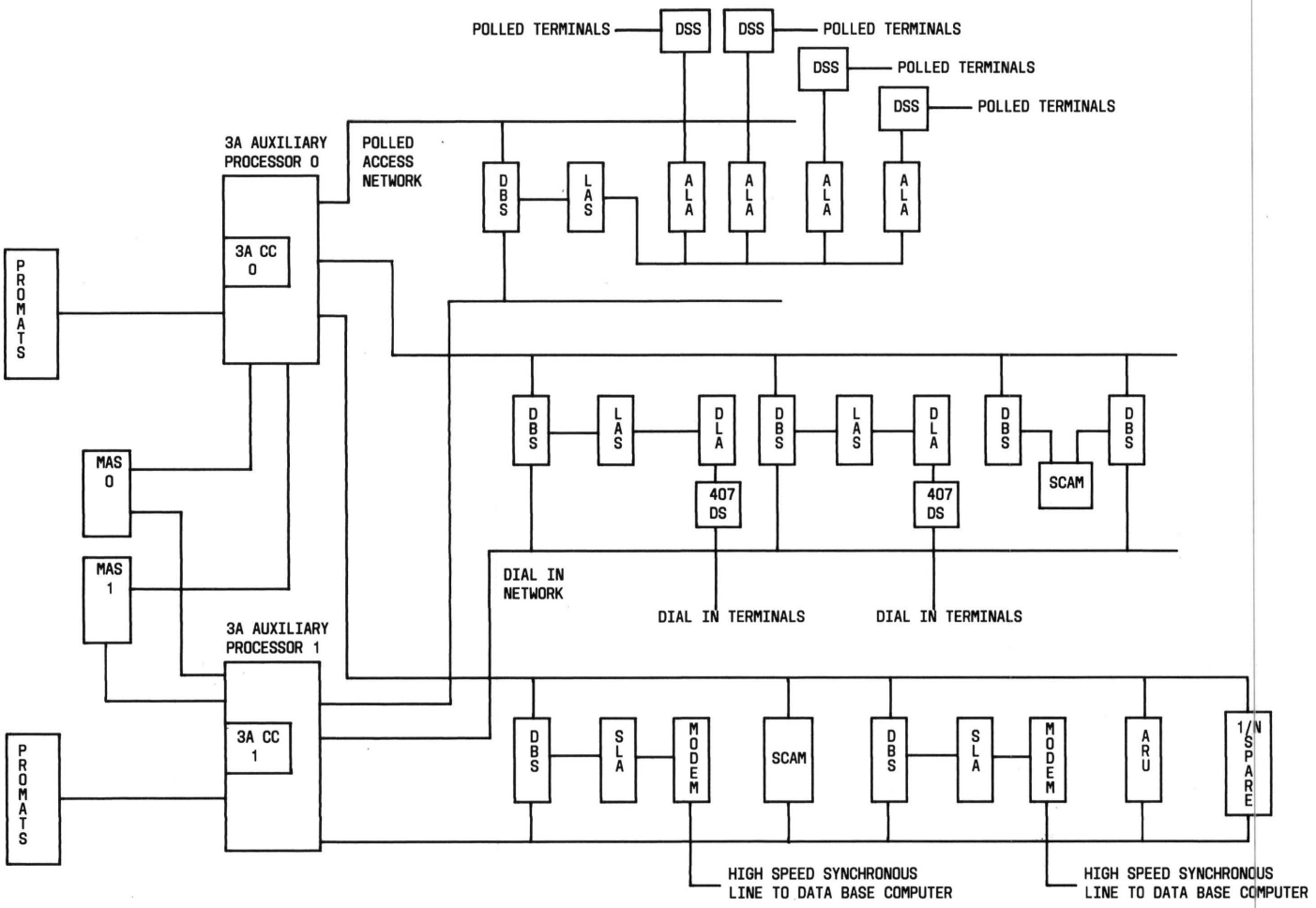


Fig. 15—TN Block Diagram

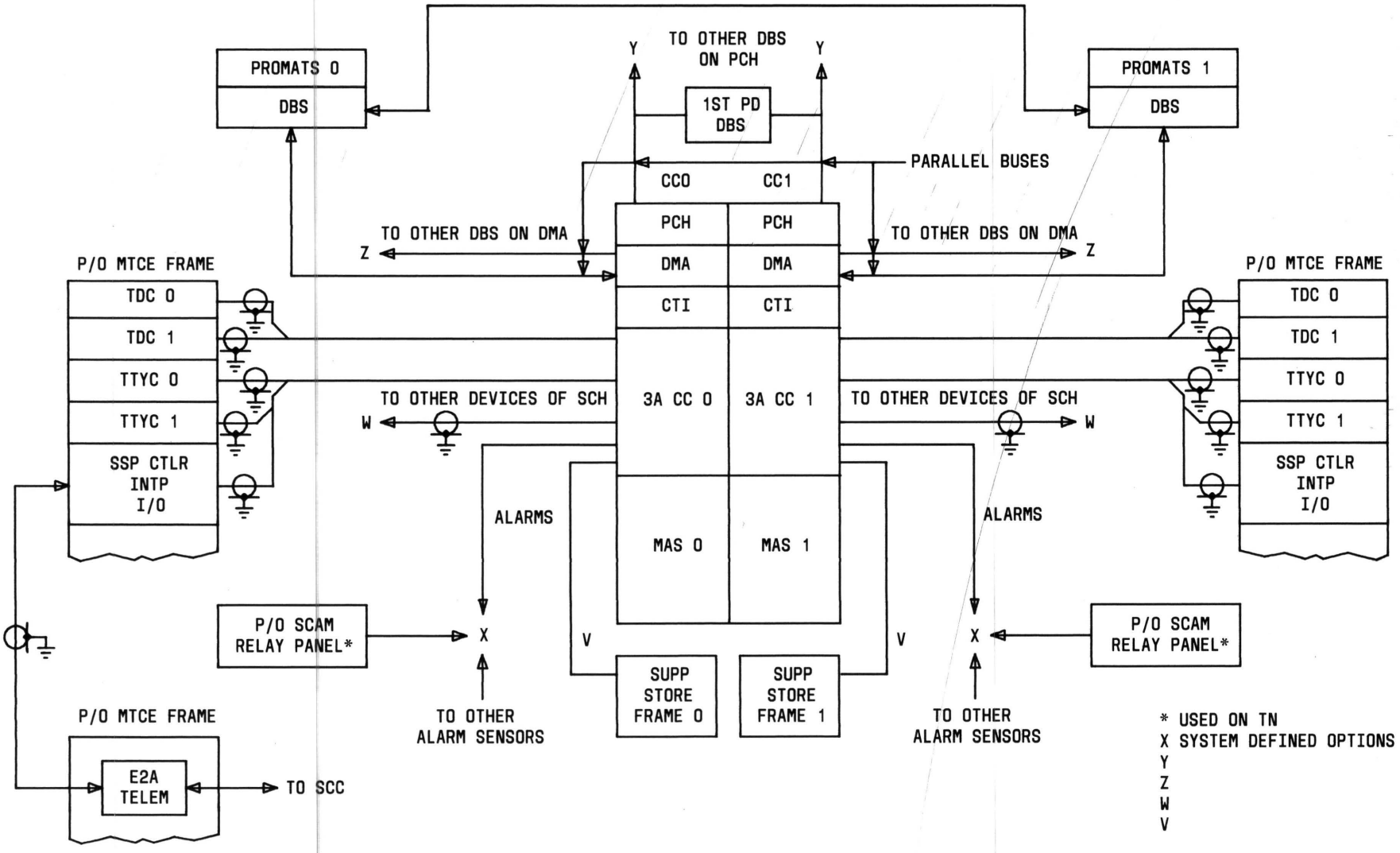


Fig. 16—Typical 3A Processor Interfaces

4.12 Since an address for the 3A CC consists of 20 bits, a pair of general registers may be utilized to address memory. Instructions are available in the extended operating system which permit the use of any even-odd register pair as address registers.

4.13 General registers R9, R10, and R11 serve particular functions concerning the I/O:

(a) R9 as a buffer for the address of the peripheral device

(b) R10 for the data to be sent to the peripheral device

(c) R11 for the results or data received from peripheral devices

When these registers are not being used for their I/O functions, they are used as general registers.

4.14 The special registers are dedicated to specific functions and, depending on those functions, may vary in length, eg, 22-bit store address register (SAR) and 18-bit store data register (SDR). Special registers are not shown as a separate functional section but form a part of the other functional sections in which they are used. Only 16 of the special registers may be displayed, loaded, or accessed by operation of the control panel. These are shown in the REGISTER SELECT area on the front of the 3A CC panel.

Microprogram Control

4.15 The microprogram control is the center of the 3A CC operation. It directs and controls the operation of all the other functional sections within the 3A CC. The microprogram control consists of a microstore, several special registers, decoders, translators, logic, and check circuits. The microstore is a programmable read only memory (PROM) type permanent memory which contains both the discrete steps (microinstructions) necessary to carry out main store program instructions and certain special functions, such as initialization, control panel sequences, interrupt recognition, etc. The special registers are for status, microstore address generation, and microinstruction interpretation purposes. Microcontrol status saves certain status states (I/O status, memory data ready, etc) and utilizes their value to modify addressing of microinstructions. Typically, an MAS instruction is used to address, via a microstore address register, a set of microinstructions which will implement the function specified by the instruction. This begins a microsequence, composed of microinstructions. Each microinstruction commands, through the instruction register and decoders, one step of the sequence. The microinstructions also contain a next instruction address field which progresses the sequence until the required function is completed. During the decode portion of a sequence, check circuitry verifies that the correct control signals to other 3A CC circuits were generated.

Data Manipulation

4.16 The data manipulation area provides the special registers, matcher, parity generator, and logic necessary to perform such functions as addition, rotation, logical combinations (Boolean functions), and find low zero.

4.17 The data manipulation area contains duplicated data manipulation logic (DML 0 and 1). Information is gated into both DMLs via the gating bus. After both DMLs perform the desired function, the results are compared by the matchers. Parity is generated on all DML results by a parity generator atached to DML 1. This parity generator supplies parity to the gating bus. Data is supplied to the bus by DML 0. The data manipulation output will then interface with the rest of the system.

4.18 Each DML consists of a function register, an A register, a B register, and combination logic. The function register provides the control information used by the DML to perform the desired function. Registers A and B buffer the data to be manipulated. The combinational logic is used to perform the functions indicated by the function register on the data A and/or B registers.

Interrupt Facility

4.19 The interrupt facility provides the means of breaking into the program flow so that a timed or more urgent task may be performed. The interrupt facility consists of two special registers (interrupt set and interrupt mask) and interrupt logic. This facility enables any desired input to the 3A CC to be recognized and serviced relative to its priority. Interrupts may be caused by such inputs as TTY messages, control panel operations, TC signals, certain error conditions, and interrupt

requests from peripheral devices or software instructions.

Processor Bus Controller

4.20 The central control store bus controller is the means or interface by which information is transmitted to or received from the main memory. The central control store bus controller contains special registers (main memory status register, program address register, store address register, store instruction register, and store data register) which buffer:

(a) Data or instructions from main memory for use within the 3A CC

(b) Data to the main memory location defined by SAR for storage

(c) Address of present and last program word fetched from memory.

Serial I/O Channels and Controllers

4.21 The serial I/O main channel contains a controller which may control up to 20 subchannels. The serial I/O channel controllers are the interface by which information is communicated between the 3A CC and the tape cartridge controller, system teletypes, and the SSP. A serial I/O channel controller consists of special registers (I/O status register and I/O data register), sequence and control logic, decoders, bipolar drivers/receivers, and error check circuits.

Parallel I/O and DMA Channels

4.22 The 3A Processor may be equipped with one or two parallel channel I/O units and one DMA unit. These units form the interface between 3A CC and high speed peripheral devices which access the parallel bus.

4.23 DMA provides a means of transferring blocks of data between MAS and high speed peripheral devices with minimal supervision by 3A CC. The DMA unit controls all details of a data transfer while the 3A CC initiates a transfer by identifying the device, number of words to be transferred, and beginning and ending MAS address.

Maintenance Channel and Controller

4.24 The maintenance channel (MCH) is an asynchronous, semiautonomous data transfer system capable of serial ac data transfers at a rate of 6.67 megabits per second. It provides a half-duplex mode (one-way transmission at a time) of communication between the duplicated 3A CCs. This communication is necessary for one 3A CC to determine the state of the other and for the on-line 3A CC to exercise the other 3A CC as well. The MCH controller of the on-line 3A CC is used to perform the following functions in relation to the other 3A CC.

(a) Periodic auditing of central control off-line status

(b) Periodic or diagnostic exercise

(c) Stopping

(d) Starting or initializing

(e) Updating the program timer

(f) Disabling the serial I/O

(g) Controlling the clock.

4.25 The MCH controller consists of special registers (transmit/receive register, command register, and buffer register), sequence and control logic, error check circuits, bipolar drivers/receivers, and a command decoder.

Control Panel Interface

4.26 The control panel is one of the means for communications between maintenance personnel and the 3A CC. The control panel interface consists of special registers (three switch registers, display buffer, data input register, data mask register, address input register, address mask register), matchers, and interface logic.

Gating Bus and Bus Parity Checker

4.27 The gating bus is the communications path within the 3A CC. Most information is transferred between functional sections of the 3A CC via this gating bus. The bus parity checker tests the parity of the information placed on the gating bus to ensure its accuracy.

Miscellaneous Registers

4.28 Within the miscellaneous section, a group of special registers and cable receivers are present. The cable receivers provide a means for receiving information from the SSP. The special registers provide:

(a) A hardware-assisted subroutine facility (hold-get register)

(b) A buffer for error signals (error register)

(c) A buffer for status and control information (system status register)

(d) A buffer for testing purposes (maintenance state register)

(e) A buffer used as a scratch area by the microprogram (C register).

D. Power

4.29 The 3A CC is not equipped with its own power supply. Power converters in the processor frame power unit must supply the following voltage inputs to the 3A CC:

(a) 3 volts (used in 1A logic)

(b) 5 volts (used in microstore, clock oscillator, panel LEDs)

(c) In addition +24 volts is provided via the power unit for use in the control panels and as reference and sensing for 3-volt regulator.

E. Maintenance

4.30 Three functions are involved in the maintenance of 3A Processor.

(a) Fault detection is the first and most important function in realizing a highly reliable system.

(b) After detection of a fault, rapid recovery of the system must occur to ensure the protection of messages in progress and the continuation of processing functions.

(c) After recovery, the fault must be diagnosed and isolated to the unit in trouble for replacement purposes.

F. Fault Detection

4.31 Fault detection is accomplished by hardware and/or software. The 3A CC is designed to be a self checking unit utilizing error checking techniques such as:

(a) ***Bit-Slicing:*** The 3A CC uses 2-bit slicing to aid in the detection of errors, especially in areas such as the general registers. Two-bit slicing means that two bits of each register are on a single circuit pack. For example, the first circuit pack contains bits 0 and 8 of every general register. This is done so that a fault will affect at most only two bits of any register and should cause a parity error which would be immediately detected by the parity checking circuits.

(b) ***Parity Check:*** Each word used in the 3A CC contains 18 bits (16 data and 2 parity bits). A parity bit is associated with 8 other bits in a 16-bit word to make the total number of ones, including the parity bit, odd. Parity checks are used throughtout the 3A CC. Each time information is transferred from one location to another via the gating bus, a parity check is performed in the gating bus parity checker. Whenever incorrect parity is found, an error is indicated.

(c) ***M-Out-of-N Codes:*** M-out-of-n codes are used throughout the 3A CC to provide maximum error detection capability. M-out-of-n means that "m" ones should be present in "n" bits. For example, 4-out-of-8 means that exactly 4 ones will always be present. The associated decoder check circuits verify that the number of ones is correct. If an incorrect code is detected, an error is indicated.

(d) ***Duplication:*** Duplication of units, such as in the data manipulation logic, is another means used in the 3A CC to detect faults. Duplicated units are given the same inputs. Their outputs are then compared to verify their correctness. When the two outputs differ, an error is indicated.

(e) ***Periodic Detection Tests:*** Since the 3A CC uses self-checking circuits, its fault detection is adequate only as long as the check circuits work properly. A combination of hardware and software is used to verify that the check circuits provide an indication when a fault occurs.

Hardware provides a means of simulating test conditions or circuit faults. By appropriately setting up the test conditions and applying a well-designed test sequence, the detection circuitry is checked on a periodic basis.

(f) ***Program Timer:*** Although the 3A CC is designed to be self-checking, an overall system sanity check for both hardware and software is provided by the program timer. The use of the hardware timer is closely related to the system program. A reset is generated for the timer only if the program proceeds through the normal program loop correctly within the prescribed period. If the program deviates from the normal course or the 3A CC halts, no reset is given. The timer automatically times out, stops processing, and starts the recovery process.

G. Recovery

4.32 After the detection of a fault, the system must quickly and automatically recover itself to a point or condition where it can again function to process messages. The error signals that result from the detected faults are buffered in the error register of the 3A CC. These signals are sorted and divided into four groups with each causing a different set of system actions.

(a) ***Interrupts:*** This is the least severe of the three since the on-line 3A CC maintains complete control. Error signals that cause this action are usually associated with the I/O facility or MCH.

(b) ***MAS Read Parity Error:*** Invokes either double store read or complement correction depending on system status when the error occurs.

(c) ***Initialization:*** This action is a restart of the 3A CC in a particular state. Error signals that cause this action are usually caused by software errors.

(d) ***Switch to Other 3A CC:*** This action changes control from one 3A CC to the other due to a fault in the on-line system.

4.33 Although the system is designed to automatically recover itself under trouble conditions, certain software or hardware faults or combinations of the two may occur in which the system is unable to configure into a working mode, eg, continuously switching 3A CCs. In these cases, manual recovery must be performed via the SSP which allows maintenance personnel the capability of forcing the system into a fixed configuration.

H. Diagnostic and Repair

4.34 A diagnostic is a test sequence that localizes a fault to an area for repair. The diagnostics operate on a "start small philosophy." This means that a small portion of the 3A CC is first diagnosed by the on-line 3A CC. If this portion of the off-line 3A CC operates properly, it may be used for further diagnosis. For example, before the on-line 3A CC runs any diagnostics on the off-line 3A CC, the maintenance channel must first be checked to verify its proper operation. As the diagnostics continue, that portion of the 3A CC that has been checked increases until correct operation of the total 3A CC is verified. If a failure occurs in the diagnostics, a TTY message is printed which gives a trouble number. This trouble number, when looked up in the appropriate trouble locating manual, should indicate the cause of the trouble. Maintenance personnel must then take the appropriate repair actions, such as the replacement of a circuit pack.

MAIN STORE

4.35 The 3A CC and MAS are duplicated in the 3A Processor for system reliability. Each 3A CC and its associated MAS is a switchable entity which is put on-line or off-line as a unit.

4.36 In normal operation, the on-line 3A CC keeps the standby store up to date; ie, the on-line 3A CC not only writes into its own store, but also into the MAS of the standby 3A CC. This keeps the standby control unit ready to take control from the on-line control unit in the event of a switch.

4.37 The two basic means of communication between the 3A CC and MAS are the main store bus (MASB) and an I/O subchannel. The MASB is the normal means of communication, and the I/O subchannel is used for diagnostic purposes.

A. Main Store Bus

4.38 The 3A CC is designed to use a direct-coupled store bus in an asynchronous mode. The asynchronous mode of operation provides the system with the flexibility of memory hardware. The

address portion of the bus is unidirectional, while the data portion of the bus is bidirectional.

4.39 The MASB consists of 53 leads. The address and data leads of the MASB are bit-sliced so that the parity bits provide adequate error detection. The 3A CC commands sent to the MAS are encoded in 2-out-of-4 codes which facilitate error detection.

B. Input/Output Subchannel

4.40 An I/O serial subchannel is provided to each controller from each 3A CC. The I/O subchannel from the 3A CC of the same control unit as the MAS has priority over the I/O subchannel from the duplicate 3A CC. The higher priority I/O subchannel is used in the initial program loading procedure to initialize the controller so that the store can be loaded. The I/O subchannel permits the on-line 3A CC to access the store of the other 3A CC for diagnostic purposes. This I/O subchannel will return either the information sent to the store by the 3A CC (loop-around) or the contents of the error register.

4.41 The MAS I/O circuitry is composed of a 21-bit shift register, I/O command decoder, 16-bit buffer register, error detection, control, and logic conversion circuitry. The shift register functions as a parallel-in, parallel-out register. The buffer register has a parallel interface to the shift register.

4.42 The MAS performs the following types of operations:

- Read
- Write
- Refresh.

4.43 Read/write, row address, column address, and chip address are derived from information received on the bus. Chip select and memory enable are derived from the MASC timing shift register. Chip select and the decoded (3 address bits) chip select are combined to provide an enabling signal to the selected 4K-bit chips. Memory enable is necessary to gate memory data from the memory planes to the MASC data register. A refresh signal (from fanout boards) is present on all memory planes of a MAS during a refresh interval. During refresh, the row address (6 address bits) bits are active and determine which one of the 64 rows of each chip in the main store is to be addressed. A refresh causes all the bits in the addressed row to be read. Reading causes the stored data to be rewritten or refreshed.

DIRECT MEMORY ACCESS

4.44 The state of the DMA and the information pertinent to data transfer of the devices are stored in various internal DMA registers. The state, mask, control, status, error data, and memory data registers are single-word registers that are used by all the devices attached to an MPCH located in the DMA. The data buffer, flag, parameter, present address low (PAL), present address high (PAH), final address low (FAL), and final address high (FAH) are 16-word registers that contain one word for each active peripheral device.

A. DMA Registers

4.45 The ***data buffer register*** provides intermediate storage between the peripheral device and the memory. When the device sends a word to memory, the word is first stored in the data buffer register. While the next request is being served, the first word is then sent to memory and the second word is brought into the data buffer. In this way, time required to access the memory and time required to fetch the next word from the device can be overlapped. The data buffer register is used in the same manner when a transfer from memory to the device is made.

4.46 The ***parameter register*** is used to establish the conditions relevant to a data transfer such as the SPCH address of the device. Conditions are fixed until the data transfer is complete. The ***flag register*** monitors progress of the transfer and principally maintains the error status.

4.47 The ***control register*** contains information pertinent to data transfers of all active devices. When bit 15 of the control register is set, the other 3A CC is prevented from accessing the memory. The remaining bits are used primarily for maintenance purposes.

4.48 Error conditions detected by the DMA are flagged by setting bits in the ***status***

register. Bit 5 (DMA error) is a summary status bit that reports the existence of an error. Any error condition detected locks the DMA in the state where the error was found.

4.49 The ***memory data register*** is used as a buffer for interfacing with the memory bus. It operates in conjunction with the ***error data register,*** which is loaded with data from the memory when the memory controller signals a parity error on a read command. With a parity error indication, the DMA will abort the data transfer for the device. Later, the 3A CC can read the error data register and analyze the data. It can then redirect the DMA to read data from the other memory or invoke complement corrections and restart the data transfer from the same memory.

4.50 Different states of the DMA are generated by the ***state register.*** It is implemented by a parallel-in/parallel-out rotating shift register.

4.51 The ***mask register*** inhibits the direct memory access request (DMAR) signal from devices which are out of service. When a bit corresponding to a device is set to zero, the DMA will not respond to the request. This allows the DMA to continue functioning even if some DMAR leads are stuck at zero.

4.52 The ***PAL register*** is used to contain the low 16 bits of the MAS address for the present MAS access. The ***PAH register*** is used to contain the high four bits of the ***present*** MAS address plus four parity bits used across the 20-bit present address. Similarly, the FAL and FAH registers, including parity bits, contain the MAS address for the ***final*** MAS access.

4.53 In order to initiate a data transfer, the 3A CC loads the PAL and PAH registers with the address of the first memory location to be read or written. If a memory write is to be performed, FAL and FAH are loaded with address of last memory location to be written. If a memory read is to be performed, FAL and FAH are loaded with last address plus one.

4.54 The PCH and DMA instructions are required to set up the DMA transfer for a device. The PCH instructions are used to set the device to a proper state, and DMA instructions are used to prepare the DMA for processing the data transfer for the device. The address of the PCH associated with the DMA (010101) should be used for all PCH instructions, and the address of the DMA (010110) should be used for all DMA instructions.

B. DMA Operation

4.55 When the system is first turned on, the initialization DMA instruction should be executed to place the DMA in a known inactive state. The DMA can be brought to an active state by writing 01010101 into the state register. Then the mask register is loaded with ones in the bit positions corresponding to the addresses of devices allowed to make DMA requests. In an active state, the DMA repeatedly senses whether there is a request from the 3A CC or from the devices according to their priorities. After the DMA has been set up properly for the data transfer from a device, the 3A CC commands the device to start the data transfer by using PCH instructions. The 3A CC is now available for other work while the DMA processes the data transfer between the device and the MAS. An interrupt will be generated from the device as soon as the data transfer is completed (final address reached) or when abnormal conditions are detected. Functions of the PCH (MPCH and SPCH) associated with the DMA are the same as the PCHs used for medium-speed devices and are covered in Section 254-300-130, I/O Interfaces.

PARALLEL CHANNEL INPUT/OUTPUT

4.56 The PCH I/O unit is composed of two functional modules: the MPCH (one per PCH I/O unit) and the SPCH (maximum of eight per PCH I/O unit).

A. Main Parallel Channel

4.57 The MPCH consists of the following functional subunits:

- Address circuit
- Information circuit
- Control circuit.

Address Circuit

4.58 The address circuit decodes the main channel select (MCS) and subchannel select (SCS)

codes on the parallel bus from 3A CC register R9. When the main channel select code matches the address of the MPCH, this circuit returns a 3-out-of-6 code to the 3A CC indicating that it has been selected, generates an internal activation signal to be used in other MPCH circuits, and decodes the subchannel select code. The circuit also sends an enable command to the selected subchannel. If MCS does not match the address of MPCH, no action is taken.

Information Circuit

4.59 The information circuit is composed of two identical circuit packs. Each pack interfaces a data byte (8 bits plus parity) between the 3A CC and the particular subchannel selected. Each circuit pack incorporates a mode control circuit, which may be stimulated to effect a report of the MPCH internal state to the 3A CC via general register R11. Control information is received from the MPCH control circuit pack defining the direction for data to proceed (ie, to the device on a write command or to the 3A CC on a read command) and whether the circuits should pass data or return status information.

Control Circuit

4.60 The control circuit provides necessary control signals to the other MPCH circuits and sends the proper device command code to identify the type of operation desired. This circuit contains a 7-bit state register with bits that are set under microprogram control by activation of miscellaneous decoder crosspoints in the 3A CC. Control information originates from the 3A CC (via miscellaneous decoder crosspoints) or from the DMA unit when used in the DMA. Section 254-300-130 contains information on the MPCH that is incorporated in the DMA unit.

B. Subparallel Channel

4.61 The SPCH serves as a transmitter/receiver and interfaces the MPCH unit with a transformer-coupled ac parallel bus. This ac parallel bus physically connects the PCH I/O unit with the dedicated peripheral devices via the duplex bus selector. The SPCH is composed of the following functional modules:

- Control/address circuit
- Information circuit.

Control/Address Circuit

4.62 The control/address circuit provides the interface for the parallel bus device address, control, clock, and response leads. This circuit returns a 2-out-of-5 check code to the MPCH when it is selected.

Information Circuit

4.63 The information circuit interfaces information data (16 data bits and 2 parity bits) between the MPCH and the ac parallel bus. It also provides an internal loop-around register for checking the integrity of the data path as desired.

4.64 When the PCH I/O unit is activated by the 3A CC, the MPCH checks message integrity, returns a response code to the 3A CC, and waits for crosspoint information used to initiate desired action. One of six possible crosspoints (MD2 through MD7) is then issued to the MPCH. A 1-out-of-6 code is stored in a 7-bit state register indicating the function to be performed (read data, write data, send device command, sense device status, identify interrupting device, or initialize duplex bus selectors). At the same time, MPCH determines when data is to be transmitted to the devices, transmits data when required, and transmits the device address.

C. AC Parallel Bus Interface

4.65 The ac parallel bus interface is used to connect the duplex bus selector (connected to the peripheral device) to the PCH I/O unit. The parallel bus interface consists of 35 leads: 6 address leads, 18 information leads, 6 control leads, 4 response leads, and a clock lead.

4.66 Six address leads are used to select the desired peripheral device. Five address leads (ADR0 through ADR4) select the desired peripheral device; the sixth lead (ADR5) provides for odd parity over the five address leads.

4.67 The 18 information leads (bidirectional) are used to transmit data and commands to the peripheral devices and receive data and status from the peripheral devices. The leads are broken down into two groups of nine each: INF(0) through INF(7) with INF lead P_L as the low parity lead

and INF(8) through INF(15) with INF lead P_H as the high parity lead. Each group corresponds to a data byte (8 bits plus parity): INF(0) through INF(7) plus INF bit P_L form the low data byte, and INF(8) through INF(15) plus INF bit P_H form the high byte.

D. Parallel Bus Interface Timing

4.68 Signals transmitted on the parallel bus interface are bipolar pulses. These pulses are 150 nanoseconds wide and use positive voltage to indicate a one and negative voltage to indicate a zero. Address and data information signals (if provided) are sent at the same time, with command signals sent following a 150-nanosecond delay. Upon receipt of the peripheral devices response, the control signal is cleared. The ensuing removal of the response triggers clearing of the address and data leads. The minimum input/output transaction execution time is 2.7 microseconds. The 3A CC will wait up to 10 microseconds for the device to respond. After 10 microseconds, the operation will be timed out and terminated.

CTI/POWER UNIT

4.69 The CTI/power unit is located at levels 62 to 70 of the 3A Processor frame. It provides the logic level shifting between 3-volt collector diffusion isolation (CDI) integrated circuits used in the 3A CC and 5-volt transistor-transistor logic integrated circuits used in the DMA and PCH units. In addition, the CTI/power unit contains three type 132M power supplies which furnish 5-volt power to the DMA, PCH 0, and PCH 1, as well as fuses and power alarm circuits.

4.70 Inputs to the CTI/power unit are gated from registers R9 and R10 gating buses in the 3A CC by miscellaneous decoder crosspoints. Logic levels of these inputs are shifted to the higher level required by DMA and PCH and are placed on the DMA and PCH input bus.

4.71 Information being returned from DMA and PCH to the 3A CC is shifted to lower voltage levels required by the 3A CC logic in the CTI/power unit and is gated onto the register R11 gating bus.

4.72 The CTI/power unit requires +3 volt power which is supplied by a 3-volt dc-to-dc converter located in the 3A Processor frame power unit. When a DMA unit is installed, the 132M power supply which provides +5 volts for DMA also supplies +5 volts for the CTI/power unit. In installations that do not use DMA, CTI/power unit is connected to the PCH 0 +5 volt power supply.

4.73 Additional information on the CTI/power unit, PCH, and DMA units is contained in Section 254-300-130.

TELETYPEWRITER CHANNELS

4.74 Two TTY channels, the maintenance TTY channel and the miscellaneous TTY channel (Fig. 17), are normally provided for communications between operating personnel and the 3A Processor. The maintenance TTY channel processes all maintenance messages between the 3A CC and personnel. The miscellaneous TTY channel normally processes administrative messages and has an autoconnect (dial-up and call back) arrangement that is available to other users whenever needed.

A. Maintenance Teletypewriter Channel

4.75 The maintenance TTY channel is the basic communication link between the 3A Processor and maintenance personnel. Input messages are typically used by the maintenance personnel to request a specific diagnostic test or to request a special report on some internal condition. Output messages consist of alarm status conditions, trouble indications, results of trouble diagnostics, and replies to interrogation requests as well as automatic periodic reports of normal occurrences.

4.76 The 3A Processor is designed to operate at an unattended office. Therefore, maintenance is expected to be the primary responsibility of a remote location, typically an SCC or technical assistance center. This means that at least one remote maintenance TTY will be located at the attended location. Both the local and remote maintenance TTYs are connected to the same TTY channel and receive the same messages from the system.

B. Miscellaneous Teletypewriter Channel

4.77 The miscellaneous TTY channel is used for all purposes other than maintenance, such as, office administration, traffic reporting, etc. These other uses of teletype channels are much less critical than maintenance functions. In a small

office, the other functions actually require very little usage of the miscellaneous channel. For instance, service orders in a small office should not be more than a few per week. Likewise, since there is relatively little equipment on which to report, traffic printouts will be quite short. For these reasons, the use of the miscellaneous TTY channel is shared by several users to perform various functions.

4.78 The miscellaneous TTY channel is also available to serve as backup protection for the maintenance TTY channel. Maintenance personnel can access the miscellaneous TTY channel in the same way as any other user (dial-up and call back). During such times, the miscellaneous TTY channel is not available for other functions. The other users of the miscellaneous TTY channel are deferred until the maintenance TTY channel is restored to normal service.

C. Autoconnect Teletypewriter Channel

4.79 The autoconnect facility provides a means for establishing dial-up connections to TTY channels to handle remote TTY functions (Fig. 17). This minimizes the need for using trunks to perform remote TTY functions.

4.80 To provide autoconnect for a remote office, the data set of the remote TTY is connected to a data coupler. The use of a data coupler in connection with a standard data telephone set provides manual answering and call origination features. The standard data telephone set is equipped with an exclusion feature to be used to switch between voice and data modes. The exclusion feature is wired so that the coupler set is off-line in the voice mode and the data telephone set is off-line in the data mode.

4.81 When the 3A Processor is operating normally (unattended), maintenance messages are sent to the remote SCC via port 1 of TTYC 0 and the private line. Port 0 of TTYC 1 is unused and port 1 of TTYC 1 serves autoconnect users. When the office is unattended, the maintenance messages are printed out on the local TTY via port 0 of TTYC 0. Other configurations are possible, depending on system requirements.

D. Controller Logic of a Teletypewriter Channel

4.82 A block diagram of TTY channels is shown in Fig. 17. Each TTY channel provides controller logic, four ports, and from one to four TTYs, depending upon port assignments. A TTY channel is connected to each 3A CC via an I/O subchannel and an interrupt control lead. The TTY functions with the 3A CC on a demand (rather than scheduled) interrupt basis. An interrupt is sent to the 3A CC at the end of the last bit for both input and output characters. The normal response of the 3A CC to a TTY interrupt is to poll the controller with a control message. This allows the controller logic of a TTY channel to return the character just received or sent, or to return a status message.

4.83 The controller logic is the transmit/receive means between the 3A CCs and TTYs on a TTY channel. The controller logic enables:

(a) Character transmission from the 3A CC to the TTY, and

(b) Character transmission from the TTY to the 3A CC

The controller logic contains channel and line circuits (Fig. 19). The channel circuits contain the buffer, control, and interface between the 3A CC and the line circuits. The line circuits contain the buffers, control, and interface between the TTY ports and the channel circuits. Within the channel circuits is the line status buffer. This buffer contains four enable bits and four alarm bits. The enable bits determine which port and TTY will receive a character from the 3A CC. Normally, all four ports are enabled, but this is a function of the TTY programs. The alarm bits of the buffer give a trouble indication for each TTY device connected in the TTY channel.

4.84 Each one of the four ports may access either a local or remote TTY (option of the operating company). However, only one TTY (regardless of whether it is local or remote) is used per port.

4.85 The TTY output information can be distributed to each port independently or to any combination of ports, including all four in parallel. However, if a number of devices are receiving a simultaneous message, the slowest device determines the time required to receive the message. Even

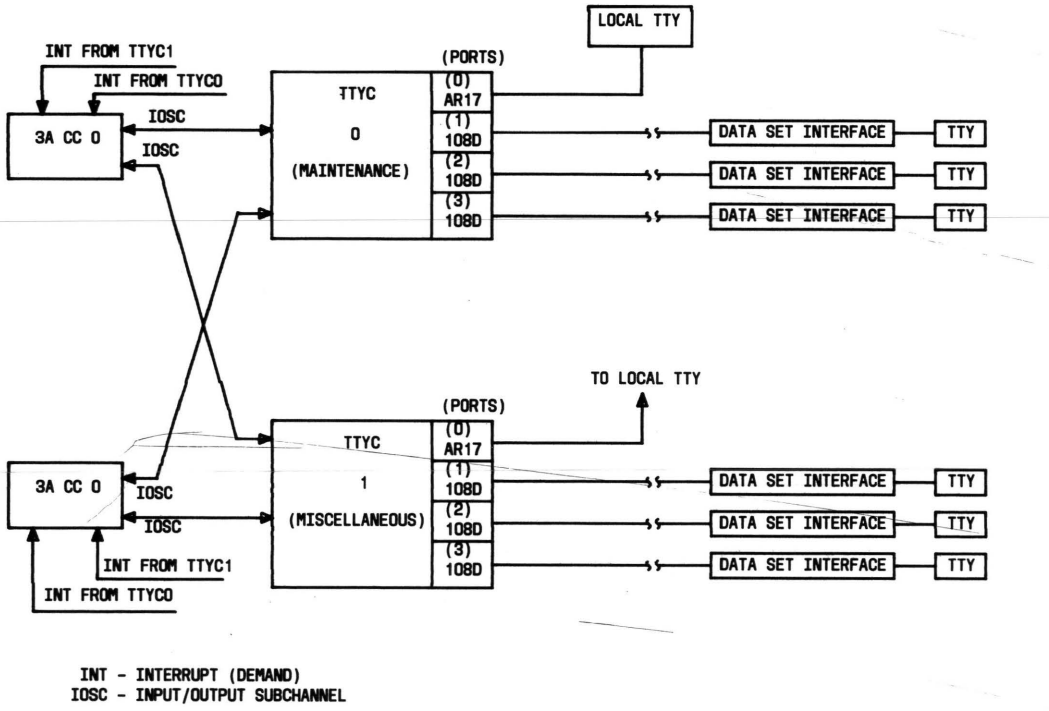


Fig. 17—TTY Channels Block Diagram

though the TTYs may receive messages simultaneously, they cannot transmit messages to the controller logic at the same time. Basically, the TTY that requests service first should be given first service. However, when more than one TTY tries to transmit characters to the controller logic at the same time, the message is garbled and the appropriate response is given at the TTY.

4.86 Communication between the 3A CC and TTY is serial in nature (consisting of an 11-bit message and 10 zeros which make up the 21-bit serial bipolar pulse messages). TTYs receive and transmit a character or function by means of an 11-bit message. This 11-bit transmission pattern contains seven data bits, one parity bit, and three synchronizing bits (one start and two stop bits). The first transmit or receive sequence bit is always a space (0) called the start bit. The next seven bits are in the American Standard Code for Information Interchange (ASCII) format which completely defines the desired letter, number, symbol, or function. These bits are followed by the parity bit. (The rightmost bit of the binary code is the first code bit.) The entire 8-bit character is passed to the 3A CC application program. Eight bits are also sent to the TTYs even if they do not check parity. The last 2 bits of the 11-bit message are the stop bits and are always a mark (1). Since a character (11-bits) is transmitted in 100 ms, each bit is approximately 9.09 ms in duration.

4.87 Descriptions and detailed operations of the TTYs are given in the following sections:

(a) The 33-Type TTY Sets—Section 574-100-101

(b) The 35-Type TTY (RO and KSR) Sets—Section 574-201-100

(c) The 35-Type TTY (ASR) Set—Section 574-202-100.

4.88 A DBS is mounted in the peripheral device it serves and therefore is not considered a part of a 3A Processor. The following discussion of DBS functions is provided to aid in understanding interface connections between 3A Processor and its periphery.

DUPLEX BUS SELECTOR

4.89 A simplified block diagram of a 3A Processor and its utilization of the DBS is shown in

Fig. 18. The parallel channel consists of up to eight subparallel channels and one controlling main parallel channel. Each subparallel channel controls a unique parallel bus and can service up to 16 peripheral devices on that bus. Each peripheral device requires a DBS for interfacing the the parallel bus. The parallel bus is a transformer-coupled 35-lead ac bus and employs bipolar pulses. It is the communication link which provides for peripheral device addressing, transfer of information between the subparallel channel and peripheral devices, control signals to the peripheral devices, and response signals from the peripheral devices. One other lead, DMAR, separate from the 35-lead bus provides an additional response signal from each DBS to the DMA channel. The peripheral devices interface to duplicate parallel buses via a DBS, thus allowing access to peripheral devices from either central control in a duplex processor configuration.

4.90 The DBS is a two-ported device and functions as a multipole, double-throw switch connecting peripheral devices to the active central control. Duplicate halves of the DBS (side 0 and side 1) interface with the corresponding duplicate processor channels. Common circuitry in the DBS interfaces the selected side of the DBS with the peripheral device. Under normal conditions, the DBS is functionally invisible to both the active processor and the peripheral devices. However, during diagnostics and system reconfiguration, the DBS can be instructed to intercept and execute I/O commands. The DBS converts the ac bus signals to transistor-transistor logic (TTL) levels and passes these signals from the active central control to the peripheral device. Conversely, the DBS converts TTL level signals from its peripheral device to bipolar ac pulses for transmission to the central control.

TAPE DATA CONTROLLER UNIT

A. Tape Data Controller Units

4.91 The TDC unit combines the TDC circuit, CTT, tape cartridge, and power to provide a backup facility for the MAS data. Each 3A CC has its own dedicated TDC and may also access the other TDC. Fig. 19 is a functional block diagram of the TDC unit. Each tape cartridge contains all the program and translation data which reside in the MAS. It also contains other programs vital to system operation but which are only used periodically. These programs are referred to as nonresident (since they are stored external to the MAS) and include device diagnostics, etc.

4.92 The functional block diagram of the TDC identifies the circuits required to interface between the 3A CC and CTT. Each of these circuits has a particular function and may be addressed (enabled) as required under software control. The function of each is described in the following paragraphs:

Serial Peripheral Interface (SPI)

4.93 The SPI (part of Fig. 19) is the interface between the serial subchannel at the 3A CC and the TDC. It provides the means to communicate with the 3A CC and establishes the timing (clock), control (commands), and data signals (information and reply) to the other circuits of the TDC.

Synchronous Data Set Controller (SDSC)

4.94 The SDSC is an option which is installed to provide communication between BUF and a user supplied synchronous data set used to transmit MAS data to a regional center.

Buffer (BUF)

4.95 BUF (part of Fig. 19) provides two serial buffer memories (two shift registers, BUF0 and BUF1, each containing 1024 bits, their associated counters and flags) which temporarily store data in transit to or from the CTT on SDSC.

Cartridge Tape Transport Controller (CTTC)

4.96 CTTC (part of Fig. 19) handles control and timing signals and data transfers to or from the CTT. It also provides automatic generation and stripping of preamble and postamble characters and performs a read-after-write check of data written on magnetic tape.

Bus Terminator (BT)

4.97 BT (part of Fig. 19) provides the proper electrical terminations for the serial and parallel buses used within the TDC. It also generates

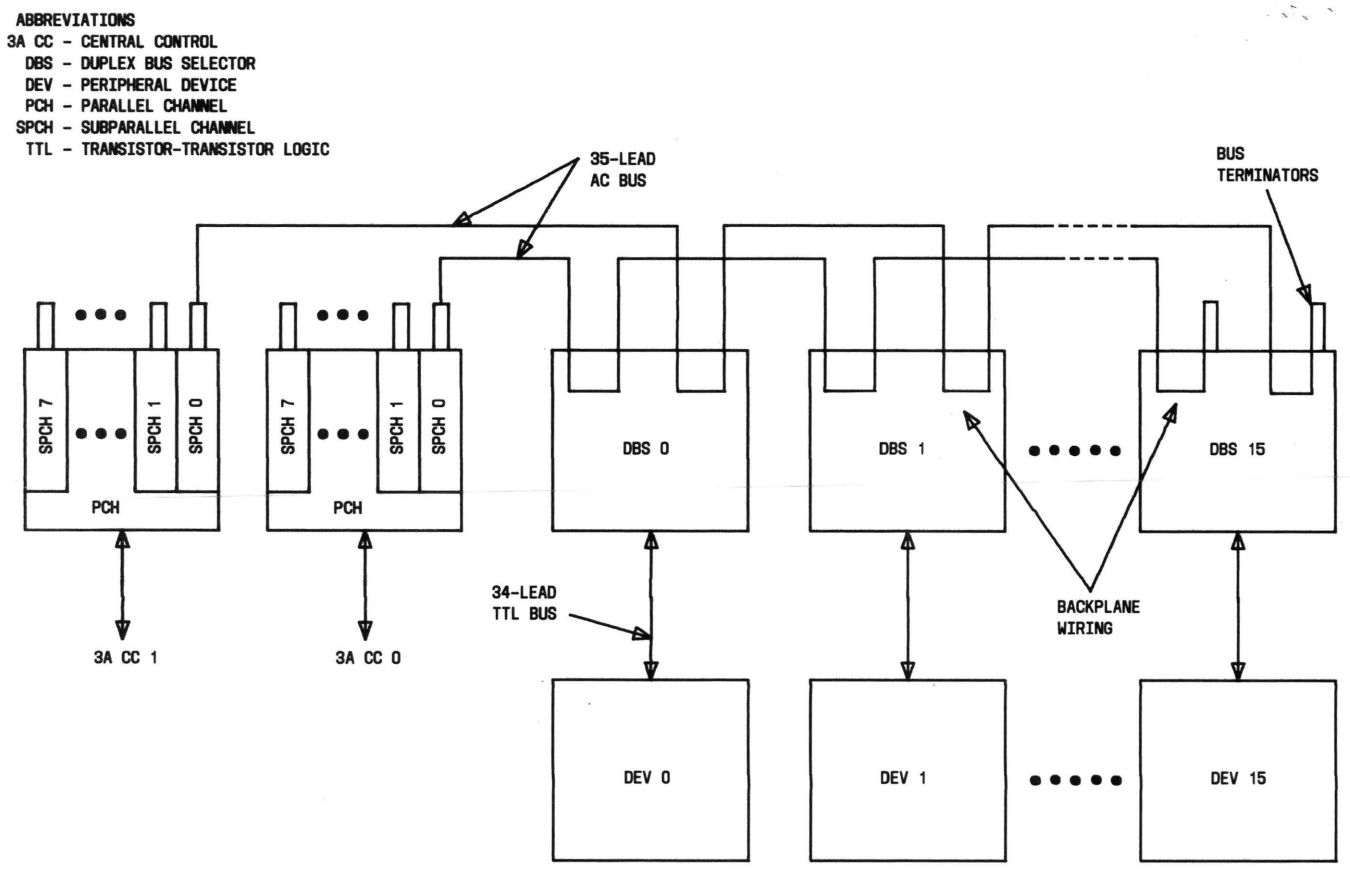


Fig. 18—DBS Utilization

the proper parity for status words originating from other circuits (BUF, SDSC, and CTTC) in the TDC and serves as a "pseudo device" for maintaining the buses within the TDC circuit.

B. Cartridge Tape Transport

4.98 The CTT (part of Fig. 19) provides four circuit packs (CP1 through CP4) and a capstan motor. The circuit packs and their functions are listed below:

Circuit Pack 1

4.99 CP1 provides a logic and control circuit that decodes motion commands from the CTTC and indicates the status of the CTT system.

Circuit Pack 2

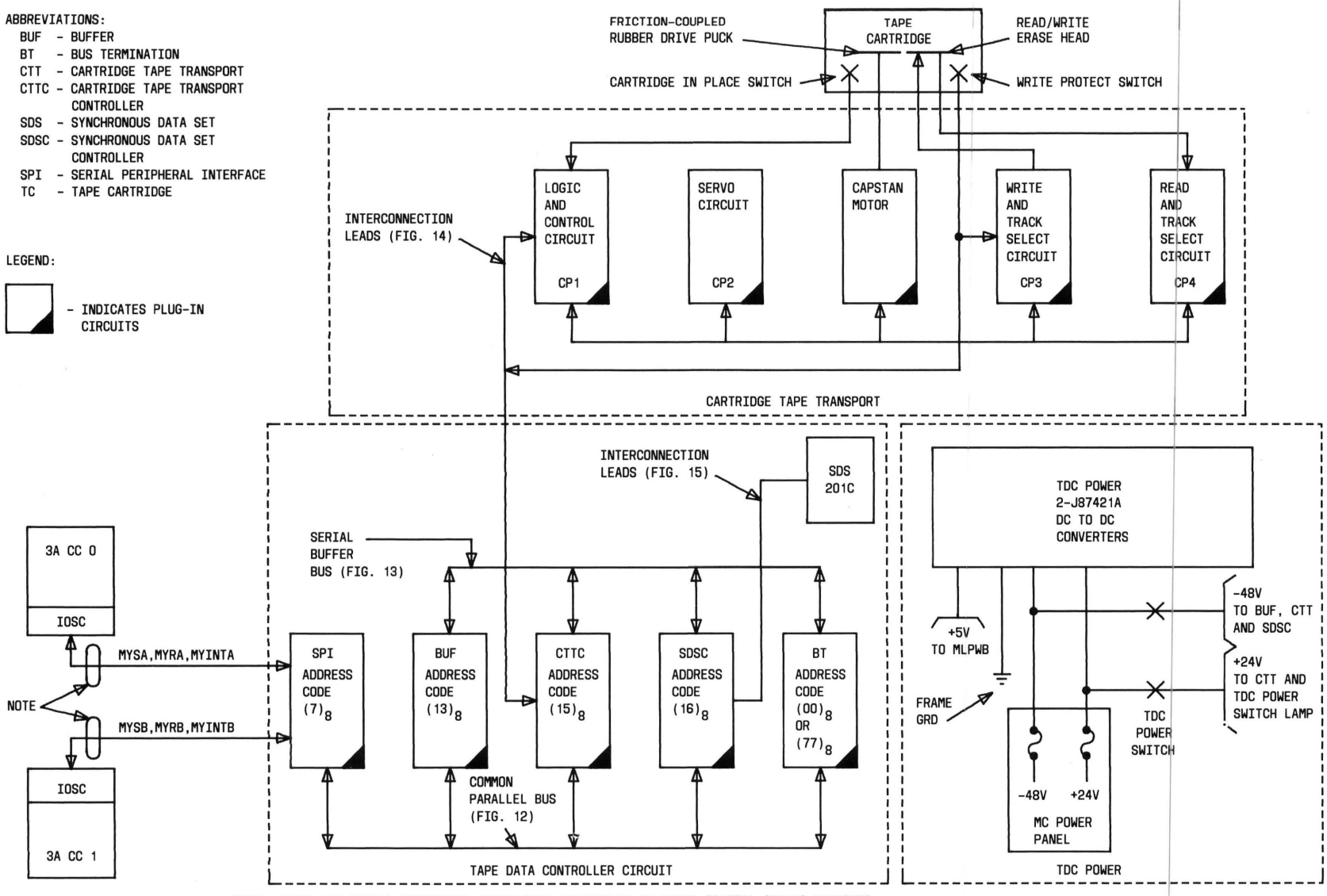
4.100 CP2 responds to the motion commands to control the direction and speed of the capstan motor that drives the tape. It also decodes the tape marks (holes) to provide position status (beginning of tape, early warning, load point, and end of tape).

Circuit Pack 3

4.101 CP3 decodes the commands for the write and track select (1-out-of-4) and provides write data to the write head in a serial, phase-encoded format. Input from the logic and control circuit (CP1) can inhibit the writing of data. CP3 permits the writing of data on magnetic tape at a tape speed of 30 inches per second.

Circuit Pack 4

4.102 CP4 reads information from the magnetic tape at 30 inches per second, decoding it into digital data. This circuit selects 1-out-of-4 tracks based on the input from CP1.



NOTE: THESE ARE SERIAL SUBCHANNEL BUSES EACH CONSISTING OF THREE COAXIAL CABLES EQUIPPED WITH TWO LEADS EACH (POSITIVE AND NEGATIVE) I.E., MYSAP AND MYSAN.

Fig. 19—TDC Block Diagram

C. Tape Cartridge

4.103 A tape cartridge contains approximately 300 feet of 1/4 inch wide magnetic tape. Data is written on tape in blocks separated by a 1.55-inch interblock gap. A block contains an integer multiple of 64 words. The first word is a block identifier and the last is a cyclic redundancy check word. In addition the CTTC adds a preamble and a postamble.

5. POWER

INTRODUCTION

5.01 Power is supplied to the 3A Processor via -48 volt buses and +24 volt converters. The -48 volt source is located in the power frame, and the +24 volt converters are located in the miscellaneous power frame.

5.02 Two -48 volt buses (A and B) provide power to the message switch. Bus A is associated with SYC 0, and bus B is associated with SYC 1.

5.03 The two 24-volt converters, located in the miscellaneous power frame, supply power to the processor frame and the maintenance frame. The 24-volt converter 0 supplies SYC 0 and the 24-volt converter 1 supplies SYC 1.

FUNCTIONAL DESCRIPTION

5.04 The functional description of power and alarms is as follows:

(a) Processor frame power

(b) Maintenance frame power

(c) PROMATS frame power

(d) Alarms.

A. Processor Frame Power

Note: The following functional description applies to each bay of the processor.

5.05 The +24 volts, filtered at the base of the frame, and -48 volts are distributed to the power converters in the MASC, the MAS, and the processor power unit.

5.06 The MASC power converters convert -48 volts to +3 volts which is distributed over the MLPWB to power the individual circuit packs in the MASC.

5.07 The MAS derives its power from dc-to-dc converters which convert -48 volts to +3 volts, +5 volts, +12 volts, and -5 volts.

5.08 The processor power unit consists of power converters which convert -48 volts to +3 volts. The +3 volts is used by the individual circuit packs of the 3A CC units. The clock, microstore, and 3A CC panel LEDs require +5 volts; the panel lamps require +24 volts. The unit is equipped with AK-type relays, some of which function to initiate major or minor power related alarms. Others function to start the power converters in the proper sequence.

B. Maintenance Frame Power

5.09 The +24 volts, filtered at the base of the frame, and -48 volts are distributed to power converters located in the E2A telemetry unit, TDCs 0 and 1, TTYCs 0 and 1, and the maintenance frame power unit.

5.10 E2A power converters supply required voltages to the 202T data set and individual circuit packs.

5.11 TDC 0 and 1 converters convert -48 volts to +5 volts to supply the individual circuit packs.

5.12 Each TTYC 0 and 1 is equipped with one converter which converts -48 volts to +3 volts for the logic circuit packs. The -24 volt regulator supplies voltage to the 108D data sets and AR17 circuit packs.

5.13 The maintenance frame power unit is equipped with two converters which supply +3 volts and -12 volts to the circuit packs mounted on the system status panel controller. This unit also supplies +24 volts to the SSP for lamps and LEDs. The unit monitors its own voltage and current and that of the power converters for the TDCs and TTYCs, thus providing the facility for visual and audible indications under normal or fault conditions.

C. PROMATS Frame Power

5.14 Bus power (-48 volts) for PROMATS connects at the top rear of the frame. It then connects to the fuse block on the DBS unit where it is fused for 8 amperes.

5.15 From the fuse, -48 volts is supplied to the KS-21104 dc-to-dc converter. The dc-to-dc converter supplies +5 volts, -24 volts, and ±15 volts for the tape transport; and +5 volts for the logic chassis within the PROMATS frame.

D. Alarms

5.16 In the normal operating condition (no fault), the audible alarm is off and alarm indicating lamps on the SSP are off. In the event of a power source or path failure, the following occurs:

- The corresponding indicator lights on the SSP
- A message giving definition of the fault is printed on the maintenance TTY
- An audible alarm sounds to call attention to the occurrence of the fault.

5.17 Refer to Section 254-300-140, Processor Power System, Common Systems for further information on processor powered alarms.

6. MAINTENANCE

INTRODUCTION

6.01 The objective of the maintenance system is to provide continuous service. The primary functions of the maintenance design to meet this objective are automatic fault detection, automatically initiated recovery, and effective diagnostic capability.

A. Redundancy

6.02 Duplication of equipment in the 3A Processor provides two sets of equipment, either of which is capable of controlling the system. The active 3A CC keeps the standby memory up to date and prepared for a rapid switch. Units duplicated are 3A CC, MAS, TDC, CTT, TTYC, and PROMATS.

B. Automatic Fault Detection

6.03 Continuously operating self-checking circuits within the 3A CC and the MASC provide immediate automatic detection of faults. This eliminates the need for operating match comparisons between the active and standby equipment. Periodic diagnostics and periodic progression tests are also available and used for detection of faults.

C. Automatically Initiated Recovery

6.04 For duplicated units, the system will retry, if possible, the activity which failed first. If still unsuccessful, it will switch to the redundant standby unit to continue service.

6.05 Unduplicated units are subject to programmed error analysis and/or quick checks, to verify their condition prior to removal from service.

D. Diagnostic Tools

6.06 Nonresident diagnostics can be initiated manually via the maintenance TTY. Isolating the fault to a specific item of hardware is accomplished by correlating the TTY printout with the TLM.

MAINTENANCE FACILITIES

6.07 The maintenance facilities which pertain to the 3A Processor are the SSP, E2A telemetry unit, and the maintenance and administrative TTY.

A. System Status Panel

6.08 The SSP provides the following features:

- System initialization
- Force and lock
- Alarms (visual)
- Alarm control
- System status
- Critical indicators to SCC
- Test control
- Display buffer.

B. E2A Telemetry Unit

6.09 The E2A telemetry unit provides the following features:

- Critical indicators to SCC
- System scan points to SCC
- Control points to SCC.

C. Maintenance and Administrative Teletypewriter

6.10 TTYC 0 provides the maintenance channel for local or remote TTYs.

6.11 Under normal conditions TTYC 1 provides the administrative channel on an autoconnect (dial-up) basis for the switching control center or the technical assistance center. If the maintenance channel fails, the administrative channel takes over the maintenance channel functions on a priority basis.

7. REFERENCES

7.01 The following sections contain information pertaining to the 3A Processor. Additional applications information will be found in the sections pertaining to individual systems with which the 3A Processor is associated.

Section 254-300-110—3A Central Control, Description, Common Systems

Section 254-300-120—3A Central Control, Theory of Operation, Common Systems

Section 254-300-130—I/O Interfaces, Common Systems

Section 254-300-140—Processor Power System, Common Systems

Section 254-300-150—Main Store and Supplemental Store, Description and Theory of Operation, Common Systems

Section 254-300-160—Processor Maintenance Frame, Common Systems

Section 254-300-170—Tape Data Controller, Description and Theory of Operation, Common Systems

Section 254-300-180—System Status Panel, Description and Theory of Operation, Common Systems

Section 254-300-190—TTY and TTY Controller, Description and Theory of Operation, Common Systems

Section 254-300-200—PROMATS, Description and Theory of Operation, Common Systems.